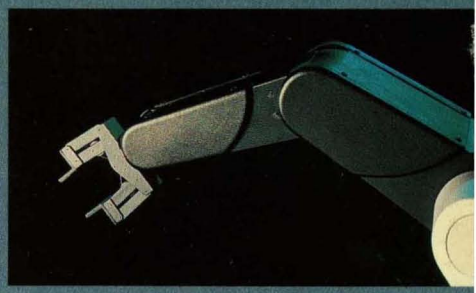
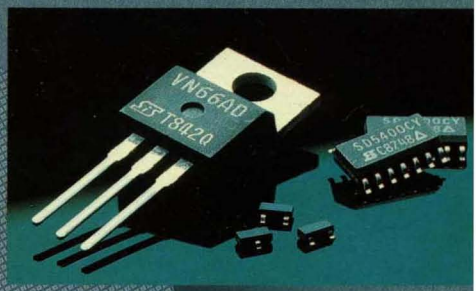
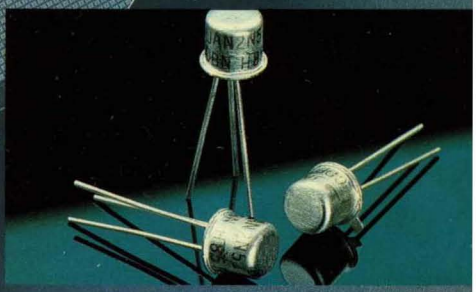
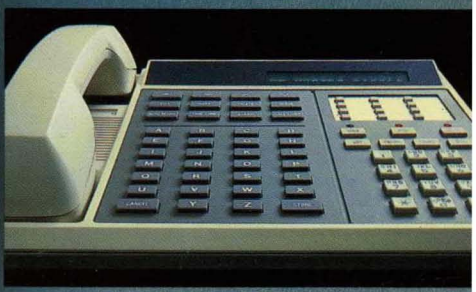
Low Power Discretes Data Book

Siliconix Low Power Discretes Data Book









Siliconix

1989

1989

LOW POWER DISCRETES

DATA BOOK

Siliconix
incorporated

Siliconix incorporated

Siliconix incorporated reserves the right to make changes in the circuitry or specifications at any time without notice and assumes no responsibility for the use of any circuits described herein and makes no representations that they are free from patent infringement.

Warning Regarding Life Support Applications

Siliconix products are not sold for applications in any medical equipment intended for use as a component of any life support system unless a specific written agreement pertaining to such intended use is executed between the manufacturer and Siliconix. Such agreement will require the equipment manufacturer either to contract for additional reliability testing of the Siliconix parts and/or to commit to undertake such testing as a part of its manufacturing process. In addition, such manufacturer must agree to indemnify and hold Siliconix harmless from any claims arising out of the use of the Siliconix parts in life support equipment.

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. This is a stress rating only and not subject to production testing. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

Printed in U.S.A.

Siliconix incorporated

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Siliconix incorporated

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ALPHA-NUMERIC INDEX

NUMERIC-ALPHA INDEX

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LOW POWER DISCRETES DEVICE ORDERING INFORMATION

TECHNOLOGY/DESIGN PREFIX-DEVICE FAMILY

BF	-European Transistor Standard Diode TO-92 Cased FET
CR	-Si Standard N-Channel Current Regulator
CRR	-Si Standard N-Channel Current Regulator
DM	-Si Special DMOS FET
DN	-Si Dual N-Channel JFET
FN	-Si N-Channel JFET
DPAD	-Si Standard Dual JFET Diode
J	-Si Standard TO-92 Cased FET
JR	-Si Standard Current Limiter
JPAD	-Si Standard JFET Diode
MU	-Si Special MOSFET
ND	-Si Standard Low Power MOS
PAD	-Si Standard JFET Diode
PN	-Si Standard TO-92 Cased FET
SD	-Si Standard DMOS FET
SST	-Surface Mount Device
U	-Si Standard FET
V	-Si Standard or Special Low Power MOS
VCR	-Si Standard N- and P-Channel Voltage Controlled Resistors
2N	-JEDEC-Registered Device
3N	-JEDEC-Registered Device

PROCESS OPTION

-1 Contact Factory - 750B Visual, Mil-STD-750 Processing (JANTXV)

-2 Contact Factory - 750B Visual, MIL-STD-750 Processing (JANTX)

3 Contact Factory - 750B Visual, MIL-STD-750, Group B and C

PACKAGE

-05 Std TO-92 Lead Formed to TO-5 Pin Circle

-18 Std TO-92 with Center Lead Formed Toward Flat in TO-18 Pin Circle

-TR Tape and Reel Available on TO-92 FETs

-TA Tape and Ammo Pack Available on TO-92 FETs

-T1, T2 Tape and Reel Available on SOT-23, SOT-143 and SOIC Products

Hi-Rel Process Capabilities

INTRODUCTION

For over twenty years Siliconix has actively participated in the Military/Hi-Rel marketplace. The company has been a preferred source supplier on numerous major military programs with Low Power Discrete (LPD) devices designed into land, air, sea and space systems.

LPD products are logical choices in Military/Hi Rel applications for several reasons. There are performance benefits to be gained using LPD devices which cannot be matched with any other existing technology. LPD devices are inherently radiation-hardened, as high as 6 X 10^5 RAD (Si). They perform reliably at cryogenic temperatures proving they can operate as a "Focal Plane Preamp" at a liquid helium temperature of 35°K.

The LPD business unit is dedicated to serving the Military/Hi-Rel market and does so in five basic ways: QPL (Qualified Parts List) devices, CECC devices, Standard Hi-Rel Process Flows, Hi-Rel "Specials", and Lockheed Monitored Line devices.

QPL Devices (See Figure 1)

For ease of delivery and in keeping with the government trend towards standardized devices, the LPD product line offers 16 QPL devices (with more QPL quals in progress). These are products qualified under Military Specification Mil-S-19500, the General Specification for Semiconductor Devices. Parts are purchased by specifying the appropriate Government Designation on the purchase order. The LPD business unit is continuously evaluating the devices within its product line for candidates as additional QPL devices. Wherever a significant need is demonstrated, the LPD Business Unit is committed to addressing that need by seeking QPL approval from DESC.

CECC Devices (See Figure 2)

CECC 50 000 is the European system of electronic component approval in which product is released to internationally agreed detail specifications conforming to CECC rules. QPL listed products are built on an approved line by a manufacturer who must comply with defined standards relating to organization, facilities and quality assurance procedures.

Throughout Europe CECC approved components are preferred items for all military and aerospace programmes.

Standard Hi-Rel Processes (See Figure 3)

Where a QPL device does not exist, LPD offers the next best thing with its –1, –2 and LP3 process flows. The –1 process flow provides many of the 100% screening steps for a JANTXV-level device as called out in Mil-S-19500. U.S. Build is included. The –2 provides many of the 100% screening steps for a JANTX-level device as called out in Mil-S-19500.

The LP3 process flow provides 100% processing similar to Mil-S-19500 for a JANTX-level device using Mil-S-750 test methods. Group A, B, and C testing is included. Portions of the 100% screening and/or the Quality Conformance Inspection testing may be performed at any of Siliconix' worldwide facilities.

Use of these standard processes can eliminate the need for a costly source control drawing. The processes can be performed on any hermetic packaged LPD device. Devices are ordered by adding the –1, –2, –LPD3 as a suffix to the standard part type (i.e. 2N5432–1, 2N5432–2, 2N5432–LP3).

Hi-Rel "Specials"

Where QPL, CECC, –1, –2 and LP3 won't do, LPD can provide processing based upon a customer source control drawing or detail specification. Siliconix has built a reputation in the industry for its skill in manufacturing such devices commonly referred to as "Specials". All Mil-S-19500/Mil-Std-750 requirements through JANTXV-level processing can be provided. Baseline control, a "must" in many Military/Hi-Rel applications, is offered. Our dedicated Program Management group can provide the coordination necessary to commandeer the more complex specials through the factory.

Lockheed Monitored Line

Siliconix also offers Lockheed-monitored line parts. This means on-line process monitoring by a resident team of quality & reliability engineers. With approval from the U.S. Air Force, this service can be used by any aerospace company or government agency.

Conclusion

Since 1964 Siliconix has been regarded as a steady, reliable supplier to the Military/Hi-Rel market. We intend to carry this reputation into the future by providing Military/Hi-Rel service you can rely on for many years to come.

Figure 1

LOW POWER DISCRETE QUALIFIED PARTS LIST (QPL)

Products Qualified as Standard Devices under Military Specification

Mil-S-19500: Semiconductor Devices, General Specification For

GOVERNMENT DESIGNATION	SILICONIX DESIGNATION TYPE NUMBER	(CAGE) (CODE)	DETAIL SPECIFICATION (SLASH SHEET)
2N4091 (JAN) JANTX JANTXV	CDBN	17856 (FSCM)	Mil-S-19500/431
2N4092 (JAN) JANTX JANTXV	CDBN	17856 (FSCM)	
2N4093 (JAN) JANTX JANTXV	CDBN	17856 (FSCM)	
2N4856 (JAN) JANTX JANTXV	CDBN	17856 (FSCM)	Mil-S-19500/385
2N4857 (JAN) JANTX JANTXV	CDBN	17856 (FSCM)	
2N4858 (JAN) JANTX JANTXV	CDBN	17856 (FSCM)	
2N4859 (JAN) JANTX JANTXV	CDBN	17856 (FSCM)	
2N4860 (JAN) JANTX JANTXV	CDBN	17856 (FSCM)	
2N4861 (JAN) JANTX JANTXV	CDBN	17856 (FSCM)	
2N5114 (JAN) JANTX JANTXV	CDBN	17856 (FSCM)	Mil-S-19500/476
2N5115 (JAN) JANTX JANTXV	CDBN	17856 (FSCM)	
2N5116 (JAN) JANTX JANTXV	CDBN	17856 (FSCM)	
2N6661 (JAN) JANTX JANTXV	CDBN	17856 (FSCM)	Mil-S-19500/547A
2N6660 (JAN) JANTX JANTXV	CDBN	17856 (FSCM)	

↑ JANS: JANTXV plus wafer lot acceptance and additional 100% processing requirements. Includes Group D testing

↑ JANTXV: JANTX plus 100% internal visual inspection

↑ JANTX: JAN plus 100% processing to Mil-S-19500 including Group A, B, C testing

↑ JAN: Controlled lot with sample environmental and life testing

Figure 2

LOW POWER DISCRETE CECC 50 000 - QUALIFIED DEVICES

Additional Product Options for European Customers

At this time, member countries of the CECC (Cenelec Electronic Components Committee) are Belgium, Denmark, Germany, France, Ireland, Italy, the Netherlands, Norway, Sweden, Switzerland and the United Kingdom.

Specific device types are individually qualified against a fixed detail specification which has been approved by the British Standards Institute (BSI) acting as the national supervising agency on behalf of CECC.

The CECC 50 000 scheme is administered in the UK by the BSI. The UK-generated specifications are prefixed with the letters BS.

A number of industry preferred standard device types are now qualified and the following detail specifications are available:

Type Number	BS Specification	Type Number	BS Specification
2N3824	BS CECC 50 012-008	U430/U431	BS CECC 50 012-025
2N4391/2/3	BS CECC 50 012-004	2N5432/3/4	BS CECC 50 012-026
2N4856A/7A/8A	BS CECC 50 012-006	VQ1001	BS CECC 50 012-040
2N4220/1/2	BS CECC 50 012-009	CR022 through CR062	BS CECC 50 013-001
2N6659/60/6I	BS CECC 50 012-016	CR068 through CR150	BS CECC 50 013-002
2N5564/65/66	BS CECC 50 012-024	CR160 through CR530	BS CECC 50 013-003

Each of the approved types is now available with additional screening options, including high temperature reverse bias burn-in, of either 48, 72 or 168 hours duration. Screening details are appended to the detail specification and conform to appendix VI of the European Standard CECC 50 000 ISSUE 3.

Product is released with a BS CECC certificate of conformity and will have been submitted to:

1. Group A sample inspection (lot by lot)-quality assessment tests, assuring product conforms to electrical specification.

2. Group B sample inspection (lot by lot)-reliability tests, including package related tests and 168 hours electrical endurance, to identify potential early failures.

3. Group C sample inspection (periodic - 3 monthly)-long term reliability tests including 1000 hours of high temperature storage and electrical endurance.

Data from the inspection tests is available to the customer in the form of CTRs (certified test records).

Manufacturing of BS CECC product is carried out in the Siliconix UK facility located in Morriston, Swansea SA6 6NE, South Wales.

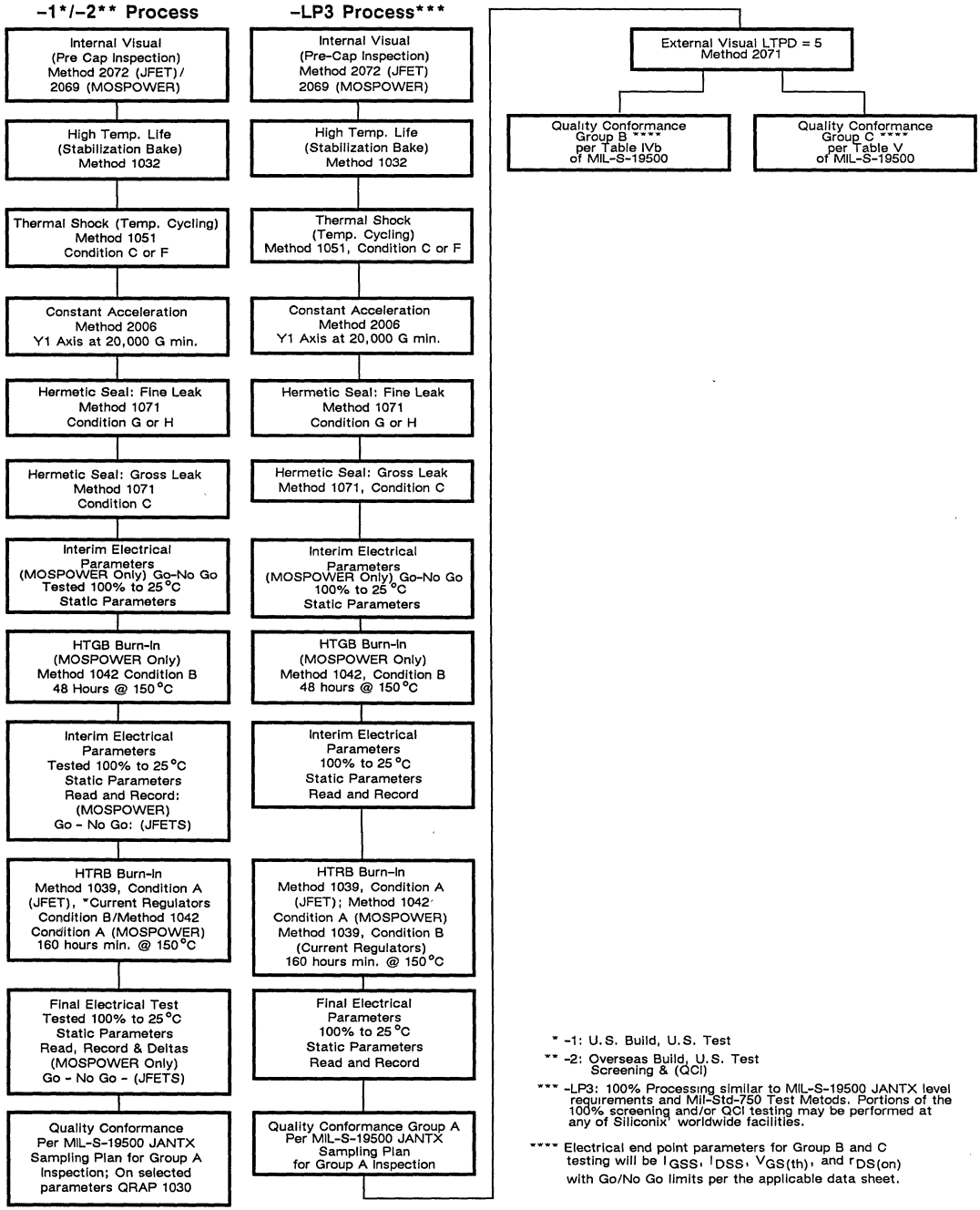
In addition to BS CECC approved product, the Siliconix UK facility can provide internationally recognized high-reliability screening options on standard products. These include Mil-750 and custom screening options.

JAN, JANTX or JANTXV processing for certain JEDEC-registered FETs can also be supplied.

For additional information and details of new/pending approvals, inquiries may be directed to the nearest sales office.

Figure 3

LPD PROCESS OPTIONS
HI-REL PROCESS FLOWS



* -1: U.S. Build, U.S. Test

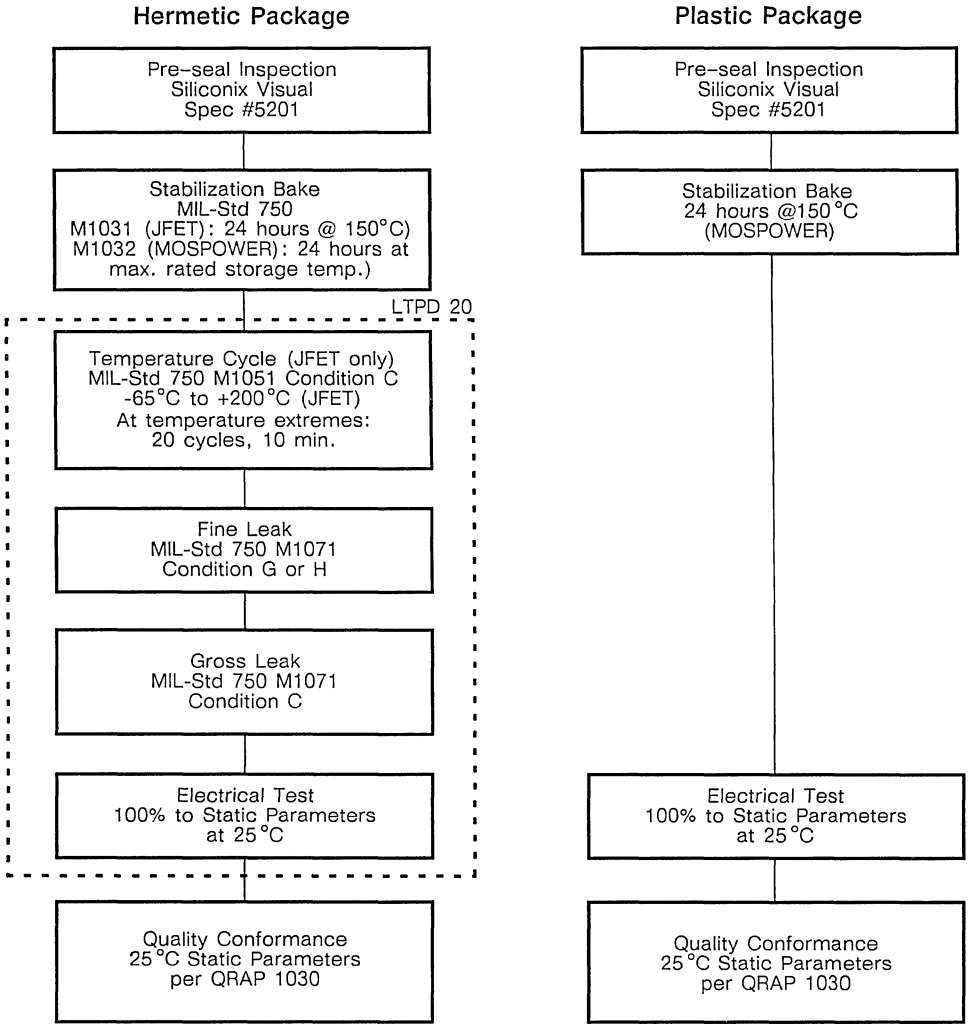
** -2: Overseas Build, U.S. Test Screening & (QCI)

*** -LP3: 100% Processing similar to MIL-S-19500 JANTX level requirements and Mil-Std-750 Test Metods. Portions of the 100% screening and/or QCI testing may be performed at any of Siliconix' worldwide facilities.

**** Electrical end point parameters for Group B and C testing will be I_{GSS}, I_{DSS}, $V_{GS(th)}$, and $r_{DS(on)}$ with Go/No Go limits per the applicable data sheet.

Figure 4

COMMERCIAL/INDUSTRIAL PROCESS FLOWS



CROSS REFERENCE

Siliconix Direct Replacement Suggestions are based on the similarity of mechanical and electrical characteristics, as reported in the manufacturer's published data. Interchangeability is not guaranteed. Before selecting a device as a substitute, compare the specifications.

Siliconix Similar Replacement Suggestions are based on the similarity of electrical characteristics, as reported in the manufacturer's published data. Interchangeablity is not guaranteed, as these parts may have different pin configurations. Before selecting a device as a substitute, compare the specifications. For devices not shown in this guide, or for additional information, the user should contact the nearest Siliconix sales office.

Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
AM0610LL	VN0610LL	
AM10LM	VN10LM	
AM2222LL	VN2222LL	
AM2222LM	VN2222LM	
A5T3821		2N4220
A5T3822		2N4221
A5T3823		2N4222
A5T3824		2N4220
A5T5460		2N5460
A5T5461		2N5461
A5T5462		2N5462
BFQ10	U401	
BFQ11	U401	
BFQ12	U402	
BFQ13	U403	
BFQ14	U404	
BFQ15	U405	
BFQ16	U405	
BFR30		SST203
BFR31		SST202
BFT10	SST202	
BFT10SM	SST202	
BFT11	SST230	
BFT11SM	SST230	
BFT46	SST4338	
BFW13	2N4867	
BF244A	BF244A	
BF244B	BF244B	
BF244C	BF244C	
BF256LA		2N5485
BF256LB		2N5485
BF256LC		2N5486
BSD10	SD2100	
BSD12	SD2100	
BSD20	SST2100	
BSD212	SD212DE	
BSD213	SD213DE	
BSD214	SD214DE	
BSD215	SD215DE	
BSD22	SST2100	
BSJ174	J174	
BSJ175	J175	
BSJ176	J176	
BSJ177	J177	
BSR174	SST174	
BSR175	SST175	
BSR176	SST176	
BSR177	SST177	
BSR56	BSR56	
BSR57	BSR57	
BSR58	BSR58	
BSR66		VN0606M
BSR67		VN0808M
BSR76		VN2410M
BSS100		VN1206L
BSS101		VN2406L

Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
BSS110		TP0610L
BSS124		VN4012L
BSS129	BSS129	
BSS138		VNO603T
BSS83		SST213
BSS84		TP0610T
BSS89	BSS89	
BSS92	BSS92	
BSS98		VN0603L
BST70		VN0808L
BST72A		VNO8O8L
BSV78	2N4856	
BSV79	2N4857	
BSV80	2N4858	
BS107	BS107	
BS107P	VN2010L	
BS170	BS170	
BS208	BS208	
BS250	BS250	
CIL-1300		J502
CIL-1301		J505
CIL-1302		J507
CIL-1303		J509
CIL-1304		J510
CIL-1305		J511
CIL-250		J511
CIL-251		J511
CL1020	CR100	
CL1520	CR150	
CL2210	CR022	
CL2220	CR220	
CL3310	CR033	
CL3320	CR330	
CL4710	CR047	
CL4720	CR470	
CL6810	CR068	
CRR0240	CRR0240	
CRR0360	CRR0360	
CRR0560	CRR0560	
CRR0800	CRR0800	
CRR1250	CRR1250	
CRR1950	CRR1950	
CRR2900	CRR2900	
CRR4300	CRR4300	
CR022	CR022	
CR024	CR024	
CR027	CR027	
CR030	CR030	
CR033	CR033	
CR039	CR039	
CR043	CR043	
CR047	CR047	
CR056	CR056	
CR062	CR062	
CR068	CR068	
CR075	CR075	

CROSS REFERENCE

Siliconix incorporated

Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
CR082	CR082	
CR091	CR091	
CR100	CR100	
CR110	CR110	
CR120	CR120	
CR130	CR130	
CR140	CR140	
CR150	CR150	
CR160	CR160	
CR180	CR180	
CR200	CR200	
CR220	CR220	
CR240	CR240	
CR270	CR270	
CR300	CR300	
CR330	CR330	
CR360	CR360	
CR390	CR390	
CR430	CR430	
CR470	CR470	
CR530	CR530	
C3141		PAD10
C3142		PAD50
C3143		PAD100
C3144		PAD500
DPAD1	DPAD1	
DPAD10	DPAD10	
DPAD100	DPAD100	
DPAD2	DPAD2	
DPAD20	DPAD20	
DPAD5	DPAD5	
DPAD50	DPAD50	
DU4339		2N6907A
DU4340	2N6907A	
ECG312		2N4416
ECG451		J210
ECG452	2N4416	
ECG456		2N4221
ECG457	J204	
ECG464		3N164
ECG466	2N4091	
ECG467	J111	
EPAD100	JPAD100	
EPAD200	JPAD200	
EPAD50	JPAD50	
EPAD500	JPAD500	
ESM25	U234	
ESM25A	U233	
ESM4091	PN4091	
ESM4092	PN4092	
ESM4093	PN4093	
ESM4302	PN4302	
ESM4303	PN4303	
ESM4304	PN4304	
E100	J203–18	
E101	J201–18	
E102	J202–18	
E103	J203–18	
E105	J105–18	
E106	J106–18	
E107	J107–18	
E108	J108–18	
E109	J109–18	
E110	J110–18	
E111	J111–18	
E111A	J111A–18	
E112	J112–18	
E112A	J112A–18	
E113	J113–18	
E113A	J113A–18	
E114	J114–18	
E174	J174–18	
E175	J175–18	
E176	J176–18	
E177	J177–18	

Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
E201	J201–18	
E202	J202–18	
E203	J203–18	
E204	J204–18	
E210	J210–18	
E211	J211–18	
E212	J212–18	
E230	J230–18	
E231	J231–18	
E232	J232–18	
E270	J270–18	
E271	J271–18	
E300		J212–18
E304	J304–18	
E305	J305–18	
E308	J308–18	
E309	J309–18	
E310	J310–18	
E400	U410	
E401	U411	
E402	U412	
E410	U410	
E411	U411	
E412	U412	
E420		U440
E421		U441
E430		U430
E431		U431
E500	J500	
E501	J501	
E502	J502	
E503	J503	
E504	J504	
E505	J505	
E506	J506	
E507	J507	
FE0654A		J210
FE0654B		J210
FE0654C		J202
FN4117	2N4117	
FN4117A	2N4117A	
FN4118	2N4118	
FN4118A	2N4118A	
FN4119	2N4119	
FN4119A	2N4119A	
FN4392	2N4392	
FN4393	2N4393	
FT704	3N163	
IMF3954		2N5146
IMF3954A		2N5146
IMF3955		2N5197
IMF3955A		2N5196
IMF3956	2N3956	
IMF3957	2N3957	
IMF3958	2N3958	
IMF5911	2N5911	
IMF5912	2N5912	
IMF6485	U405	
ITE3066		J202
ITE3067		J201
ITE3068		J201
ITE4091		J111
ITE4092		J112
ITE4093		J113
ITE4117		PN4117
ITE4118		PN4118
ITE4119		PN4119
ITE4338		J201
ITE4339		J204
ITE4340		J202
ITE4341		J204
ITE4391	PN4391–18	
ITE4392	PN4392–18	
ITE4393	PN4393–18	
ITE4416	PN4416–18	

Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
ITE4867		2N4867
ITE4868		2N4868
ITE4869		2N4869
IT100	2N5116	
IT101	2N5114	
IT108	2N5486	
IT109	U310	
IT1700	3N163	
IVN6002CND	VN40AD	
IVN6300ANF	VN0808M	
JPAD10	JPAD10	
JPAD100	JPAD100	
JPAD20	JPAD20	
JPAD200	JPAD200	
JPAD5	JPAD5	
JPAD50	JPAD50	
JPAD500	JPAD500	
JR135V	JR135V	
JR170V	JR170V	
JR200V	JR200V	
JR220V	JR220V	
JR240V	JR240V	
J105	J105	
J105-18	J105-18	
J106	J106	
J106-18	J106-18	
J107	J107	
J107-18	J107-18	
J108	J108	
J108-18	J108-18	
J109	J109	
J109-18	J109-18	
J110	J110	
J110-18	J110-18	
J110A	J110A	
J111	J111	
J111-18	J111-18	
J111A	J111A	
J112	J112	
J112-18	J112-18	
J112A	J112A	
J113	J113	
J113-18	J113-18	
J113A	J113A	
J114	J114	
J114-18	J114-18	
J1401	U401	
J1402	U402	
J1403	U403	
J1404	U404	
J1405	U405	
J1406	U406	
J174	J174	
J174-18	J174-18	
J175	J175	
J175-18	J175-18	
J176	J176	
J176-18	J176-18	
J177	J177	
J177-18	J177-18	
J201	J201	
J201-18	J201-18	
J202	J202	
J202-18	J202-18	
J203	J203	
J203-18	J203-18	
J204	J204	
J204-18	J204-18	
J210	J210	
J210-18	J210-18	
J211	J211	
J211-18	J211-18	
J212	J212	
J212-18	J212-18	
J230	J230	
J230-18	J230-18	
J231	J231	
J231-18	J231-18	
J232	J232	
J232-18	J232-18	
J270	J270	
J270-18	J270-18	
J271	J271	
J271-18	J271-18	
J300		J212
J300-18		J212-18
J300A		J210
J300B		J211
J300C		J211
J300D		J212
J304	J304	
J304-18	J304-18	
J305	J305	
J305-18	J305-18	
J308	J308	
J308-18	J308-18	
J309	J309	
J309-18	J309-18	
J310	J310	
J310-18	J310-18	
J401	U401	
J402	U402	
J403	U403	
J404	U404	
J405	U405	
J406	U406	
J4091	PN4091	
J4092	PN4092	
J4093	PN4093	
J410	U410	
J411	U411	
J412	U412	
J4302	PN4302	
J4303	PN4303	
J4391	PN4391	
J4392	PN4392	
J4393	PN4393	
J4416	PN4416	
J500	J500	
J501	J501	
J502	J502	
J503	J503	
J504	J504	
J505	J505	
J506	J506	
J507	J507	
J508	J508	
J509	J509	
J510	J510	
J5103	2N5485	
J5104	2N5485	
J511	J511	
J552	J552	
J553	J553	
J554	J554	
J555	J555	
J556	J556	
J557	J557	
J9100	J552	
KE4091		PN4091
KE4092		PN4092
KE4093		PN4093
KE4220		J202
KE4222		J203
KE4391		PN4391
KE4392		PN4392
KE4393		PN4393
KE4416		PN4416
KK4416-18	PN4416-18	
K114		J211

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Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
K114-18		J211-18
K210-18	J210-18	
K211-18	J211-18	
K300-18	J210-18	
K304-18	J304-18	
K305-18	J305-18	
K308-18	J308-18	
K309-18	J309-18	
K310-18	J310-18	
LDF603	2N4221A	
LD014CNC		JR240V
LSJ33A		J113
LS3069		J203
LS3070		J202
LS3071		J201
LS3458		J232
LS3487		J201
LS3819		J204
LS3821		J202
LS3822		J305
LS3921		2N4220
LS3967		J304
LS3968		J305
LS3969		J230
LS4220		J202
LS4221		J305
LS4223		J305
LS4224		J305
LS4339		J201
LS4340		J202
LS4341		J203
LS4391		J111
LS4392		J112
LS4393		J113
LS4416		PN4416
LS4856		J111
LS4857		J112
LS4858		J113
LS4859		J111
LS4860		J112
LS4861		J113
LS5103		J305
LS5104		J305
LS5105		J304
LS5245		J304
LS5246		J305
LS5247		J304
LS5248		J304
LS5358		J202
LS5359		J202
LS5360		J305
LS5362		J304
LS5363		J304
LS5364		J304
LS5391		J231
LS5392		J305
LS5394		J305
LS5395		J304
LS5396		J304
LS5457		J305
LS5458		J305
LS5459		J305
LS5484		J305
LS5485		J305
LS5486		J304
LS5556		J320
LS5557		J231
LS5558		J232
LS5638		J111
LS5639		J112
LS5640		J113
MEF101		J203
MEM511		3N163
MFE2010	2N5434	
MFE2011	2N5433	

Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
MFE2012	2N5432	
MFE3069	2N4341	
MFE3459	2N4339	
MFE3460	2N4338	
MFE3821	2N4220	
MFE3822	2N4221	
MFE910		VN10KE
MFE9200		VN2406L
MK10		J212
MMBFJ111	SST111	
MMBFJ112	SST112	
MMBFJ113	SST113	
MMBFJ113	SST113	
MMBFJ174	SST174	
MMBFJ174	SST174	
MMBFJ175	SST175	
MMBFJ175	SST175	
MMBFJ176	SST176	
MMBFJ176	SST176	
MMBFJ177	SST177	
MMBFJ177	SST177	
MMBFJ309	SST309	
MMBFJ309	SST309	
MMBFJ310	SST310	
MMBFJ310	SST310	
MMBFU310	SSTU310	
MMBF170		2N7002
MMBF4391	SST4391	
MMBF4392	SST4392	
MMBF4393	SST4393	
MMBF4416	SST4416	
MMBF4860	SST4860	
MMBF4861	SST4861	
MMBF5457	SST5457	
MMBF5459	SST5459	
MMBF5460	SST5460	
MMBF5461	SST5461	
MMBF5462	SST5462	
MMBF5463	SST5463	
MMBF5484	SST5484	
MMBF5485	SST5485	
MMBF5486	SST5486	
MMT3823	2N4222	
MPF10LM		VN10LM
MPF102		J304
MPF103		J202
MPF104		J202
MPF105		J203
MPF106	2N5485	
MPF107	2N5486	
MPF108		J304
MPF109		J304
MPF110	2N3819	
MPF111		J304
MPF112		J304
MPF203	J310	
MPF4150		VN1706L
MPF4391	PN4391-18	
MPF4392	PN4392-18	
MPF4393	PN4393-18	
MPF6660		2N6660
MPF6661		2N6661
MPF820	J212	
MPF910		VN10LM
MPF9200		VN2406L
MPF9200		VN2406L
MPF970	J174	
MPF971	J176	
M163	3N163	
M164	3N164	
M440	M440	
M441	M441	
M5911	M5911	
M5912	M5912	
ND2012L	ND2012L	

Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
ND2020E	ND2020E	
ND2020L	ND2020L	
ND2406L	ND2406L	
ND2410B	ND2410B	
ND2410L	ND2410L	
NF3819		J212–188
NF4302	2N4302	
NF4303	2N4303	
NF4304	2N4304	
NF4445	2N5432	
NF4446	2N5433	
NF4447	2N5432	
NF4448	2N5433	
NF500	2N4416	
NF501	2N4416	
NF506	2N4416	
NF510	2N4393	
NF5102	J230	
NF511	2N4393	
NF5163	2N5163	
NF520	2N4339	
NF521	2N4339	
NF522	2N4339	
NF523	2N4340	
NF530	2N4341	
NF531	2N4339	
NF532	2N4341	
NF533	2N4339	
NF5457	J202	
NF5458	J202	
NF5459	J20359	
NF5484	2N5484	
NF5485	2N5485	
NF5486	2N5486	
NF550		2N5566
NF5555	2N5555	
NF5638	2N5638	
NF5639	2N5639	
NF5640	2N5640	
NF5653	2N5653	
NF5654	2N5654	
NF580	2N5432	
NF581	2N5432	
NF582	2N5433	
NF583	2N5434	
NF584	2N5433	
NF585	2N4859	
NOS100B		ND2410B
NOS101B		ND2410B
NOS102B		ND2410B
NPC108	J304	
NPC108A	J304	
PMBF4391	SST4391	
PMBF4392	SST4392	
PMBF4393	SST4393	
PN4091	PN4091	
PN4092	PN4092	
PN4093	PN4093	
PN4117	PN4117	
PN4117A	PN4117A	
PN4118	PN4118	
PN4118A	PN4118A	
PN4119	PN4119	
PN4119A	PN4119A	
PN4120	PN4120	
PN4120A	PN4120A	
PN4220		PN4302
PN4221		PN4303
PN4222		PN4304
PN4302	PN4302	
PN4302–18	PN4302–18	
PN4303	PN4303	
PN4303–18	PN4303–18	
PN4304	PN4304	
PN4304–18	PN4304–18	

Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
PN4391	PN4391	
PN4391–18	PN4391–18	
PN4392	PN4392	
PN4392–18	PN4392–18	
PN4393	PN4393	
PN4393–18	PN4393–18	
PN4416	PN4416	
PN4856		2N4856
PN4857		2N4857
PN4858		2N4858
PN4859		2N4859
PN4860		2N4860
PN4861		2N4861
PN5114		2N5114
PN5115		2N5115
PN5116		2N5116
PN5432		2N5432
PN5433		2N5433
PN5434		2N5434
P1086	P1086	
P1086–18	P1086–18	
P1086E	P1086	
P1087	P1087	
P1087E	P1087	
SDF1001		J108
SDF1002		J109
SDF1003		J110
SDF500		2N5196
SDF501		2N5197
SDF502		2N3956
SDF503		2N3957
SDF504		2N3958
SDF505		2N5196
SDF506		2N5197
SDF507		2N3956
SDF508		2N3957
SDF509		2N3958
SDF510		2N5196
SDF511		2N5197
SDF512		2N3956
SDF513		2N3957
SDF514		2N3958
SD210DE	SD210DE	
SD210EE	SD210DE	
SD2100	SD2100	
SD211DE	SD211DE	
SD211EE	SD211DE	
SD212DE	SD212DE	
SD212EE	SD212DE	
SD213DE	SD213DE	
SD213EE	SD213DE	
SD214DE	SD214DE	
SD214EE	SD214DE	
SD215DE	SD215DE	
SD5000I	SD5000I	
SD5000J	SD5000N	
SD5000N	SD5000N	
SD5001I	SD5001I	
SD5001J	SD5001N	
SD5001N	SD5001N	
SD5002I	SD5002I	
SD5002J	SD5002N	
SD5002N	SD5002N	
SD5200I		SD5000I
SD5200N		SD5000N
SD5400CY	SD5400CY	
SD5401CY	SD5401CY	
SD5402CY	SD5402CY	
SI8901A	SI8901A	
SI8901Y	SI8901Y	
SK3112		J231
SK3746/326		J305
SK3834/132		J211
SK3977/456		2N4421
SK9072/452		2N4416

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Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
SK9148/461		2N5199
SK9160/462		2N4869
SK9161/457		J305
SK9162/467		2N4391
SK9163/466		2N4991
SK9460/458		J230
SO4391	SST4391	
SO4392	SST4392	
SO4393	SST4393	
SO4416	SST4416	
SSTDPAD100	SSTDPAD100	
SSTDPAD20	SSTDPAD20	
SSTDPAD5	SSTDPAD5	
SSTDPAD50	SSTDPAD50	
SST108	SST108	
SST109	SST109	
SST110	SST110	
SST111	SST111	
SST112	SST112	
SST113	SST113	
SST174	SST174	
SST175	SST175	
SST176	SST176	
SST177	SST177	
SST201	SST201	
SST202	SST202	
SST203	SST203	
SST204	SST204	
SST211	SST211	
SST213	SST213	
SST215	SST215	
SST270	SST270	
SST271	SST271	
SST308	SST308	
SST309	SST309	
SST310	SST310	
SST404	SST404	
SST405	SST405	
SST406	SST406	
SST4091	SST4091	
SST4092	SST4092	
SST4093	SST4093	
SST4338	SST4338	
SST4339	SST4339	
SST4340	SST4340	
SST4341	SST4341	
SST440	SST440	
SST441	SST441	
SST4416	SST4416	
SST4856	SST4856	
SST4857	SST4857	
SST4858	SST4858	
SST4859	SST4859	
SST4860	SST4860	
SST4861	SST4861	
SST5460	SST5460	
SST5461	SST5461	
SST5462	SST5462	
SST5463	SST5463	
SST5464	SST5464	
SST5465	SST5465	
SST5484	SST5484	
SST5485	SST5485	
SST5486	SST5486	
SST5912	SST5912	
SST6908	SST6908	
SST6909	SST6909	
SST6910	SST6910	
SST6911		SST6908
SU2098	2N5197	
SU2098B	2N5196	
TD5902	U421	
TD5903	U422	
TD5904	U423	
TD5905	U421	
TD5906	U422	
TD5907	U424	
TD5908	U425	
TD5909	U426	
THJJ105	J105CHP	
THJJ106	J106CHP	
THJJ107	J107CHP	
THJJ108	J108CHP	
THJJ109	J109CHP	
THJJ110	J110CHP	
THJJ111	J111CHP	
THJJ111A	J111ACHP	
THJJ112	J112CHP	
THJJ112A	J112ACHP	
THJJ113	J113CHP	
THJJ113A	J113ACHP	
THJJ174	J174CHP	
THJJ175	J175CHP	
THJJ176	J176CHP	
THJJ177	J177CHP	
THJJ201	J201CHP	
THJJ202	J202CHP	
THJJ203	J203CHP	
THJJ210	J210CHP	
THJJ211	J211CHP	
THJJ212	J212CHP	
THJJ230	J230CHP	
THJJ231	J231CHP	
THJJ232	J232CHP	
THJJ270	J270CHP	
THJJ271	J271CHP	
THJJ300A		J212CHP
THJJ300B		J210CHP
THJJ300C		J211CHP
THJJ304	J304CHP	
THJJ305	J305CHP	
THJJ308	J308CHP	
THJJ309	J309CHP	
THJJ310	J310CHP	
THJP1086	P1086CHP	
THJP1087	P1087CHP	
THJU290	U290CHP	
THJU291	U291CHP	
THJU304	U304CHP	
THJU305	U305CHP	
THJU306	U306CHP	
THJU308	U308CHP	
THJU309	U309CHP	
THJU310	U310CHP	
THJU401	U401CHP	
THJU402	U402CHP	
THJU403	U403CHP	
THJU404	U404CHP	
THJU405	U405CHP	
THJU406	U406CHP	
THJ4091	2N4091CHP	
THJ4092	2N4092CHP	
THJ4093	2N4093CHP	
THJ4117	2N4117CHP	
THJ4118	2N4118CHP	
THJ4119	2N4119CHP	
THJ4220	2N4220CHP	
THJ4221	2N4221CHP	
THJ4222	2N4222CHP	
THJ4223		2N4222CHP
THJ4224		2N4222CHP
THJ4292	2N4392CHP	
THJ4293	2N4393CHP	
THJ4338	2N4338CHP	
THJ4339	2N4339CHP	
THJ4340	2N4340CHP	
THJ4341	2N4341CHP	
THJ4391	2N4391CHP	
THJ4416	2N4416CHP	
THJ4416A	2N4416ACHP	

Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
THJ4856	2N4856CHP	
THJ4856A	2N4856ACHP	
THJ4857	2N4857CHP	
THJ4857A	2N4857ACHP	
THJ4858	2N4858CHP	
THJ4858A	2N4858ACHP	
THJ4859	2N4859CHP	
THJ4859A	2N4859ACHP	
THJ4860	2N4860CHP	
THJ4860A	2N4860ACHP	
THJ4861	2N4861CHP	
THJ4861A	2N4861ACHP	
THJ4867	2N4767CHP	
THJ4868	2N4868CHP	
THJ4869	2N4869CHP	
THJ5018	2N5114CHP	
THJ5019	2N5114CHP	
THJ5046	2N5196CHP	
THJ5047	2N5199CHP	
THJ5114	2N5114CHP	
THJ5115	2N5115CHP	
THJ5116	2N5116CHP	
THJ5199	2N5199CHP	
THJ5432	2N5432CHP	
THJ5433	2N5433CHP	
THJ5434	2N5434CHP	
THJ5457	J202CHP	
THJ5458	J202CHP	
THJ5459	J203CHP	
THJ5484	2N5484CHP	
THJ5485	2N5485CHP	
THJ5486	2N5486CHP	
THJ5638	2N5638CHP	
THJ5639	2N5639CHP	
THJ5640	2N5640CHP	
THJ5911	2N5911CHP	
THJ5912	2N5912CHP	
TIS14	2N4416	
TIS88A	2N4416A	
TMF5911	2N5911CHP	
TMF5912	2N5912CHP	
TMPFJ111	SST111	
TMPFJ112	SST112	
TMPFJ113	SST113	
TMPFJ174	SST174	
TMPFJ175	SST175	
TMPFJ176	SST176	
TMPFJ177	SST177	
TMPFJ201	SST201	
TMPFJ202	SST202	
TMPFJ203	SST203	
TMPFJ210	SST210	
TMPFJ211	SST211	
TMPFJ212	SST212	
TMPFJ270	SST270	
TMPFJ271	SST271	
TMPFJ300		SST212
TMPFJ304	SST304	
TMPFJ305	SST305	
TMPFJ308	SST308	
TMPFJ309	SST309	
TMPFJ310	SST310	
TMPFU304	SST304	
TMPFU310	SST310	
TMPF3819	SST4416	
TMPF3820		SST270
TMPF4091	SST4856	
TMPF4092	SST4857	
TMPF4093		SST4856
TMPF4338		SST201
TMPF4339		SST204
TMPF4340		SST202
TMPF4341		SST203
TMPF4391	SST4391	
TMPF4392	SST4392	

Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
TMPF4393	SST4393	
TMPF4416	SST4416	
TMPF4416	SST4416	
TMPF4416A		SST4416
TMPF4856	SST4856	
TMPF4856A	SST4856A	
TMPF4857	SST4857	
TMPF4857A	SST4857A	
TMPF4858	SST4848	
TMPF4858A	SST4848A	
TMPF4859	SST4859	
TMPF4859A	SST4859A	
TMPF4860	SST4860	
TMPF4860A	SST4860A	
TMPF4861	SST4861	
TMPF4861A	SST4861A	
TMPF5114	SST5114	
TMPF5115	SST5115	
TMPF5116	SST5116	
TMPF5457	SST5457	
TMPF5458	SST5458	
TMPF5459	SST5459	
TMPF5460	SST5460	
TMPF5461	SST5461	
TMPF5462	SST5462	
TMPF5484	SST5484	
TMPF5485	SST5485	
TMPF5486	SST5486	
TNO1O2N2		VN0300B
TNO1O2N3		VN0300L
TNO520N2		VN2406B
TNO520N3		VN2410L
TN0524N3		VN2410L
TN4117A	2N4117A	
TN4118A	2N4118A	
TP0610E	TP0610E	
TP0610L	TP0610L	
TP0610T	TP0610T	
UCX1702		3N164
UC155		U309
UC155E		J309
UC155W		J309
UC1700		3N163
UC210		2N4416
UC2130		2N5196
UC240	2N4869	
UC241		2N4221
UC250		2N4091
UC251	2N4392	
UC452		2N4392
UC588		PN4416
UC703		2N4221
UC705		U310
UC707		2N4856
UC714		2N4222
UC755		2N4341
UC756		2N4341
UC758		J202
U1177	2N4220A	
U1325	2N4222	
U183	2N4416	
U1837	U1837	
U1837-18	U1837-18	
U1837E	U1837	
U184	2N4416	
U1897	U1897	
U1897-18	U1897-18	
U1897E	U1897-18	
U1898	U1898	
U1898-18	U1898-18	
U1898E	U1898-18	
U1899	U1899	
U1899-18	U1899-18	
U1899E	U1899-18	
U197	2N4338	

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Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
U198	2N4340	
U199		2N4341
U1994		J304
U1994E		J304-18
U200		2N4393
U201		2N4392
U202		2N4391
U2047E	PN4416-18	
U2134		2N5199
U231	2N5197	
U232	2N5198	
U233	2N5199	
U234	2N5199	
U235	2N5199	
U240	2N5432	
U241	2N5433	
U242	2N5432	
U243	2N5433	
U248	U42402	
U249	U424	
U250	U425	
U251	U426	
U257	M5912	
U280		2N5197
U281		2N5197
U282		2N5198
U283		2N5198
U284		2N5199
U285		2N5199
U290	U290	
U291	U291	
U295		U290
U296		U291
U300		2N5114
U3000	2N4341	
U3001	2N4339	
U3002	2N4338	
U301		2N5115
U3010	2N4341	
U3011	2N4340	
U3012	2N4338	
U304	2N5114	
U305	2N5115	
U306	2N5116	
U308	U308	
U309	U309	
U310	U310	
U311	U310	
U312		U309
U320		2N5432
U321		2N5434
U322		2N5432
U350	U350	
U401	U401	
U402	U402	
U403	U403	
U404	U404	
U405	U405	
U406	U406	
U410	U410	
U411	U411	
U412	U412	
U421	U421	
U422	U422	
U423	U423	
U424	U424	
U425	U425	
U426	U426	
U427	U427	
U428	U428	
U430	U430	
U431	U431	
U440	U440	
U441	U441	
U443	U443	

Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
U444	U444	
U508	CRR0240	
VCR2N	VCR2N	
VCR3P	VCR3P	
VCR4N	VCR4N	
VCR5P	VCR3P	
VCR7N	VCR7N	
VN0104N5	VN66AD	
VN0104N6		VQ1004J
VN0104N7		VQ1004P
VN0106N5	VN66AD	
VN0106N6		VQ1004J
VN0106N7		VQ1004P
VN0106N9		VN10LE
VN0116N2		VN1706B
VN0116N3		VN1710L
VN0116N5	VN1706D	
VN0120N2		VN2406B
VN0120N3		VN2410L
VN0120N5	VN2406D	
VN0216N2		VN1706B
VN0216N3		VN1706L
VN0216N5		VN1706D
VN0220N2		VN2406B
VN0220N3		VN2406L
VN0220N5		VN2406D
VN0300B	VN0300B	
VN0300D	VN0300D	
VN0300L	VN0300L	
VN0300M	VN0300M	
VN0350N3		VN3515L
VN0535N2		VN4012B
VN0535N3		VN3515L
VN0540N2		VN4012B
VN0540N3		VN4012L
VN0603L	VN0603L	
VN0603L	VN0603L	
VN0603T	VN0603T	
VN0606L	VN0606L	
VN0606M	VN0606M	
VN0606T	VN0605T	
VN0610L	VN0610L	
VN0610LL	VN0610LL	
VN0808L	VN0808L	
VN0808M	VN0808M	
VN10KE	VN10KE	
VN10KM	VN10KM	
VN10KMA	VN10KM	
VN10KN3		VN10LM
VN10KN9		VN10LE
VN10LE	VN10LE	
VN10LM	VN10LM	
VN1008L	VN1008L	
VN1206B	VN1206B	
VN1206D	VN1206D	
VN1206L	VN1206L	
VN1206M	VN1206M	
VN1210L	VN1210L	
VN1210M	VN1210M	
VN1304N2		VN1206B
VN1304N3		VN1206L
VN1304N6		VQ1004J
VN1304N7		VQ1004P
VN1306N2		VN1206B
VN1306N3		VN1206L
VN1306N6		VQ1004J
VN1306N7		VQ1004P
VN1310N2		VN1206B
VN1310N3		VN1206L
VN1316N2		VN4012B
VN1316N3		BS107
VN1320N2		VN4012B
VN1320N3		BS107
VN1706B	VN1706B	
VN1706D	VN1706D	

Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
VN1706L	VN1706L	
VN1706M	VN1706M	
VN1710L	VN1710L	
VN1710M	VN1710M	
VN2010L	VN2010L	
VN2020L	VN2020L	
VN2222KM	VN2222KM	
VN2222L	VN2222L	
VN2222LL	VN2222LL	
VN2222LM	VN2222LM	
VN2406B	VN2406B	
VN2406D	VN2406D	
VN2406L	VN2406L	
VN2406M	VN2406M	
VN2410L	VN2410L	
VN2410M	VN2410M	
VN30AB		VN35AB
VN35AB	VN35AB	
VN35AK	VN35AB	
VN3515L	VN3515L	
VN40AD	VN40AD	
VN40AF		VN40AFD
VN4010B		VN4012B
VN4010L		VN4012L
VN4012B	VN4012B	
VN4012L	VN4012L	
VN46AD	VN46AD	
VN46AF		VN46AFD
VN50300L	VN50300L	
VN50300T	VN50300T	
VN66AD	VN66AD	
VN66AF		VN66AFD
VN67AA		VN67AB
VN67AB	VN67AB	
VN67AD	VN67AD	
VN67AF		VN67AFD
VN67AK		VN67AB
VN80AF		VN80AFD
VN88AD	VN88AD	
VN88AF		VN88AFD
VN89AA		VN99AB
VN89AB	VN99AB	
VN89AD	VN89AD	
VN89AF		VN89AFD
VN90AA		VN90AB
VN90AB	VN90AB	
VN98AJ		VN99AB
VN98AK	2N6661	
VN99AB	VN99AB	
VN99AK		VN99AB
VP0104N3		TP0610L
VP0104N6		VQ2004J
VP0104N9		TP0610E
VP0106N3		TP0610L
VP0106N9		TP0610E
VP0116N2		VP2020B
VP0116N3		VP2020L
VP0120N2		VP2020B
VP0120N3		VP2020L
VP0204N2	VP0808B	
VP0300B	VP0300B	
VP0300L	VP0300L	
VP0300M	VP0300M	
VP0610E	VP0610E	
VP0610L	VP0610L	
VP0610T	VP0610T	
VP0808B	VP0808B	
VP0808L	VP0808L	
VP0808M	VP0808M	
VP1008B	VP1008B	
VP1008L	VP1008L	
VP1008M	VP1008M	
VP2020E	VP2020E	
VP2020L	VP2020L	
VP2410B	VP2410B	
VP2410L	VP2410L	
VQ1000CJ	VQ1000J	
VQ1000CP	VQ1000P	
VQ1000J	VQ1000J	
VQ1000N6	VQ1000J	
VQ1000N7	VQ1000P	
VQ1000P	VQ1000P	
VQ1000P-7	VQ1000P-7	
VQ1000P/883	VQ1000P-7	
VQ1001G	VQ1001P	
VQ1001J	VQ1001J	
VQ1001P	VQ1001P	
VQ1004J	VQ1004J	
VQ1004P	VQ1004P	
VQ1006J	VQ1006J	
VQ1006P	VQ1006P	
VQ2000J	VQ2000J	
VQ2000P	VQ2000P	
VQ2001G	VQ2001P	
VQ2001J	VQ2001J	
VQ2001P	VQ2001P	
VQ2004J	VQ2004J	
VQ2004P	VQ2004P	
VQ2006J	VQ2006J	
VQ2006P	VQ2006P	
VQ3001G	VQ3001P	
VQ3001J	VQ3001J	
VQ3001N6	VQ3001J	
VQ3001N7	VQ3001P	
VQ3001P	VQ3001P	
VQ7254J	VQ7254J	
VQ7254N6	VQ7254J	
VQ7254N7	VQ7254P	
VQ7254P	VQ7254P	
VQ7254P-7	VQ7254P-7	
VQ7254P/883	VQ7254P-7	
ZVN01A2A	VN0300L	
ZVN01A2L	VN0300L	
ZVN0102A	VN0300L	
ZVN0102B	VN0300B	
ZVN0102L	VN0300L	
ZVN0104B	VN67AB	
ZVN0104L	VN46AD	
ZVN0106L	VN66AD	
ZVN0108L	VN88AD	
ZVN0109B	2N6661	
ZVN0109L		VN88AD
ZVN0110A	VN1206L	
ZVN0110B	VN1206B	
ZVN0110L	VN1206D	
ZVN0114A	VN1706L	
ZVN0116A	VN1706L	
ZVN0116B	VN1706B	
ZVN0117TA	VN1710L	
ZVN0120A	VN2410L	
ZVN0120A	VN2410L	
ZVN1304A	VN2222L	
ZVN1304B	VN67AB	
ZVN1306A	VN0610L	
ZVN1306B	VN67AB	
ZVN1308A	VN1210L	
ZVN1308B	VN1210B	
ZVN1309A	VN2410L	
ZVN1310A	VN2406L	
ZVN1314A	VN2410L	
ZVN1316A	VN2410L	
ZVN1320A	VN2410L	
ZVN1404A	VN0610L	
ZVN1404B	VN67AB	
ZVN1406A	VN0610L	
ZVN1406B	VN67AB	
ZVN1408A	VN2410L	
ZVN1409A	VN2410L	
ZVN1414A	VN2410L	
ZVN1416A	VN2410L	

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Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
ZVN1420A	VN2020L	
ZVN2115A	VN1710L	
ZVN2115B	VN1710B	
ZVN3302A	VN0300L	
ZVN3302B	VN0300B	
ZVN3304A	VN1206L	
ZVN3304B	VN1206B	
ZVN3306B		VN1206B
ZVN3310A		VN1206L
ZVN530A	VN3515L	
ZVN535A	VN3515L	
ZVN540A	VN4012L	
ZVP0120A		BSS92
ZVP1306A		TP0610L
ZVP1306B		TP0610B
ZVP1308A		BSS92
ZVP1320A		BSS92
ZVP1408B	VP0808B	
ZVP1409B	VP1008B	
ZVP1410B	VP1008B	
ZVP3306A		TP0610L
1N5283		CRO22
1N5284		CR024
1N5285		CR027
1N5286		CR030
1N5287		CR033
1N5288		CR039
1N5289		CR043
1N5290		CR047
1N5291		CR056
1N5292		CR062
1N5293		CR068
1N5294		CR075
1N5295		CR082
1N5296		CR091
1N5297		CR100
1N5298		CR110
1N5299		CR120
1N5300		CR130
1N5301		CR140
1N5302		CR150
1N5303		CR160
1N5304		CR180
1N5305		CR200
1N5306		CR220
1N5307		CR240
1N5308		CR270
1N5309		CR300
1N5310		CR330
1N5311		CR360
1N5312		CR390
1N5313		CR430
1N5314		CR470
2N2386		J270
2N2386A		J270
2N2497		J270
2N2498		J270
2N2499		J270
2N2500		J270
2N2606		J176
2N2607		J176
2N2841		J270
2N2842		J270
2N2843		J270
2N2844		J270
2N3066	2N4340	
2N3067	2N4338	
2N3068	2N4338	
2N3069	2N4341	
2N3070	2N4339	
2N3071	2N4338	
2N3084	2N4340	
2N3085	2N4340	
2N3086	2N4340	
2N3087	2N4340	

Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
2N3088	2N4338	
2N3088A	2N4338	
2N3089	2N4338	
2N3089A	2N4338	
2N3112		J270
2N3277		J276
2N3278		J276
2N3328		J176
2N3329		J176
2N3330		J176
2N3331		J176
2N3332		J176
2N3365	2N4340	
2N3366	2N4338	
2N3367	2N4338	
2N3368	2N4341	
2N3369	2N4339	
2N3370	2N4340	
2N3376		J201
2N3378		J270
2N3380		J176
2N3382		J176
2N3384		J175
2N3386	2N5116	
2N3436	2N4341	
2N3437	2N4340	
2N3438	2N4338	
2N3452	2N4340	
2N3453	2N4338	
2N3454		J201
2N3455	2N4340	
2N3456	2N4338	
2N3457	2N4338	
2N3458	2N4341	
2N3466		2N4220
2N3684		2N4221
2N3684A		2N4221
2N3685		2N4220
2N3685A		2N4220
2N3686		2N4220
2N3686A		2N4220
2N3819	2N3819	
2N3819-18	2N3819-18	
2N3820	J270	
2N3821	2N4220	
2N3822	2N4221	
2N3823	2N4222	
2N3824	2N4220	
2N3909	2N3909	
2N3909A	2N3909A	
2N3921		U401
2N3922		U402
2N3954		2N5196
2N3954A		2N5194
2N3955		2N5197
2N3955A	2N3955A	
2N3956	2N3956	
2N3957	2N3957	
2N3958	2N3958	
2N3966		2N4416
2N3967	2N4221	
2N3967A	2N4221	
2N3968	2N4340	
2N3968A	2N4340	
2N3969	2N4339	
2N3969A	2N4339	
2N3970	2N4391	
2N3971	2N4391	
2N3972	2N4393	
2N3993	2N5116	
2N4084		U402
2N4085		U404
2N4091	2N4091	
2N4091A	2N4091	
2N4092	2N4092	

Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
2N4092A	2N4092	
2N4093	2N4093	
2N4093A	2N4093	
2N4094	2N4856	
2N4095	2N4857	
2N4117	2N4117	
2N4117A	2N4117A	
2N4118	2N4118	
2N4118A	2N4118A	
2N4119	2N4119	
2N4119A	2N4119A	
2N4120	3N163	
2N4220	2N4220	
2N4220A	2N4220A	
2N4221	2N4221	
2N4221A	2N4221A	
2N4222	2N4222	
2N4222A	2N4222A	
2N4223		2N4222
2N4223A		2N4222
2N4224		2N4222
2N4224A		2N4222
2N4267	3N163	
2N4302	PN4302-18	
2N4303	PN4303-18	
2N4304	PN4304-18	
2N4338	2N4338	
2N4339	2N4339	
2N4340	2N4340	
2N4341	2N4341	
2N4391	2N4391	
2N4392	2N4392	
2N4393	2N4393	
2N4416	2N4416	
2N4416A	2N4416A	
2N4417		SST4416
2N4445	2N5432	
2N4446	2N5433	
2N4447	2N5432	
2N4448	2N5432	
2N4856	2N4856	
2N4856A	2N4856A	
2N4857	2N4857	
2N4857A	2N4857A	
2N4858	2N4858	
2N4858A	2N4858A	
2N4859	2N4859	
2N4859A	2N4859A	
2N4860	2N4860	
2N4860A	2N4860A	
2N4861	2N4861	
2N4861A	2N4861A	
2N4867	2N4867	
2N4867A	2N4867A	
2N4868	2N4868	
2N4868A	2N4868A	
2N4869	2N4869	
2N4869A	2N4869A	
2N4977	2N5432	
2N4978	2N5433	
2N4979	2N5434	
2N5018		2N5114
2N5019	2N5116	
2N5045	2N5196	
2N5046	2N5198	
2N5047	2N5199	
2N5078		J211
2N5103	2N4416	
2N5104	2N4416	
2N5105	2N4416	
2N5114	2N5114	
2N5115	2N5115	
2N5116	2N5116	
2N5158	2N5434	
2N5159	2N5433	

Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
2N5163	JII3-18	
2N5196	2N5196	
2N5197	2N5197	
2N5198	2N5198	
2N5199	2N5199	
2N5245	J304-18	
2N5246	J305-18	
2N5247	MPF109-18	
2N5248	2N5486	
2N5257	J202	
2N5258	J202	
2N5259	J202	
2N5358		2N4339
2N5359		2N4339
2N5360	2N4340	
2N5361		2N4341
2N5362		2N4341
2N5363	2N4222A	
2N5364		2N4222
2N5391	2N4867A	
2N5392	2N4868A	
2N5393	2N4869A	
2N5394	2N4869A	
2N5395	2N4869A	
2N5396	2N4869A	
2N5397	U310	
2N5398		J212
2N5432	2N5432	
2N5433	2N5433	
2N5434	2N5434	
2N5452		2N5196
2N5453		2N5198
2N5454		2N5199
2N5456		2N4340
2N5457	J202	
2N5458	J202	
2N5459	J203	
2N5460	2N4560	
2N5461	2N5461	
2N5462	2N5462	
2N5463	2N5463	
2N5464	2N5464	
2N5465	2N5465	
2N5484	2N5484	
2N5485	2N5485	
2N5486	2N5486	
2N5515		2N5196
2N5516		2N5197
2N5517		2N5198
2N5518		2N5199
2N5519		2N5199
2N5520		2N5196
2N5521		2N5197
2N5522		2N5198
2N5523		2N5199
2N5524		2N5199
2N5543		2N5197
2N5544		2N5197
2N5545		2N5199
2N5546		2N5198
2N5547		2N5199
2N5549		2N4392
2N5556	2N4339	
2N5557		2N4340
2N5558		2N4341
2N5561	U401	
2N5562	U402	
2N5563	U404	
2N5564	DN5564	
2N5564	2N5564	
2N5565	DN5565	
2N5565	2N5565	
2N5566	DN5566	
2N5566	2N5566	
2N5567	DN5567	

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Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
2N5592	2N4341	
2N5593	2N4341	
2N5594	2N4341	
2N5638	2N5638	
2N5638-18	2N5638-18	
2N5639	2N5639	
2N5639-18	2N5639-18	
2N5640	2N5640	
2N5640-18	2N5640-18	
2N5647	2N4117A	
2N5648	2N4117A	
2N5649	2N4117A	
2N5653	J112	
2N5654		J111
2N5668		MPF108
2N5669		MPF108
2N5670		MPF108
2N5902		U404
2N5903		U424
2N5904		U425
2N5905		U426
2N5906		U421
2N5907		U421
2N5908		U421
2N5909		U423
2N5911	2N5911	
2N5912	2N5912	
2N5949	U1837-18	
2N5950	U1837-18	
2N5951	U1837-18	
2N5952	J305-18	
2N5953	J305-18	
2N6451	2N4393	
2N6452	2N4393	
2N6453	2N4393	
2N6454	2N4393	
2N6483	U401	
2N6484	U402	
2N6485	U404	
2N6659	2N6659	
2N6659/750	2N6659-5	
2N6660	2N6660	
2N6660/750	2N6660-5	
2N6661	2N6661	
2N6661/750	2N6661-5	
2N6661JAN	2N6661JAN	
2N6661JANTX	2N6661JANTX	
2N6661JANTXV	2N6661JANTXV	
2N6905	2N6905	
2N6905A	2N6905A	
2N6906	2N6906	
2N6906A	2N6906A	
2N6907	2N6907	
2N6907A	2N6907A	
2N6908	2N6908	
2N6909	2N6909	
2N6910	2N6910	
2N6911		2N6908
2N7000	2N7000	
2N7001	2N7001	
2N7002	2N7002	
2N7003		VN50300T
2N7007	2N7007	
2N7008	2N7008	
2N7009		VN50300L
2N7019		VP0610T
2N7019	VP0610T	
2N7020	ND2020E	
2N7022	VN4012B	
2N7023	VP2020E	
2N7024	ND2410B	
2N7025	TP0610L	
2N7026	TP0610T	
2N7027	TP0610E	
2N7030	VP2410B	

Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
2N7104	2N7104	
2N7105	2N7105	
2N7106	2N7106	
2N7107	2N7107	
2N7108	2N7108	
2N7109	2N7109	
2N7116	2N7116	
2N7117	2N7117	
2SK103		SST201
2SK104E		PN4302
2SK104F		PN4302F
2SK104H		PN4302
2SK104J		PN4303
2SK105E		2N4220
2SK105F		2N4220
2SK105H		2N4221
2SK105J		2N4221
2SK107		J304
2SK108		PN4392
2SK109		U406
2SK11	2N4220	
2SK113		2N4393
2SK117		2N4341
2SK118		2N4340
2SK119		2N4340
2SK12		2N4220A
2SK120		2N5484
2SK121		J210
2SK123		SST201
2SK125		J310
2SK127		2N4221
2SK128		J232
2SK13		2N4340
2SK136		J232
2SK141		2N4221
2SK148		2N5485
2SK149		J309
2SK15		2N4220A
2SK150		U405
2SK154		2N5485
2SK155		J309
2SK156A		PN4118
2SK156B		PN4119
2SK156C		PN4119
2SK157		SST202
2SK158		2N4340
2SK16H		2N4221
2SK16HA		2N4220
2SK16HB		2N4221
2SK16HC		2N4221
2SK160		SST202
2SK161		2N5485
2SK163		J113
2SK165		J309
2SK168D		2N5485
2SK168E		J304
2SK168F		2N5486
2SK17		J230
2SK18		2N3958
2SK18A		2N3958
2SK184		2N4221
2SK185		2N5566
2SK186		J232
2SK19BL		J309
2SK19GR		J304
2SK19Y		2N5485
2SK192ABL		2N5486
2SK192AGR		2N5484
2SK192AY		2N5484
2SK193EF		2N5484
2SK193FF		2N5484
2SK193KF		2N5484
2SK193LF		2N5484
2SK193MF		2N5485
2SK193PF		2N5484

Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
2SK193UF		J201
2SK195E		2N5484
2SK195F		2N5484
2SK195H		2N5484
2SK195J		2N5485
2SK197C		SST202
2SK197D		SST4416
2SK197E		SST4416
2SK198		2N4221
2SK199		2N5485
2SK208		SST202
2SK209		SST4416
2SK210BL		SST309
2SK210GR		SST4416
2SK210Y		SST4416
2SK211		SST4416
2SK212C		2N5484
2SK212D		2N5484
2SK212E		2N5484
2SK212F		2N5484
2SK217C		SST202
2SK217D		SST4416
2SK217E		SST4416
2SK222		J232
2SK23A-8		2N5485
2SK23A-9		2N4416A
2SK238K14		SST202
2SK238K15		SST202
2SK238K16		SST4416
2SK238K17		SST4416
2SK24		J203
2SK242C		SST202
2SK242D		SST202
2SK242E		SST4416
2SK242F		SST4416
2SK246BL		2N4221
2SK246GR		2N4221
2SK247P		J230
2SK247Q		J230
2SK247R		J231
2SK247S		J232
2SK25		2N5486
2SK266		PN4119A
2SK270		U405
2SK292		2N5484
2SK30		J210
2SK30AGR		2N4341
2SK30AO		2N4339
2SK30AR		2N4338
2SK30ATM		J211
2SK30AY		2N4340
2SK301P		J230
2SK301Q		J231
2SK301R		J232
2SK301S		J203
2SK303C		SST204
2SK303D		SST204
2SK303E		SST202
2SK303F		SST203
2SK314		2N4416A
2SK315E		2N5484
2SK315F		2N5485
2SK315G		J211
2SK323		SST203
2SK33		J304
2SK330BL		J203
2SK330GR		J202
2SK330Y		J202
2SK331		SST201
2SK334		SST201
2SK34	PN4302	
2SK35		J210
2SK362		U1899
2SK363		U1897
2SK364		U1898
2SK365		U1899
2SK366		U1898
2SK369		U1898
2SK37		2N5484
2SK370		J109
2SK372		U1897
2SK374		2N4341
2SK376		PN4119
2SK377		SST201
2SK381		JII3
2SK389		SST405
2SK39		PN4119
2SK39A		PN4119
2SK40		2N4339
2SK40B		2N4339
2SK40C		2N4340
2SK40D		J231
2SK404		2N5485
2SK41		2N5486
2SK41C		2N5484
2SK41D		2N5484
2SK41E		2N5484
2SK41F		2N5485
2SK42		2N5484
2SK422		VN67AB
2SK425		SST4416
2SK426		SST4416
2SK43		J232
2SK43S		J113
2SK43S-D		J113
2SK44		J230
2SK45		2N4220A
2SK46		J230
2SK47		2N5484
2SK48	2N4220	
2SK49		2N5484
2SK49E		2N5484
2SK49F		2N5484
2SK49H		2N5484
2SK507		J308
2SK508		SST308
2SK54		2N5484
2SK54B		2N5484
2SK54C		2N5484
2SK55		2N5485
2SK55D		2N5485
2SK55E		2N5485
2SK56		2N5484
2SK57		2N5484
2SK58		U441
2SK59		2N4867
2SK61		2N5484
2SK65		J201
2SK66		J231
2SK67		SST201
2SK67A		SST201
2SK68		2N4221
2SK68A		2N4221
2SK72		2N5158
2SK83		2N5484
2SK84		J231
2SK93		PN4119
2SK94		SST202
2SK97		SST406
3N163	3N163	
3N164	3N164	

This Cross Reference material is accurate to the best knowledge and belief of Siliconix incorporated. Since individual circuit design and layout can influence device performance, the purchaser must be responsible for the ultimate selection and determination of interchangeability.

SELECTOR GUIDE

INTRODUCTION

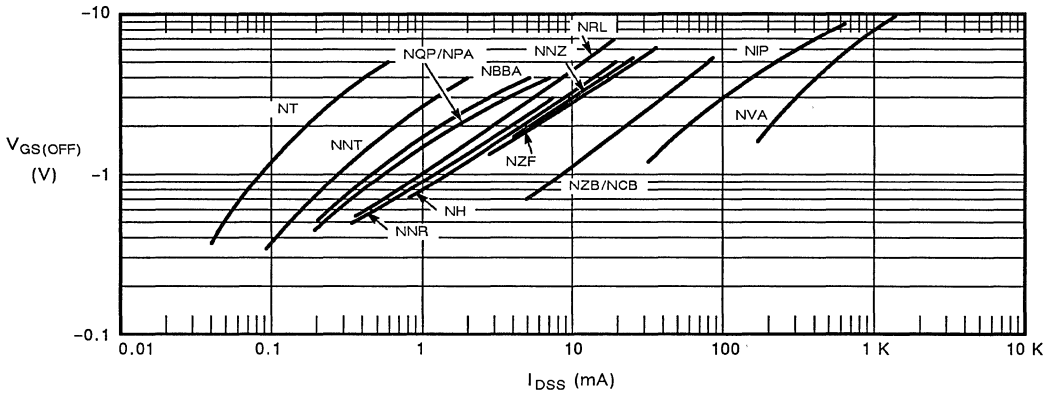
Low Power Discrete selector guides have been provided to assist design engineers in a number of ways. With their help selecting the proper JFET or MOSFET can be reduced to a minimum.

First, curve and bar graphs have been constructed to allow you to rapidly gain an understanding of how our geometries have been characterized to provide a wide range of design alternatives. Once a geometry which has the desired characteristics has been identified, you can then turn to the typical performance curves (section 7). Here a more detailed curve set and a list of representative part numbers is provided. Turning to the appropriate data sheet and confirming specifications completes the selection process.

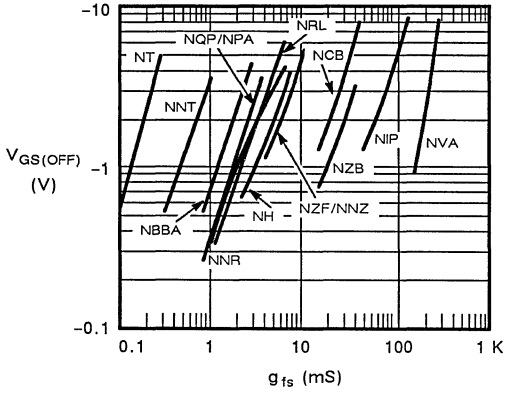
Secondly, a listing of individual device types with their key electrical parameters has been provided for all three product line segments. To aid in selecting a JFET, for example, the list has been broken out by major applications. In fact the user can select JFETs optimized for low-leakage, low-noise, high-gain, high-frequency, and general purpose amplification, as well as n- and p-channel analog switches, current limiting, low leakage diodes, voltage controlled resistors, and specialty JFET circuits. Similar lists are also provided for our lateral DMOS and Low Power MOS product line segments.

All in all Siliconix is confident one of its low power products will find a home in you next application. When system performance is at stake the proper sue of discrete components often is the difference between design success or failure. Through the use of the selector guides, this decision is faster and more reliable.

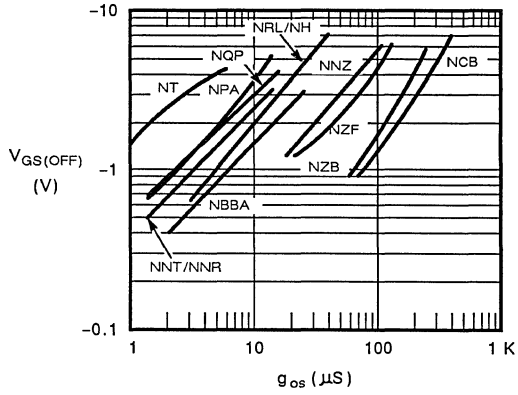
Cutoff Voltage vs. Drain Current



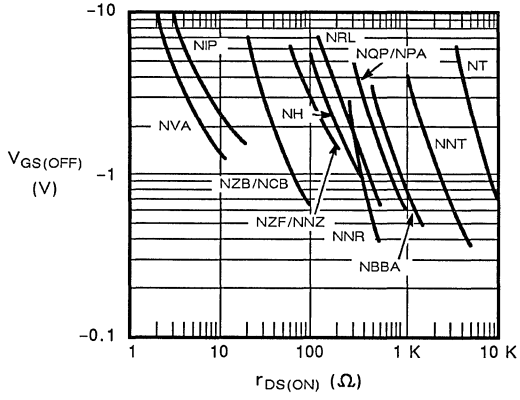
Cutoff Voltage vs. Common-Source Forward Transconductance



Cutoff Voltage vs. Common-Source Output Conductance

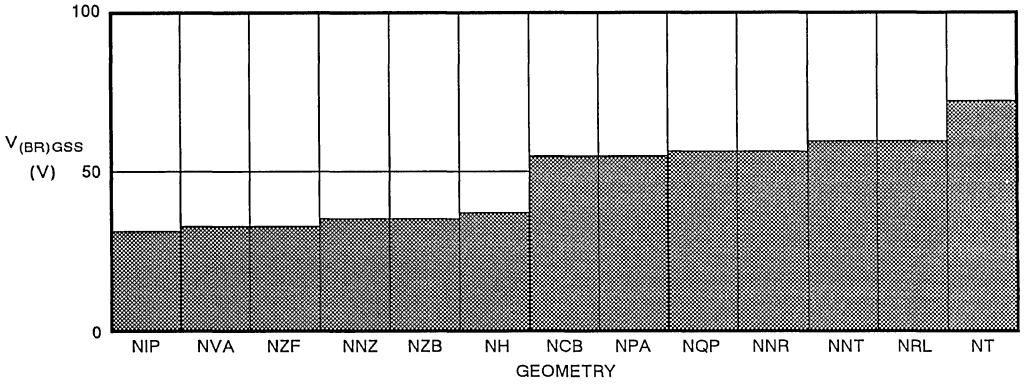


Cutoff Voltage vs. On-Resistance

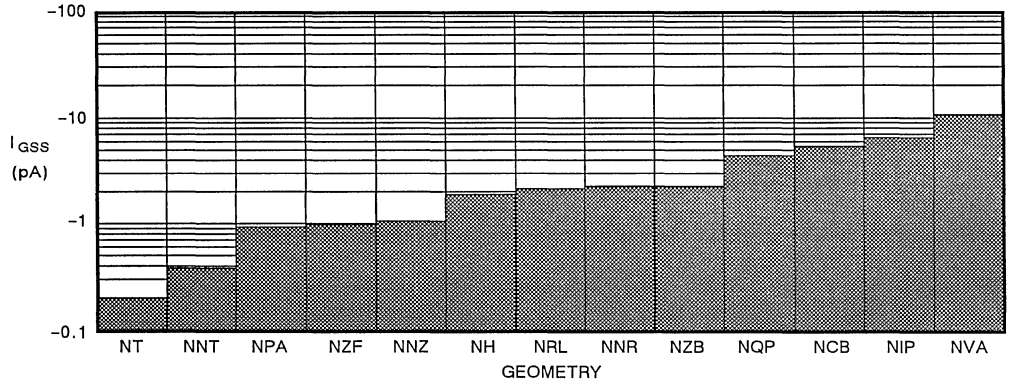


N-CHANNEL GEOMETRY TYPICALS

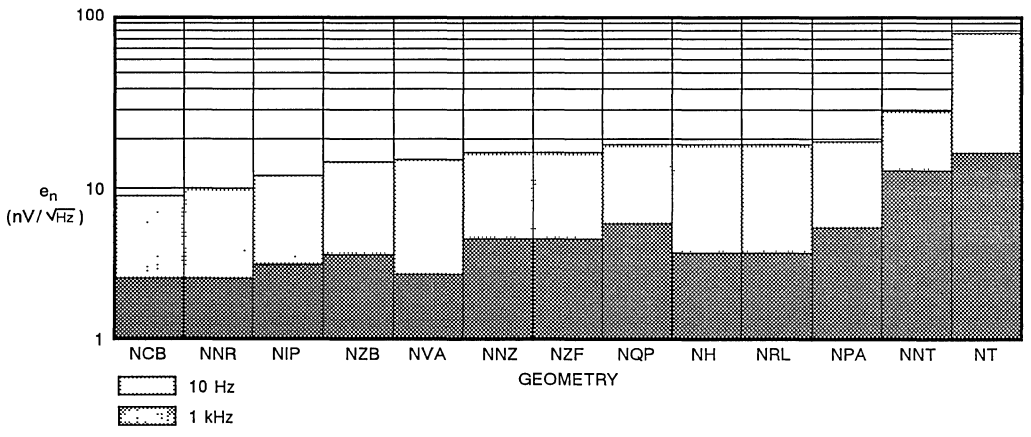
Gate-Source Breakdown Voltage vs. Geometry



Gate Leakage vs. Geometry

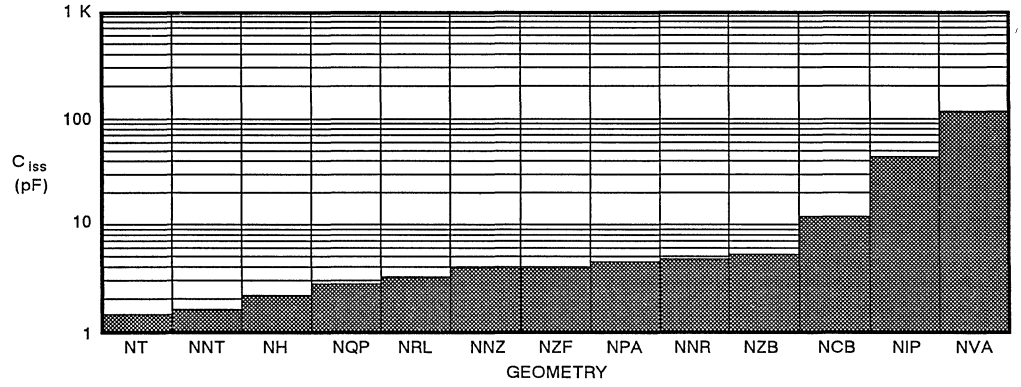


Noise Voltage vs. Geometry

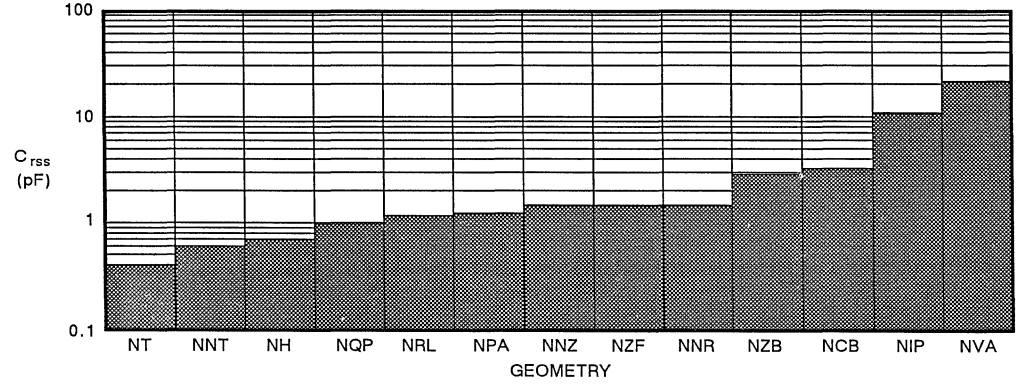


3

Input Capacitance vs. Geometry

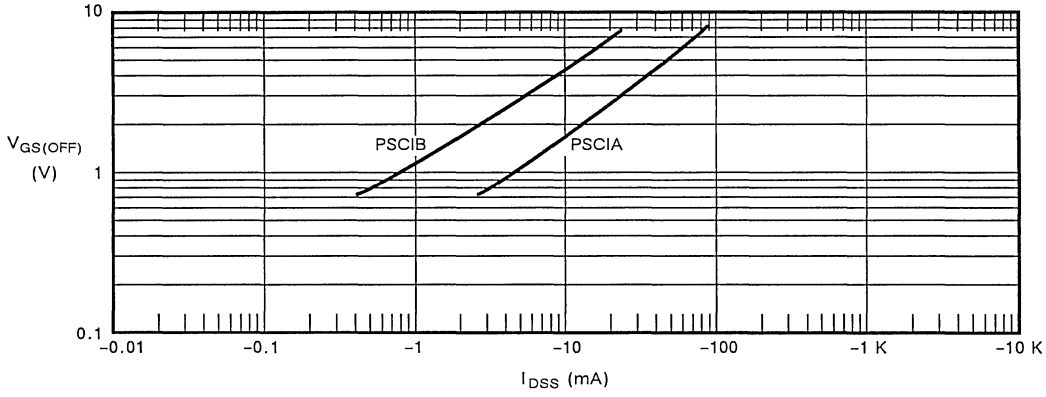


Reverse-Transfer Capacitance vs. Geometry

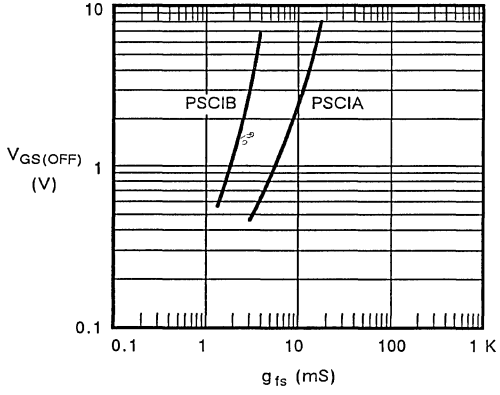


P-CHANNEL GEOMETRY TYPICALS

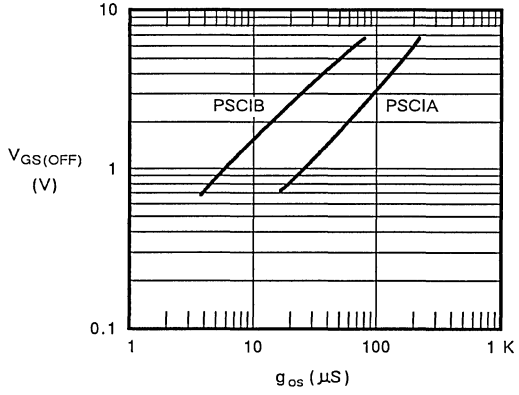
Cutoff Voltage vs. Drain Current



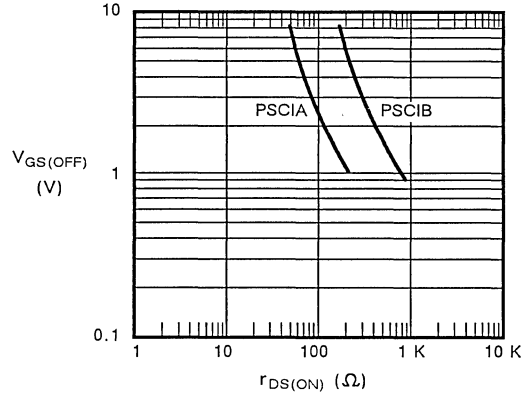
Cutoff Voltage vs. Common-Source Forward Transconductance



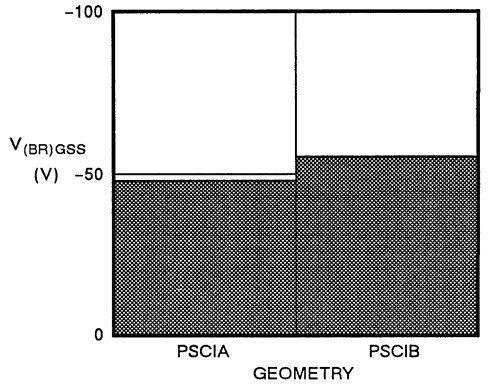
Cutoff Voltage vs. Common-Source Output Conductance



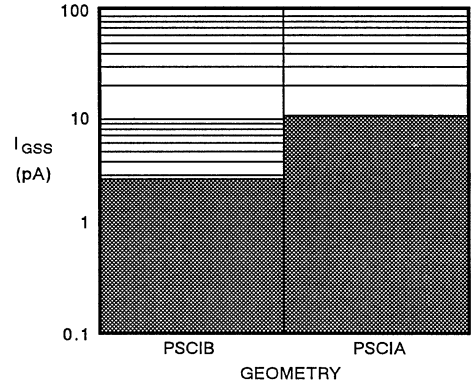
Cutoff Voltage vs. On-Resistance



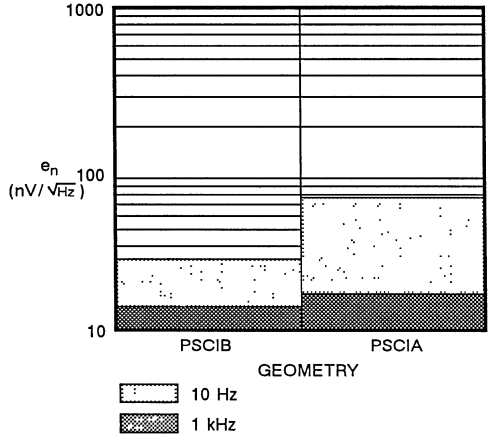
Gate-Source Breakdown Voltage vs. Geometry



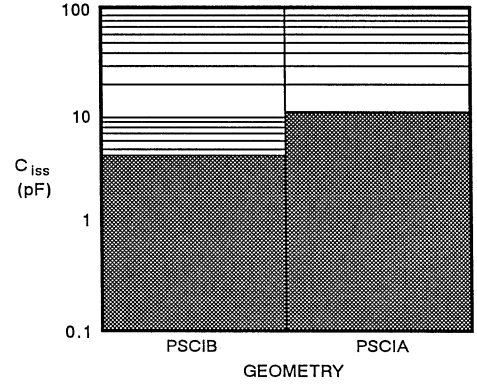
Gate Leakage vs. Geometry



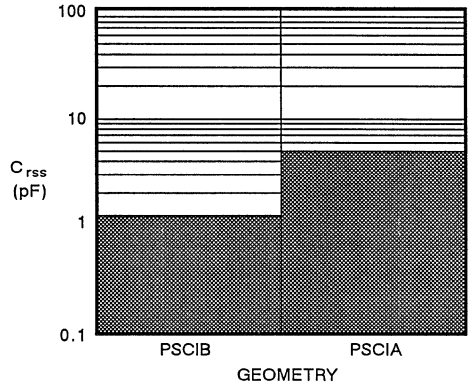
Noise Voltage vs. Geometry



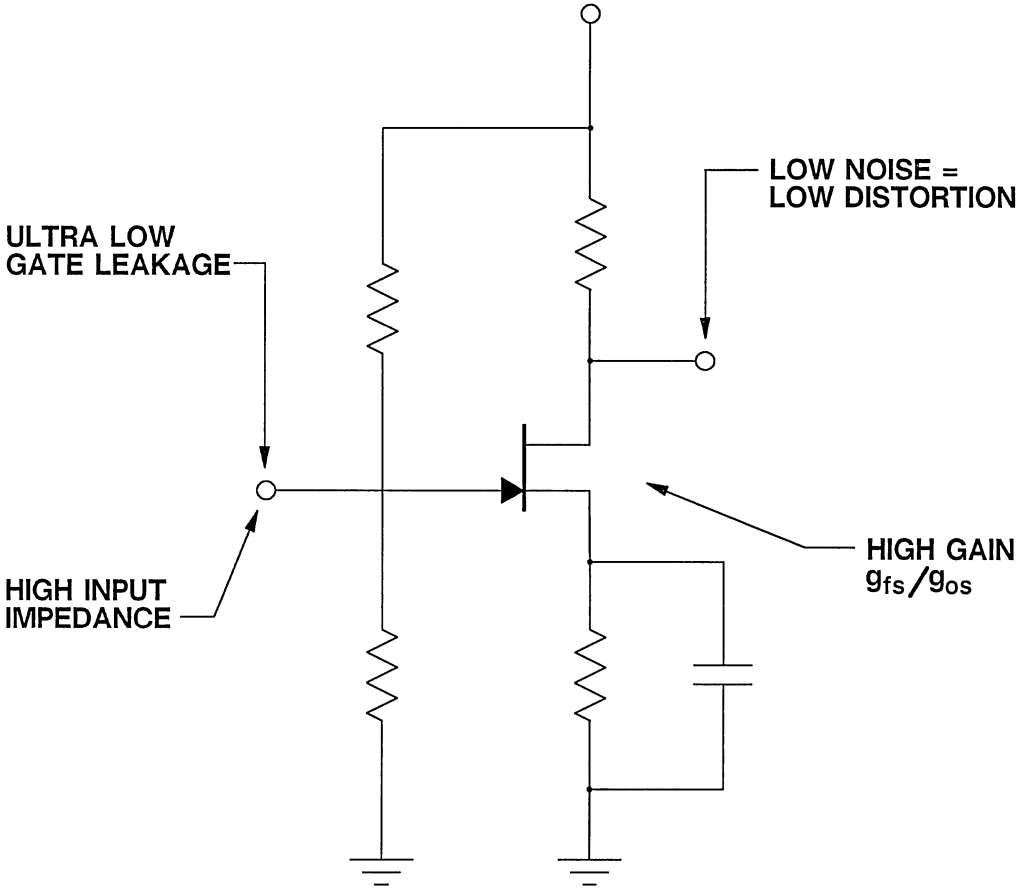
Input Capacitance vs. Geometry



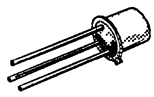
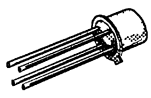
Reverse-Transfer Capacitance vs. Geometry



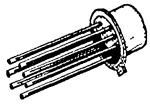
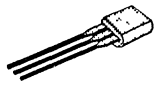
JFET AMPLIFIERS



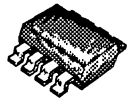
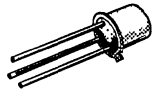
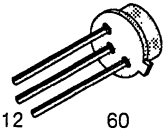
LOW LEAKAGE JFET AMPLIFIERS

PART #	$V_{(BR)GSS}$ (V)	I_{DSS} MIN (mA)	I_{DSS} MAX (mA)	I_{GSS} (pA)	g_{fs} (mS)	g_{os} (µS)	C_{iss} (pF)	C_{rss} (pF)	e_n (nV)	OFF-SET
SOT-23										
SST201	–57	0.2	1	–2	0.5	–	4.5	1.3	6	–
SST202	–57	0.9	4.5	–2	1	–	4.5	1.3	6	–
SST203	–57	4	20	–2	1.5	–	4.5	1.3	6	–
SST204	–57	0.2	3	–2	6	–	4.5	1.3	6	–
TO-18										
2N4338	–57	0.2	0.6	–2	0.6	5	5	1.5	6	–
2N4339	–57	0.5	1.5	–2	0.8	15	5	1.5	6	–
2N4340	–57	1.2	3.6	–2	1.3	30	5	1.5	6	–
2N4341	–57	3	9	–2	2	60	5	1.5	6	–
TO-72										
2N4117	–70	0.03	0.09	–0.2	0.07	3	1.2	0.3	15	–
2N4117A	–70	0.03	0.09	–0.2	0.07	3	1.2	0.3	15	–
2N4118	–70	0.08	0.24	–0.2	0.08	5	1.2	0.3	15	–
2N4118A	–70	0.08	0.24	–0.2	0.08	5	1.2	0.3	15	–
2N4119	–70	0.2	0.6	–0.2	0.1	10	1.2	0.3	15	–
2N4119A	–70	0.2	0.6	–0.2	0.1	10	1.2	0.3	15	–
2N4867	–57	0.4	1.2	–2	0.7	1.5	4.5	1.3	6	–
2N4867A	–57	0.4	1.2	–2	0.7	1.5	4.5	1.3	6	–
2N4868	–57	1	3	–2	1	4	4.5	1.3	6	–
2N4868A	–57	1	3	–2	1	4	4.5	1.3	6	–
2N4869	–57	2.5	7.5	–2	1.3	10	4.5	1.3	6	–
2N4869A	–57	2.5	7.5	–2	1.3	10	4.5	1.3	6	–

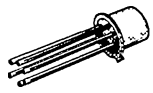
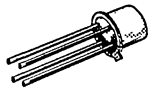
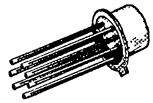
LOW LEAKAGE JFET AMPLIFIERS (Cont'd)

PART #	$V_{(BR)GSS}$ (V)	I_{DSS} MIN (mA)	I_{DSS} MAX (mA)	I_{GSS} (pA)	g_{fs} (mS)	g_{os} (µS)	C_{iss} (pF)	C_{rss} (pF)	e_n (nV)	OFF-SET
TO-78 										
U421	–60	0.06	1	–0.6	0.6	4	1.4	0.7	30	10
U422	–60	0.06	1	–0.6	0.6	4	1.4	0.7	30	15
U423	–60	0.06	1	–0.6	0.6	4	1.4	0.7	30	25
U424	–60	0.06	1.8	–0.8	0.6	4	1.4	0.7	30	10
U425	–60	0.06	1.8	–0.8	0.6	4	1.4	0.7	30	15
U426	–60	0.06	1.8	–0.8	0.6	4	1.4	0.7	30	25
TO-92 										
J201	–57	0.2	1	–2	0.5	–	4.5	1.3	6	–
J202	–57	0.9	4.5	–2	1	–	4.5	1.3	6	–
J203	–57	4	20	–2	1.5	–	4.5	1.3	6	–
J204	–57	0.2	3	–2	0.5	–	4.5	1.3	6	–
J230	–57	0.7	3	–2	1	–	4.5	1.3	14	–
J231	–57	2	6	–2	1.5	–	4.5	1.3	14	–
J232	–57	5	10	–2	2.5	–	4.5	1.3	14	–
PN4117	–70	0.03	0.09	–0.2	3	1.3	0.4	1.3	–	–
PN4117A	–70	0.03	0.09	0.2	3	1.3	0.4	15	–	–
PN4118	–70	0.08	0.24	–0.2	5	1.3	0.4	15	–	–
PN4118A	–70	0.08	0.24	0.2	5	1.3	0.4	15	–	–
PN4119	–70	0.2	0.6	–0.2	10	1.3	0.4	15	–	–
PN4119A	–70	0.2	0.6	0.2	10	1.3	0.4	15	–	–
PN4302	–57	0.5	5	–1	1	50	4.5	1.3	6	–
PN4303	–57	4	10	–1	2	50	4.5	1.3	6	–
PN4304	–57	0.5	15	–1	1	50	4.5	1.3	6	–

LOW NOISE JFET AMPLIFIERS

PART #	$V_{(BR)GSS}$ (V)	I_{DSS} MIN (mA)	I_{DSS} MAX (mA)	I_{GSS} (pA)	g_{fs} (mS)	g_{os} (µS)	C_{iss} (pF)	C_{rss} (pF)	e_n (nV) @1KHz	OFF-SET
SOT-23										
SST201	–57	0.2	1	–2	0.5	–	4.5	1.3	6	–
SST202	–57	0.9	4.5	–2	1	–	4.5	1.3	6	–
SST203	–57	4	20	–2	1.5	–	4.5	1.3	6	–
SST204	–57	0.2	3	–2	6	–	4.5	1.3	6	–
SST308	–35	12	60	–2	14	110	4	1.9	6	–
SST309	–35	12	30	–2	14	110	4	1.9	6	–
SST310	–35	24	60	–2	14	110	4	1.9	6	–
SST4416	–36	5	15	–2	6	15	2.2	0.7	9	–
SO-8										
SST404	–58	0.5	10	–2	1.5	1.3	4	1.5	10	15
SST405	–58	0.5	10	–2	1.5	1.3	4	1.5	10	20
SST406	–58	0.5	10	–2	1.5	1.3	4	1.5	10	40
TO-18										
2N4338	–57	0.2	0.6	–2	0.6	5	5	1.5	6	–
2N4339	–57	0.5	1.5	–2	0.8	15	5	1.5	6	–
2N4340	–57	1.2	3.6	–2	1.3	30	5	1.5	6	–
2N4341	–57	3	9	–2	2	60	5	1.5	6	–
TO-206AC (TO-52)										
U308	–35	12	60	–2	14	250	4	1.9	6	–
U309	–35	12	30	–2	14	250	4	1.9	6	–
U310	–35	24	60	–2	14	250	4	1.9	6	–

LOW NOISE JFET AMPLIFIERS (Cont'd)

PART #	$V_{(BR)GSS}$ (V)	I_{DSS} MIN (mA)	I_{DSS} MAX (mA)	I_{GSS} (pA)	g_{fs} (mS)	g_{os} (µS)	C_{lss} (pF)	C_{rss} (pF)	e_n (nV) @1KHz	OFF-SET
TO-71										
2N6905	-55	0.5	10	-2	4	4	4	1.5	10	5
2N6906	-55	0.5	10	-2	4	4	4	1.5	10	10
2N6907	-55	0.5	10	-2	4	4	4	1.5	10	25
U401	-58	0.5	10	-2	4	5	4	1.5	10	5
U402	-58	0.5	10	-2	4	5	4	1.5	10	10
U403	-58	0.5	10	-2	4	5	4	1.5	10	10
U404	-58	0.5	10	-2	4	5	4	1.5	10	15
U405	-58	0.5	10	-2	4	5	4	1.5	10	20
U406	-58	0.5	10	-2	4	5	4	1.5	10	40
TO-72										
2N4220	-57	0.5	3	-2	1	10	5	1.5	6	-
2N4416	-36	5	15	-2	6	15	2.2	0.7	9	-
2N4416A	-36	5	15	-2	6	15	2.2	0.7	9	-
2N4867	-57	0.4	1.2	-2	0.7	1.5	4.5	1.3	6	-
2N4867A	-57	0.4	1.2	-2	0.7	1.5	4.5	1.3	6	-
2N4868	-57	1	3	-2	1	4	4.5	1.3	6	-
2N4868A	-57	1	3	-2	1	4	4.5	1.3	6	-
2N4869	-57	2.5	7.5	-2	1.3	10	4.5	1.3	6	-
2N4869A	-57	2.5	7.5	-2	1.3	10	4.5	1.3	6	-
TO-78										
U430	-35	12	30	-5	15	100	4.5	2	6	-
U431	-35	24	60	-5	15	100	4.5	2	6	-
TO-92										
2N3819	-35	2	20	-2	5.7	5.5	2.2	0.7	10	-
2N5484	-35	1	5	-2	3	50	2.2	0.7	10	-
2N5485	-35	4	10	-2	3.5	60	2.2	0.7	10	-

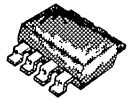
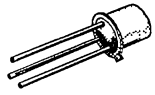
LOW NOISE JFET AMPLIFIERS (Cont'd)

PART #	$V_{(BR)GSS}$ (V)	I_{DSS} MIN (mA)	I_{DSS} MAX (mA)	I_{GSS} (pA)	g_{fs} (mS)	g_{os} (µS)	C_{iss} (pF)	C_{rss} (pF)	e_n (nV) @1KHz	OFF-SET
TO-92 (Cont'd) 										
2N5486	-35	8	20	-2	4	75	2.2	0.7	10	-
BF244A	-35	2	6.5	-2	3	-	2	0.8	10	-
BF244B	-35	2	6.5	-2	3	-	2	0.8	10	-
BF244C	-35	2	6.5	-2	3	-	2	0.8	10	-
BF245A	-35	2	6.5	-2	3	-	2	0.8	10	-
BF245B	-35	6	15	-2	3	-	2	0.8	10	-
BF245C	-35	12	25	-2	3	-	2	0.8	10	-
J201	-57	0.2	1	-2	0.5	-	4.5	1.3	6	-
J202	-57	0.9	4.5	-2	1	-	4.5	1.3	6	-
J203	-57	4	20	-2	1.5	-	4.5	1.3	6	-
J204	-57	0.2	3	-2	0.5	-	4.5	1.3	6	-
J230	-57	0.7	3	-2	1	-	4.5	1.3	14	-
J231	-57	2	6	-2	1.5	-	4.5	1.3	14	-
J232	-57	5	10	-2	2.5	-	4.5	1.3	14	-
J304	-35	5	15	-2	4.5	50	2.2	0.7	10	-
J305	-35	1	8	-2	3	50	2.2	0.7	10	-
J308	-35	12	60	-2	14	110	4	1.9	6	-
J309	-35	12	30	-2	14	110	4	1.9	6	-
J310	-35	24	60	-2	14	110	4	1.9	6	-
PN4302	-57	0.5	5	-1	1	50	4.5	1.3	6	-
PN4303	-57	4	10	-1	2	50	4.5	1.3	6	-
PN4304	-57	0.5	15	-1	1	50	4.5	1.3	6	-
PN4416	-36	5	15	-2	6	15	2.2	0.7	9	-

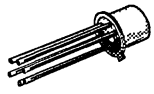
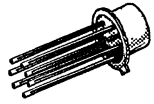
HIGH GAIN JFET AMPLIFIERS

PART #	$V_{(BR)GSS}$ (V)	I_{DSS} MIN (mA)	I_{DSS} MAX (mA)	I_{GSS} (pA)	g_{fs} (mS)	g_{os} (µS)	C_{iss} (pF)	C_{rss} (pF)	e_n (nV) @1KHz	OFF-SET
SOT-23 										
BSR56	-55	50	-	-5	-	-	13	3.5	-	-
BSR57	-55	20	100	-5	-	-	13	3.5	-	-
BSR58	-55	8	80	-5	-	-	13	3.5	-	-
SST111	-55	20	-	-5	6	25	7	3	4	-
SST112	-55	5	-	-5	6	25	7	3	4	-

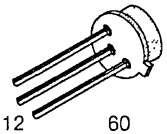
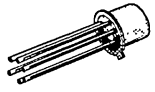
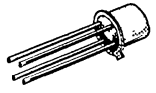
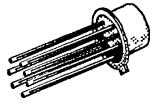
HIGH GAIN JFET AMPLIFIERS (Cont'd)

PART #	$V_{(BR)GSS}$ (V)	I_{DSS} MIN (mA)	I_{DSS} MAX (mA)	I_{GSS} (pA)	g_{fs} (mS)	g_{os} (µS)	C_{iss} (pF)	C_{rss} (pF)	e_n (nV) @1KHz	OFF-SET
SOT-23 (Cont'd) 										
SST113	-55	2	–	-5	6	25	7	3	4	–
SST4091	-55	30	–	-5	6	25	12	3.5	3	–
SST4092	-55	15	–	-5	6	25	12	3.5	3	–
SST4093	-55	8	–	-5	6	25	12	3.5	3	–
SST4391	-55	50	–	-5	6	25	13	3.5	3	–
SST4392	-55	25	–	-5	6	25	13	3.8	3	–
SST4393	-55	5	–	-5	6	25	13	4	3	–
SST4859	-55	30	–	-5	6	25	12	3.5	3	–
SST4860	-55	15	–	-5	6	25	12	3.5	3	–
SST4861	-55	8	–	-5	6	25	12	3.5	3	–
SO-8 										
SST440	-35	6	30	-1	6	20	3.5	1	4	10
SST441	-35	6	30	-1	6	20	3.5	1	4	20
SST5912	-35	7	40	-1	6	20	3.5	1	4	15
TO-18 										
2N4091	-55	30	–	-5	6	25	13	3.5	3	–
2N4092	-55	15	–	-5	6	25	13	3.5	3	–
2N4093	-55	8	–	-5	6	25	13	3.5	3	–
2N4391	-55	50	150	-5	6	25	12	3.3	3	–
2N4392	-55	25	75	-5	6	25	12	3.2	3	–
2N4393	-55	5	30	-5	6	25	12	2.8	3	–
2N4856	-55	50	–	-5	6	25	7	3	3	–
2N4856A	-55	50	–	-5	6	25	7	3	3	–
2N4857	-55	20	100	-5	6	25	7	3	3	–
2N4857A	-55	20	100	-5	6	25	7	3	3	–
2N4858	-55	8	80	-5	6	25	7	3	3	–
2N4858A	-55	8	80	-5	6	25	7	3	3	–
2N4859	-55	50	–	-5	6	25	7	3	3	–
2N4859A	-55	50	–	-5	6	25	7	3	3	–
2N4860	-55	20	100	-5	6	25	7	3	3	–
2N4860A	-55	20	100	-5	6	25	7	3	3	–
2N4861	-55	8	80	-5	6	25	7	3	3	–
2N4861A	-55	8	80	-5	6	25	7	3	3	–

HIGH GAIN JFET AMPLIFIERS (Cont'd)

PART #	$V_{(BR)GSS}$ (V)	I_{DSS} MIN (mA)	I_{DSS} MAX (mA)	I_{GSS} (pA)	g_{fs} (mS)	g_{os} (μS)	C_{iss} (pF)	C_{rss} (pF)	e_n (nV) @1KHz	OFF-SET
TO-71										
2N5564	-55	5	30	-5	9	35	10	2.5	12	5
2N5565	-55	5	30	-5	9	35	10	2.5	12	10
2N5566	-55	5	30	-5	9	35	10	2.5	12	20
M440	-35	6	30	-1	6	20	3.5	1	4	10
M441	-35	6	30	-1	6	20	3.5	1	4	20
TO-78										
M5911	-35	7	40	-1	6	20	3.5	1	4	10
M5912	-35	7	40	-1	6	20	3.5	1	4	15
TO-92										
2N5638	-55	50	-	-5	6	25	7	3	3	-
2N5639	-55	25	-	-5	6	25	7	3	3	-
2N5640	-55	5	-	-5	6	25	7	3	3	-
J111	-55	20	-	-5	6	25	7	3	4	-
J111A	-55	5	-	-5	6	25	7	3	4	-
J112	-55	2	-	-5	6	25	7	3	4	-
J112A	-55	30	-	-5	6	25	7	3	4	-
J113	-55	15	-	-5	6	25	7	3	4	-
J113A	-55	8	-	-5	6	25	7	3	4	-
PN4091	-55	30	-	-5	6	25	13	3.5	4	-
PN4092	-55	15	-	-5	6	25	13	3.5	4	-
PN4093	-55	8	-	-5	6	25	13	3.5	4	-
PN4391	-55	50	150	-5	6	25	12	3.5	3	-
PN4392	-55	25	100	-5	6	25	12	3.5	3	-
PN4393	-55	5	60	-5	6	25	12	3.5	3	-
U1897	-55	30	-	-5	6	25	14	3	3	-
U1898	-55	15	-	-5	6	25	14	3	3	-
U1899	-55	8	-	-5	6	25	14	3	3	-

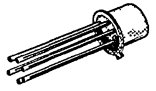
HIGH FREQUENCY JFET AMPLIFIERS

PART #	$V_{(BR)GSS}$ (V)	I_{DSS} MIN (mA)	I_{DSS} MAX (mA)	I_{GSS} (pA)	g_{fs} (mS)	g_{os} (μS)	C_{iss} (pF)	C_{rss} (pF)	e_n (nV) @1KHz	OFF-SET
SOT-23										
SST308	-35	12	60	-2	14	110	4	1.9	6	-
SST309	-35	12	30	-2	14	110	4	1.9	6	-
SST310	-35	24	60	-2	14	110	4	1.9	6	-
SST4416	-36	5	15	-2	6	15	2.2	0.7	9	-
TO-206AC (TO-52)										
U308	-35	12	60	-2	14	250	4	1.9	6	-
U309	-35	12	30	-2	14	250	4	1.9	6	-
U310	-35	24	60	-2	14	250	4	1.9	6	-
TO-71										
U440	-35	6	30	-1	6	70	3	1	4	10
U441	-35	6	30	-1	6	70	3	1	4	20
TO-72										
2N4416	-36	5	15	-2	6	15	2.2	0.7	9	-
2N4416A	-36	5	15	-2	6	15	2.2	0.7	9	-
TO-78										
2N5911	-35	7	40	-1	6	70	3	1	4	10
2N5912	-35	7	40	-1	6	70	3	1	4	15
U430	-35	12	30	-5	15	100	4.5	2	6	-
U431	-35	24	60	-5	15	100	4.5	2	6	-
U443	-35	6	30	-1	6	70	3	1	4	10
U444	-35	6	30	-1	6	70	3	1	4	20

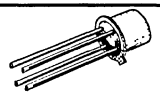
HIGH FREQUENCY JFET AMPLIFIERS (Cont'd)

PART #	$V_{(BR)GSS}$ (V)	I_{DSS} MIN (mA)	I_{DSS} MAX (mA)	I_{GSS} (pA)	g_{fs} (mS)	g_{os} (µS)	C_{iss} (pF)	C_{rss} (pF)	e_n (nV) @1KHz	OFF-SET
TO-92										
2N5484	−35	1	5	−2	3	50	2.2	0.7	10	–
2N5485	−35	4	10	−2 3	.5	60	2.2	0.7	10	–
2N5486	−35	8	20	−2	4	75	2.2	0.7	10	–
BF244A	−35	2 6	.5	−2	3	–	2	0.8	10	–
BF244B	−35	2 6	.5	−2	3	–	2	0.8	10	–
BF244C	−35	2 6	.5	−2	3	–	2	0.8	10	–
BF245A	−35	2 6	.5	−2	3	–	2	0.8	10	–
BF245B	−35	6	15	−2	3	–	2	0.8	10	–
BF245C	−35	12	25	−2	3	–	2	0.8	10	–
J210	−35	2	15	−1	4	150	4	1.5	5	–
J211	−35	7	20	−1	6	200	4	1.5	5	–
J212	−35	15	40	−1	7	200	4	1.5	5	–
J304	−35	5	15	−2 4	.5	50	2.2	0.7	10	–
J305	−35	1	8	−2	3	50	2.2	0.7	10	–
J308	−35	12	60	−2	14	110	4	1.9	6	–
J309	−35	12	30	−2	14	110	4	1.9	6	–
J310	−35	24	60	−2	14	110	4	1.9	6	–
PN4416	−36	5	15	−2	6	15	2.2	0.7	9	–

GENERAL PURPOSE JFET AMPLIFIERS

PART #	$V_{(BR)GSS}$ (V)	I_{DSS} MIN (mA)	I_{DSS} MAX (mA)	I_{GSS} (pA)	g_{fs} (mS)	g_{os} (µS)	C_{iss} (pF)	C_{rss} (pF)	e_n (nV) @1KHz	OFF-SET	CLASS
TO-71											
2N3956	−57	0.5	5	−10	2.5	2	3	1	10	15	D
2N3957	−57	0.5	5	−10	2.5	2	3	1	10	20	D
2N3958	−57	0.5	5	−10	2.5	2	3	1	10	25	D
2N5196	−57	0.7	7	−10	2.5	2	3	1	9	5	D
2N5197	−57	0.7	7	−10	2.5	2	3	1	9	5	D
2N5198	−57	0.7	7	−10	2.5	2	3	1	9	10	D
2N5199	−57	0.7	7	−10	2.5	2	3	1	9	15	D

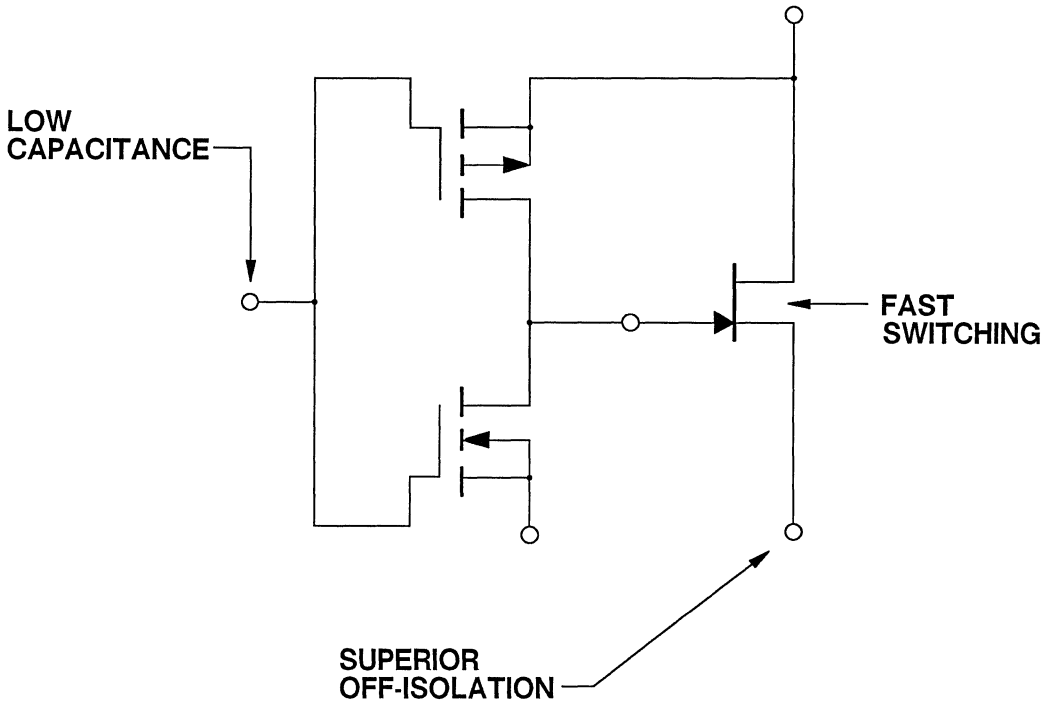
GENERAL PURPOSE JFET AMPLIFIERS (Cont'd)

PART #	$V_{(BR)GSS}$ (V)	I_{DSS} MIN (mA)	I_{DSS} MAX (mA)	I_{GSS} (pA)	g_{fs} (mS)	g_{os} (µS)	C_{iss} (pF)	C_{rss} (pF)	e_n (nV) @1KHz	OFF-SET	CLASS
TO-72											
2N4220	-57	0.5	3	-2	1	10	5	1.5	6	–	A
2N4220A	-57	0.5	3	-2	1	10	5	1.5	6	–	A
2N4221	-57	2	6	-2	2	20	5	1.5	6	–	A
2N4221A	-57	2	6	-2	2	20	5	1.5	6	–	A
2N4222	-57	5	15	-2	2.5	40	5	1.5	6	–	A
2N4222A	-57	5	15	-2	2.5	40	5	1.5	6	–	A
TO-92											
2N3819	-35	2	20	-2	5.7	5.5	2.2	0.7	10	–	A

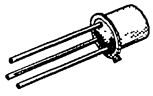
P-CHANNEL GENERAL PURPOSE JFET AMPLIFIERS

PART #	$V_{(BR)GSS}$ (V)	I_{DSS} MIN (mA)	I_{DSS} MAX (mA)	I_{GSS} (pA)	g_{fs} (mS)	g_{os} (µS)	C_{iss} (pF)	C_{rss} (pF)	e_n (nV) @1KHz	OFF-SET
SOT-23										
SST270	45	-2	-15	10	15	200	20	4	20	–
SST271	45	-6	-50	10	18	500	20	4	20	–
TO-92										
2N5460	55	-1	-5	3	1	75	4.5	1.2	15	–
2N5461	55	-2	-9	3 1	.5	75	4.5	1.2	15	–
2N5462	55	-4	-16	3	2	75	4.5	1.2	15	–
2N5463	55	-1	-5	3	1	75	4.5	1.2	15	–
2N5464	55	-2	-9	3 1	.5	75	4.5	1.2	15	–
2N5465	55	-4	-16	3	2	75	4.5	1.2	15	–
J270	45	-2	-15	10	15	200	20	4	20	–
J271	45	-6	-50	10	18	500	20	4	20	–

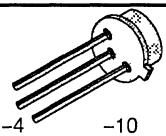
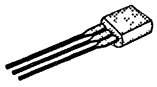
JFET
ANALOG SWITCHES



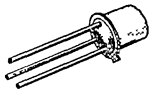
N-CHANNEL JFET ANALOG SWITCHES

PART #	$V_{(BR)GSS}$ (V)	$V_{GS(off)}$ MIN (V)	$V_{GS(off)}$ MAX (V)	I_{DSS} MIN (mA)	I_{DSS} MAX (mA)	$I_{D(OFF)}$ (pA)	$r_{DS(ON)}$ (Ω)	C_{iss} (pF)	C_{rss} (pF)	t_{ON} (ns)
SOT-23 										
BSR56	-55	-4	-10	50	–	5	25	13	3.5	4
BSR57	-55	-2	-6	20	100	5	40	13	3.5	4
BSR58	-55	-0.8	-4	8	80	5	60	13	3.5	4
SST108	-32	-3	-10	80	-2	0	8	60	11	4
SST109	-32	-2	-6	40	-2	0	12	60	11	4
SST110	-32	-0.5	-4	10	-2	0	18	60	11	4
SST111	-55	-3	-10	20	–	5	30	7	3	4
SST112	-55	-1	-5	5	–	5	50	7	3	4
SST113	-55	–	-3	2	–	5	100	7	3	4
SST4091	-55	-5	-10	30	–	5	30	12	3.5	4
SST4092	-55	-2	-7	15	–	5	50	12	3.5	4
SST4093	-55	-1	-5	8	–	5	80	12	3.5	4
SST4391	-55	-4	-10	50	–	5	30	13	3.5	4
SST4392	-55	-2	-5	25	–	5	60	13	3.8	4
SST4393	-55	-0.5	-3	5	–	5	100	13	4	4
SST4859	-55	-5	-10	30	–	5	30	12	3.5	4
SST4860	-55	-2	-7	15	–	5	50	12	3.5	4
SST4861	-55	-1	-5	8	–	5	80	12	3.5	4
TO-18 										
2N4091	-55	-5	-10	30	–	5	30	13	3.5	4
2N4092	-55	-2	-7	15	–	5	50	13	3.5	4
2N4093	-55	-1	-5	8	–	5	80	13	3.5	4
2N4391	-55	-4	-10	50	150	5	30	12	3.3	4
2N4392	-55	-2	-5	25	75	5	60	12	3.2	4
2N4393	-55	-0.5	-3	5	30	5	100	12	2.8	4
2N4856	-55	-4	-10	50	–	5	25	7	3	4
2N4856A	-55	-4	-10	50	–	5	25	7	3	4
2N4857	-55	-2	-6	20	100	5	40	7	3	4
2N4857A	-55	-2	-6	20	100	5	40	7	3	4
2N4858	-55	-0.8	-4	8	80	5	60	7	3	4
2N4858A	-55	-0.8	-4	8	80	5	60	7	3	4
2N4859	-55	-4	-10	50	–	5	25	7	3	4
2N4859A	-55	-4	-10	50	–	5	25	7	3	4
2N4860	-55	-2	-6	20	100	5	40	7	3	4
2N4860A	-55	-2	-6	20	100	5	40	7	3	4
2N4861	-55	-0.8	-4	8	80	5	60	7	3	4
2N4861A	-55	-0.8	-4	8	80	5	60	7	3	4

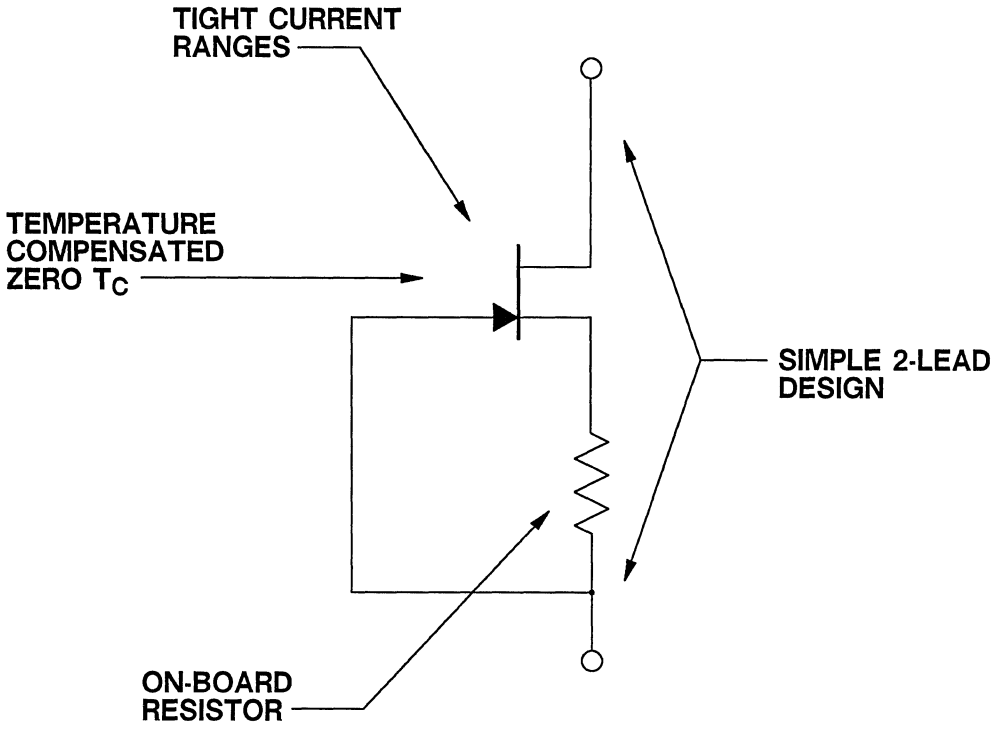
N-CHANNEL JFET ANALOG SWITCHES (Cont'd)

PART #	$V_{(BR)GSS}$ (V)	$V_{GS(off)}$ MIN (V)	$V_{GS(off)}$ MAX (V)	I_{DSS} MIN (mA)	I_{DSS} MAX (mA)	$I_{D(OFF)}$ (pA)	$r_{DS(ON)}$ (Ω)	C_{iss} (pF)	C_{rss} (pF)	t_{ON} (ns)
TO-206AC (TO-52)										
2N5432	-32	-4	-10	150	-	10	5	20	11	2.5
2N5433	-32	-3	-9	100	-	10	7	20	11	2.5
2N5434	-32	-1	-4	30	-	10	10	20	11	2.5
U290	-35	-4	-10	500	-	10	31	20	20	14
U291	-35	-1.5	-4.5	200	-	10	71	20	20	14
TO-92										
2N5638	-55	-	-	50	-	5	30	7	3	4
2N5639	-55	-	-	25	-	5	60	7	3	4
2N5640	-55	-	-	5	-	5	100	7	3	4
J105	-35	-4.5	-10	500	-	10	31	20	20	14
J106	-35	-2	-6	200	-	10	61	20	20	14
J107	-35	-0.5	-4.5	100	-	10	81	20	20	14
J108	-32	-3	-10	80	-	20	8	60	11	4
J109	-32	-2	-6	40	-	20	12	60	11	4
J110	-32	-0.5	-4	10	-	20	18	60	11	4
J110A	-32	-0.5	-4	10	-	20	25	60	11	4
J111	-55	-3	-10	20	-	5	30	7	3	4
J111A	-55	-1	-5	5	-	5	50	7	3	4
J112	-55	-	-3	2	-	5	100	7	3	4
J112A	-55	-5	-10	30	-	5	30	7	3	4
J113	-55	-2	-7	15	-	5	50	7	3	4
J113A	-55	-1	-5	8	-	5	80	7	3	4
PN4091	-55	-5	-10	30	-	5	30	13	3.5	4
PN4092	-55	-2	-7	15	-	5	50	13	3.5	4
PN4093	-55	-1	-5	8	-	5	80	13	3.5	4
PN4391	-55	-4	-10	50	150	5	30	12	3.5	4
PN4392	-55	-2	-5	25	100	5	60	12	3.5	4
PN4393	-55	-0.5	-3	5	60	5	100	12	3.5	4
U1897	-55	-5	-10	30	-	5	30	14	3	4
U1898	-55	-2	-7	15	-	5	50	14	3	4
U1899	-55	-1	-5	8	-	5	80	14	3	4

P-CHANNEL JFET ANALOG SWITCHES

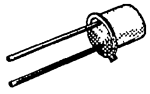
PART #	$V_{(BR)GSS}$ (V)	$V_{GS(off)}$ MIN (V)	$V_{GS(off)}$ MAX (V)	I_{DSS} MIN (mA)	I_{DSS} MAX (mA)	$I_{D(OFF)}$ (pA)	$r_{DS(ON)}$ (Ω)	C_{iss} (pF)	C_{rss} (pF)	t_{ON} (ns)
SOT-23 										
SST174	45	5	10	-20	-135	-10	85	20	5	25
SST175	45	3	6	-7	-70	-10	125	20	5	25
SST176	45	1	4	-2	-35	-10	250	20	5	25
SST177	45	0.8	2.25	-1.5	-20	-10	300	20	5	25
SST5114	45	5	10	-30	-90	-5	75	20	6	16
SST5115	45	3	6	-15	-60	-5	100	20	6	30
SST5116	45	1	4	-5	-25	-5	150	20	6	60
TO-18 										
2N5114	45	5	10	-30	-90	-10	75	20	6	16
2N5114J	45	5	10	-30	-90	-10	75	20	6	16
2N5115	45	3	6	-15	-60	-10	100	20	6	30
2N5115J	45	3	6	-15	-60	-10	100	20	6	30
2N5116	45	1	4	-5	-25	-10	150	20	6	60
2N5116J	45	1	4	-5	-25	-10	175	20	6	42
TO-92 										
J174	45	5	10	-20	-135	-10	85	20	5	25
J175	45	3	6	-7	-70	-10	125	20	5	25
J176	45	1	4	-2	-35	-10	250	20	5	25
J177	45	0.8	2.25	-1.5	-20	-10	300	20	5	25
P1086	45	–	10	-10	–	-10	75	20	5	25
P1087	45	–	5	-5	–	-10	150	20	5	25

JFET
CURRENT LIMITERS



JFET CURRENT LIMITERS

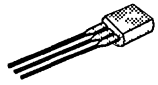
TO-18



PART #	NOMINAL REGULATOR CURRENT	% REGULATION	P_{OV} MIN
CR022	0.22	10	100
CR024	0.24	10	100
CR027	0.27	10	100
CR030	0.3	10	100
CR033	0.33	10	100
CR039	0.39	10	100
CR043	0.43	10	100
CR047	0.47	10	100
CR056	0.56	10	100
CR062	0.62	10	100
CR068	0.68	10	100
CR075	0.75	10	100
CR082	0.82	10	100
CR091	0.91	10	100
CR100	1	10	100
CR110	1.1	10	100
CR120	1.2	10	100
CR130	1.3	10	100
CR140	1.4	10	100
CR150	1.5	10	100
CR160	1.6	10	100
CR180	1.8	10	100
CR200	2	10	100
CR220	2.2	10	100
CR240	2.4	10	100
CR270	2.7	10	100
CR300	3	10	100
CR330	3.3	10	100
CR360	3.6	10	100
CR390	3.9	10	100
CR430	4.3	10	100
CR470	4.7	10	100
CR530	5.3	10	100
CRR0240	0.24	20	100
CRR0360	0.36	20	100
CRR0560	0.56	20	100
CRR0800	0.8	20	100
CRR1250	1.25	20	100
CRR1950	1.95	20	100
CRR2900	2.9	20	100
CRR4300	4.3	20	100

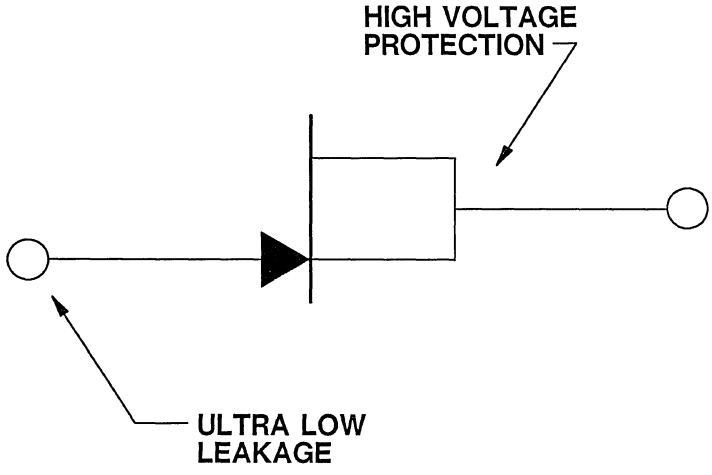
JFET CURRENT LIMITERS (Cont'd)

TO-92

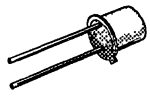
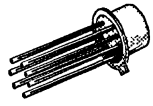


PART #	NOMINAL REGULATOR CURRENT	% REGULATION	P_{OV} MIN
J500	0.24	20	50
J501	0.33	20	50
J502	0.43	20	50
J503	0.56	20	50
J504	0.75	20	50
J505	1	20	50
J506	1.4	20	50
J507	1.8	20	50
J508	2.4	20	50
J509	3	20	50
J510	3.6	20	50
J511	4.7	20	50
J552	0.5	–	100
J553	0.5	40	50
J554	1	40	50
J555	2	40	50
J556	3	40	50
J557	4.5	40	50

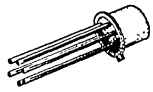
JFET DIODES



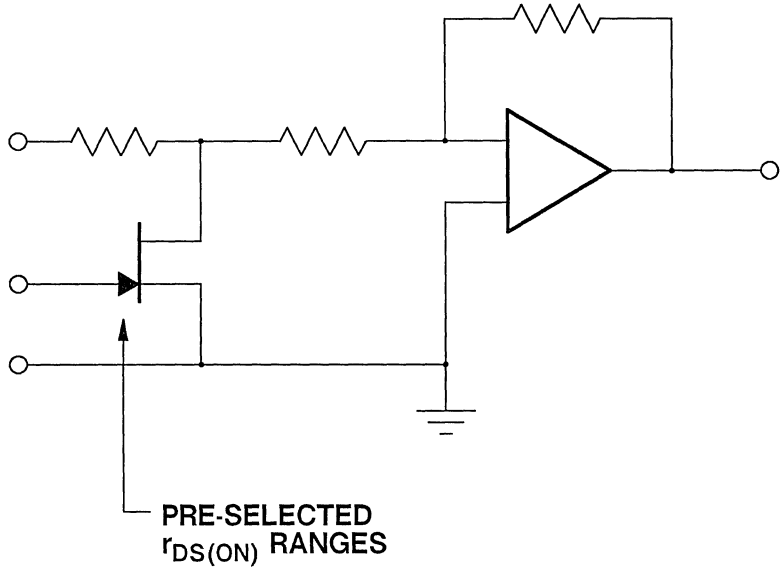
JFET LOW-LEAKAGE DIODES

PART #	REVERSE CURRENT	BREAKDOWN VOLTAGE
SOT-23 		
SSTPAD5	–5	–35
SSTPAD10	–10	–35
SSTPAD20	–20	–35
SSTPAD50	–50	–35
SSTPAD100	–100	–35
SSTPAD200	–200	–35
SSTPAD500	–500	–35
SO-8 		
SSTDPAD5	–5	–30
SSTDPAD10	–10	–30
SSTDPAD20	–20	–30
SSTDPAD50	–50	–30
SSTDPAD100	–100	–30
TO-18 		
PAD1	–1	–45
PAD2	–2	–45
PAD5	–5	–45
PAD10	–10	–35
PAD20	–20	–35
PAD50	–50	–35
PAD100	–100	–35
TO-78 		
DPAD1	–1	–45

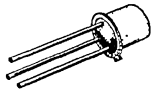
JFET LOW-LEAKAGE DIODES (Cont'd)

PART #	REVERSE CURRENT	BREAKDOWN VOLTAGE
TO-71 		
DPAD2	-2	-45
DPAD5	-5	-45
DPAD10	-10	-35
DPAD20	-20	-35
DPAD50	-50	-35
DPAD100	-100	-35
TO-92 		
JPAD5	-5	-35
JPAD10	-10	-35
JPAD20	-20	-35
JPAD50	-50	-35
JPAD100	-100	-35
JPAD200	-200	-35
JPAD500	-500	-35

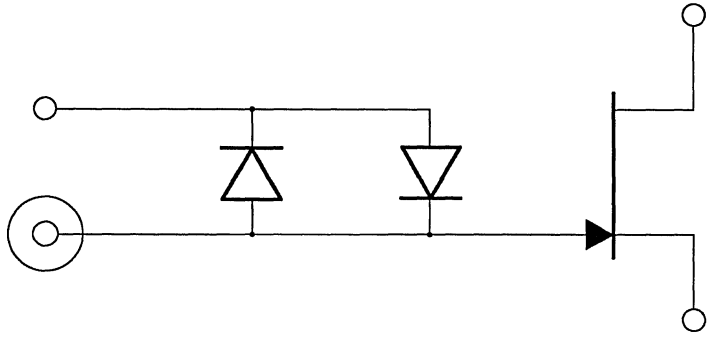
JFET VOLTAGE CONTROLLED RESISTORS



JFET VOLTAGE CONTROLLED RESISTORS

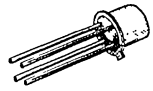
PART #	$r_{DS(ON)}$ MIN	$r_{DS(ON)}$ MAX	$V_{GS(off)}$ MIN	I_{GSS} (pA)	C_{DG}
TO-18 					
N-CHANNEL JFET					
VCR2N	20	60	-1	-5	7.5
VCR4N	200	600	-3.5	-0.2	3
VCR7N	4000	8000	-2.5	-0.1	1.5
P-CHANNEL JFET					
VCR3P	70	200	1	20	25

JFET
SPECIALTY PRODUCTS

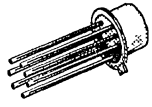


2N6908 MONOLITHIC JFET CIRCUIT

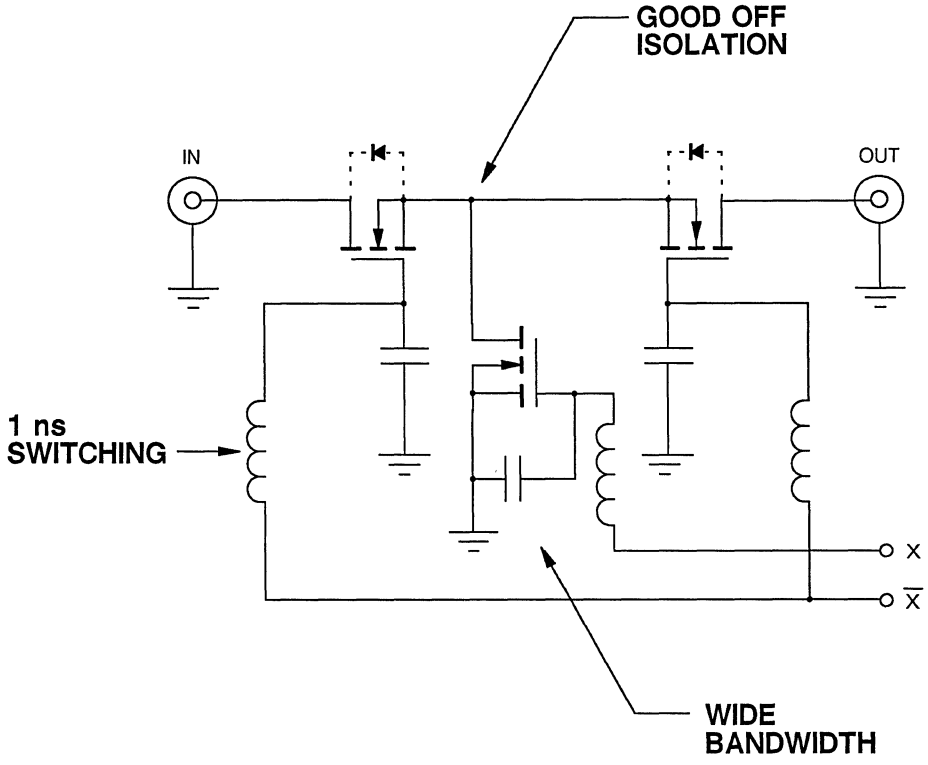
N-CHANNEL JFET (with diode protected input)

PART #	$V_{GS(off)}$ MAX	$V_{(BR)GSS}$ (V)	g_{fs} (μS)	I_{GSS} MAX (pA)	C_{lss} (pF)	$\bar{e}_n$ nV/√Hz
TO-72 						
2N6908	-1.8	-30	100	-25	5	25
2N6909	-2.3	-30	400	-25	5	25
2N6910	-3.5	-30	1200	-25	5	25
SOT-143 						
SST6908	-1.8	-30	100	-25	5	25
SST6909	-2.3	-30	400	-25	5	25
SST6910	-3.5	-30	1200	-25	5	25

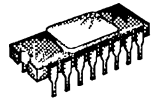
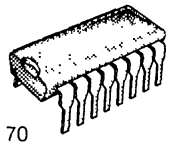
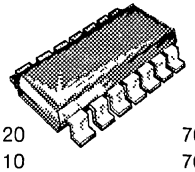
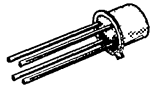
JFET QUAD RING DOUBLE BALANCED MIXER

PART #	$V_{(BR)GSS}$ (V)	$r_{DS(ON)}$ (Ω)	NF (dB)
TO-78 			
V350	-25	90	7

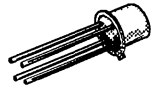
DMOS



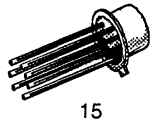
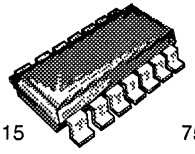
N-CHANNEL ENHANCEMENT-MODE LATERAL DMOS

PART #	$V_{(BR)DS}$ (V)	$r_{DS(ON)}$ (Ω)	$V_{GS(th)}$ (V)	C_{rss} (pF)	t_{ON} (ns)
16-PIN CERAMIC DIP					
2N7116	20	70	2	0.5	2
2N7117	10	70	2	0.5	2
2N7118	15	70	2	0.5	2
SD5000I	10	70	2	0.5	2
SD5001I	20	70	2	0.5	2
SD5002I	15	70	2	0.5	2
16-PIN PLASTIC DIP					
SD5000N	20	70	2	0.5	2
SD5001N	15	70	2	0.5	2
SD5002N	10	70	2	0.5	2
SOT-143					
SST211	10	50	2	0.5	2
SST213	10	50	2	0.5	2
SST215	20	50	2	0.5	2
SO-14					
SD5400CY	20	70	2	0.5	2
SD5401CY	10	70	2	0.5	2
SD5402CY	15	70	2	0.5	2
TO-72					
2N7104	20	70	2	0.5	2
2N7105	10	70	2	0.5	2
2N7106	10	70	2	0.5	2
2N7107	10	70	2	0.5	2
2N7108	15	70	2	0.5	2
2N7109	20	70	2	0.5	2
SD210DE	20	45	2	0.5	2
SD211DE	10	45	2	0.5	2
SD212DE	10	45	2	0.5	2

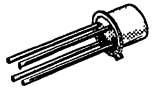
N-CHANNEL ENHANCEMENT-MODE LATERAL DMOS (Cont'd)

PART #	$V_{(BR)DS}$ (V)	$r_{DS(ON)}$ (Ω)	$V_{GS(th)}$ (V)	C_{rss} (pF)	t_{ON} (ns)
TO-72 (Cont'd) 					
SD213DE	10	45	2	0.5	2
SD214DE	15	45	2	0.5	2
SD215DE	20	45	2	0.5	2

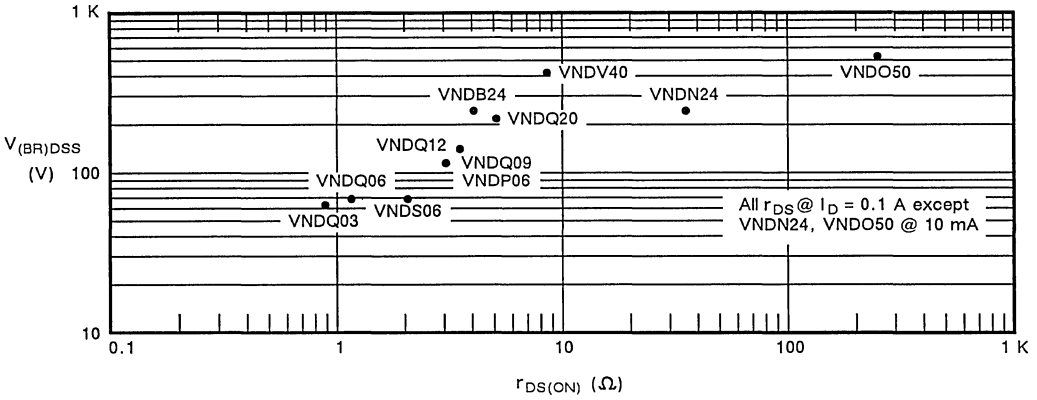
DOUBLE BALANCED MIXER

PART #	$V_{(BR)DS}$ (V)	$r_{DS(ON)}$ (Ω)	$V_{GS(th)}$ (V)	C_{rss} (pF)	t_{ON} (ns)
TO-78 					
Si8901A	15	75	2	–	–
SO-14 					
Si8901CY	15	75	2	–	–

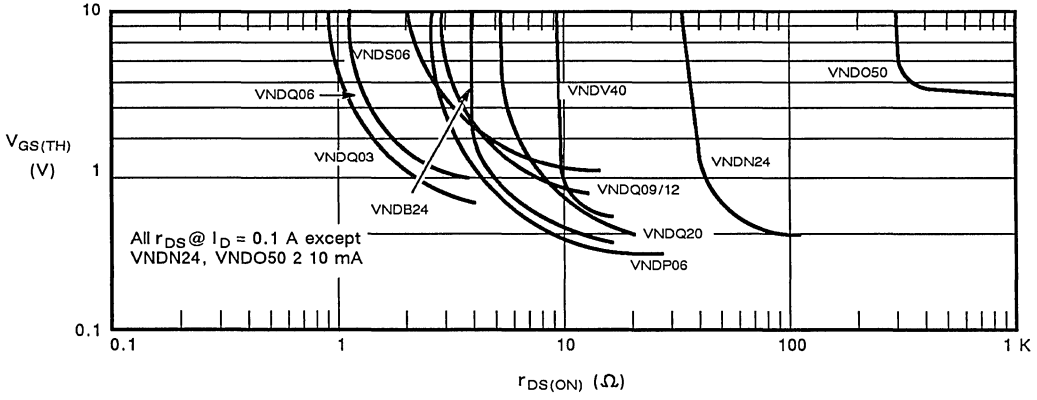
N-CHANNEL DEPLETION-MODE LATERAL DMOS

PART #	$V_{(BR)DS}$ (V)	$r_{DS(ON)}$ (Ω)	$V_{GS(th)}$ (V)	C_{rss} (pF)	t_{ON} (ns)
TO-72 					
SD2100	25	200	–2	2.5	2
SOT-143 					
SST2100	25	200	–2	2.5	2

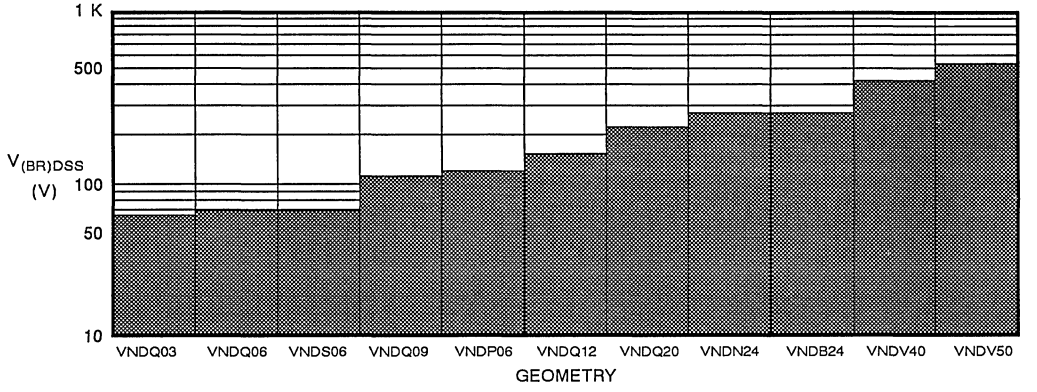
On-Resistance vs. Drain-Source Breakdown Voltage



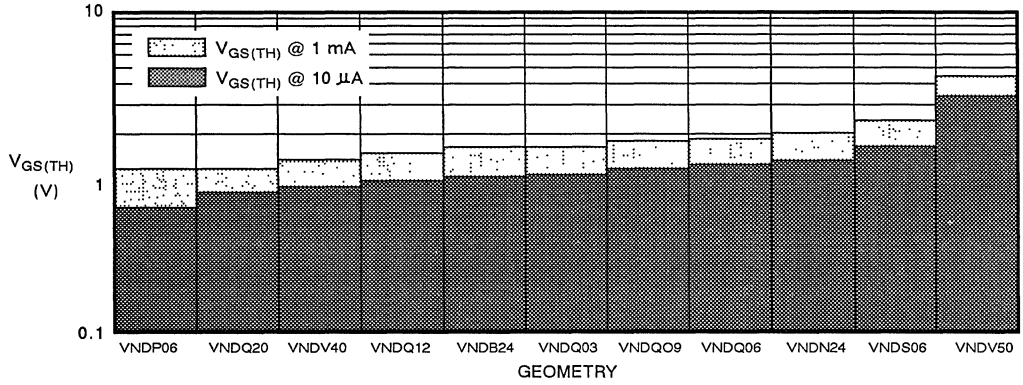
Gate-Source Voltage vs. On-Resistance



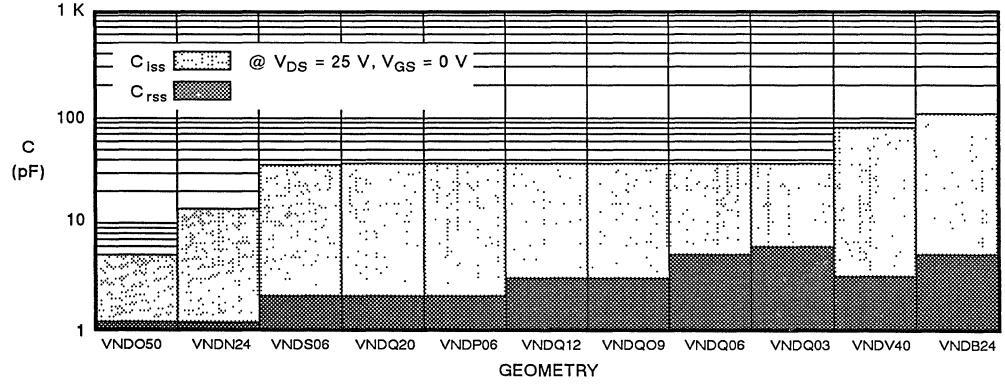
Drain-Source Breakdown Voltage vs. Geometry



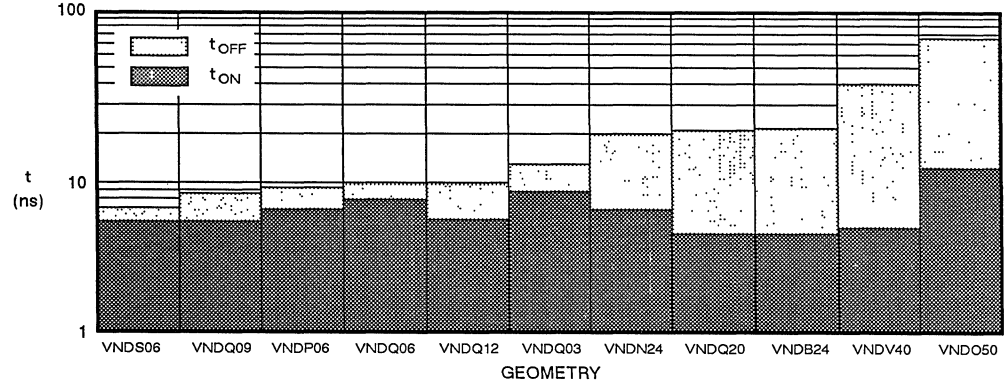
Gate-Source Threshold Voltage vs. Geometry



Capacitance vs. Geometry

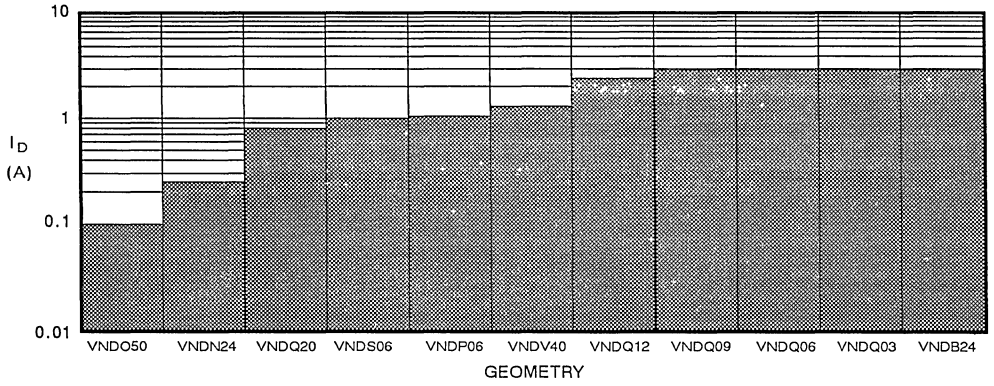


Typical Switching Time vs. Geometry

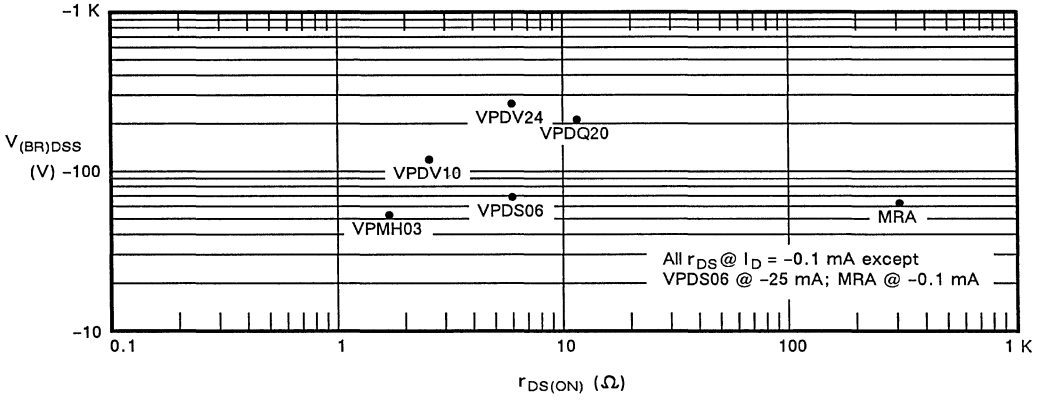


N-CHANNEL GEOMETRIES

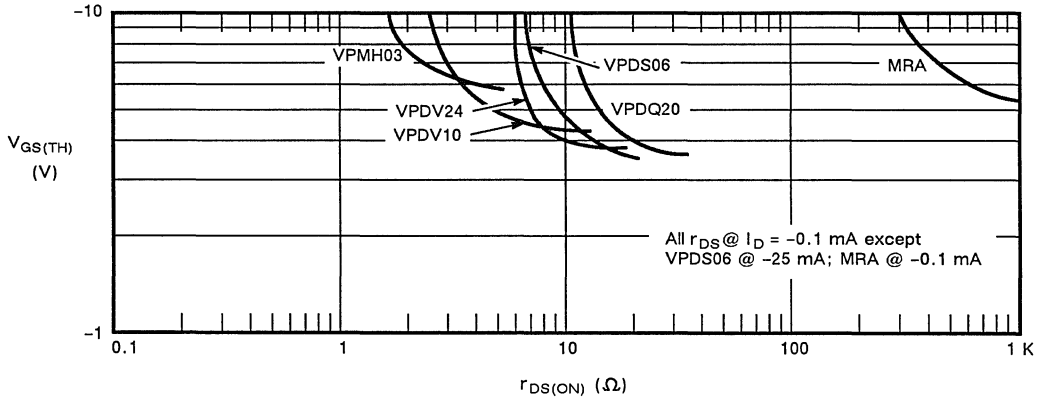
Maximum Drain Current vs. Geometry



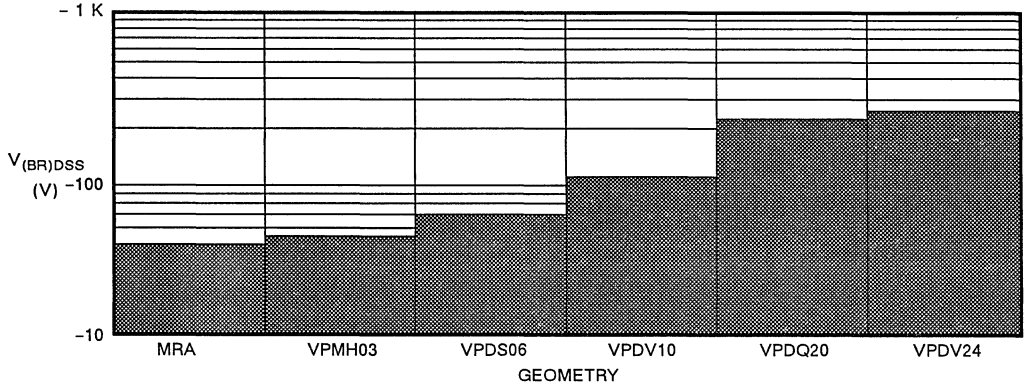
On-Resistance vs. Drain-Source Breakdown Voltage



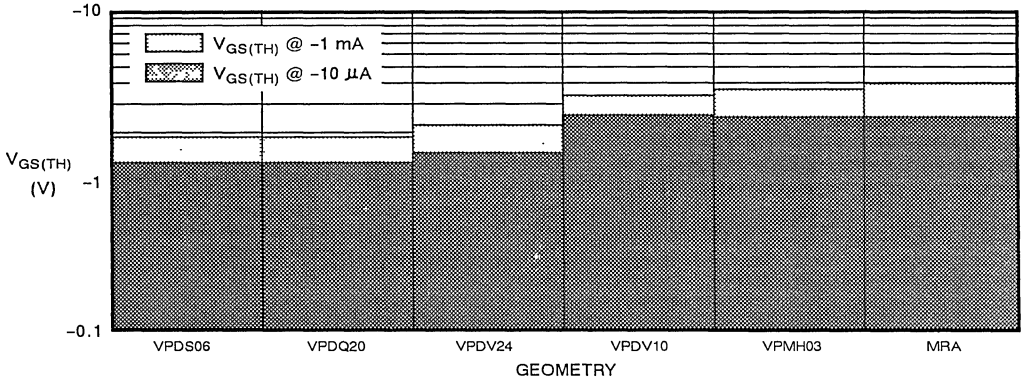
On-Resistance vs. Gate-Source Voltage



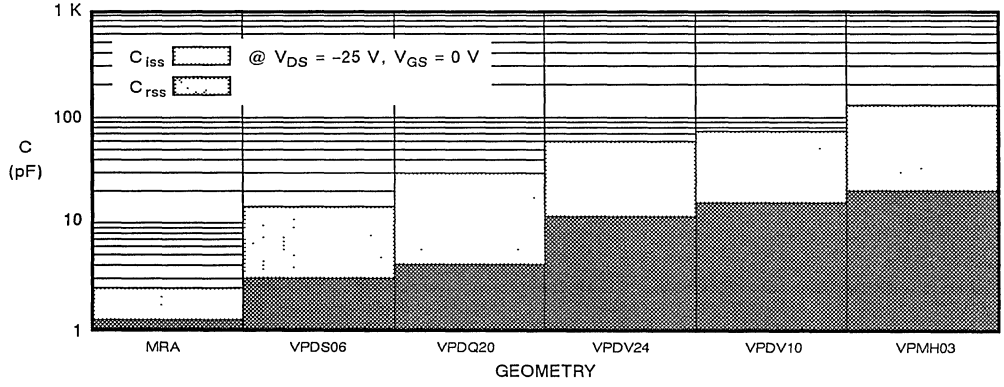
Drain-Source Breakdown Voltage vs. Geometry



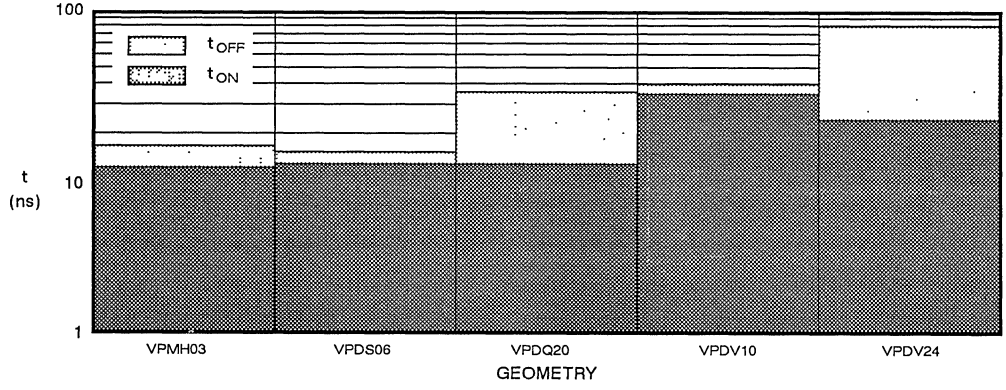
Gate-Source Threshold Voltage vs. Geometry



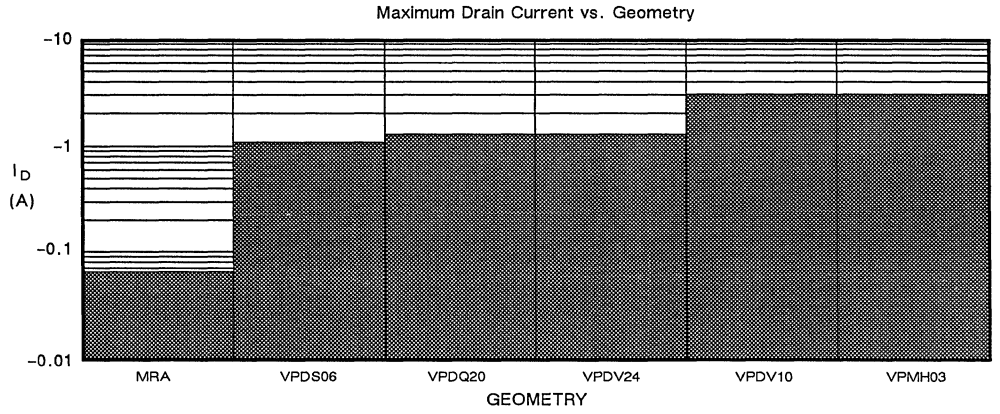
Capacitance vs. Geometry



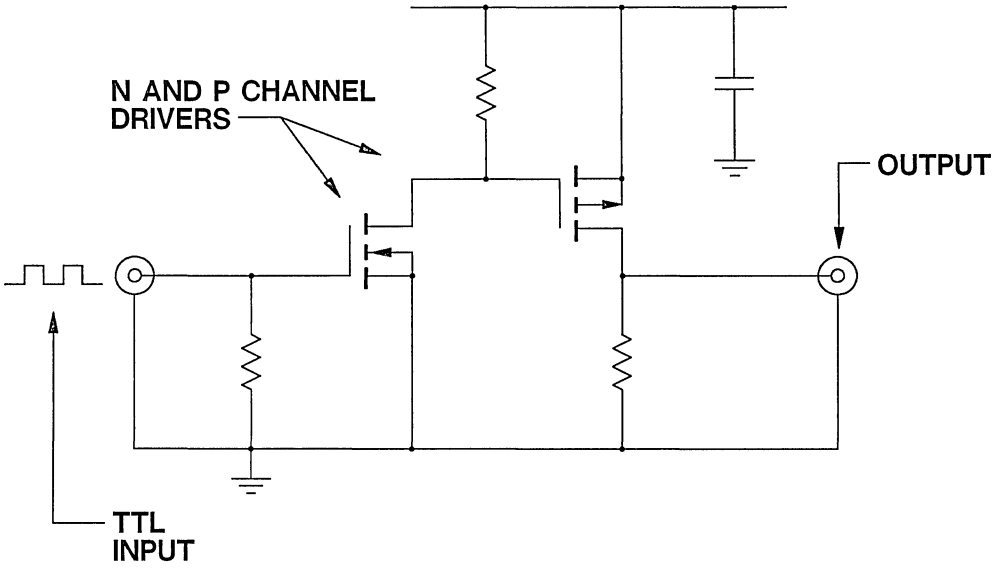
Typical Switching Time vs. Geometry



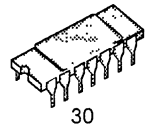
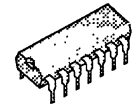
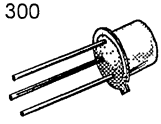
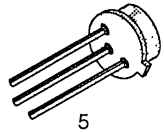
3


Maximum Drain Current vs. Geometry
-10
-1
-0.1
-0.01
I_D
(A)
MRA
VPDS06
VPDQ20
VPDV24
VPDV10
VPMH03
GEOMETRY

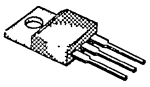
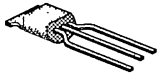
LOW POWER MOS



N-CHANNEL

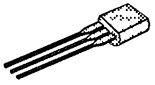
PART #	$V_{(BR)DS}$ (V)	$r_{DS(ON)}$ (Ω)	$V_{GS(th)}$ (V)	t_{ON} (ns)	C_{iss} (pF)	I_D (mA)	PD
14-PIN CERAMIC (P) & PLASTIC (J)							
VQ1001J	30	1	2.5	30	38	0.85	2
VQ1001P	30	1	2.5	30	38	0.85	2
VQ1004P	60	3.5	2.5	10	35	0.46	2
VQ1004J	60	3.5	2.5	10	35	0.46	2
VQ1000J	60	5.5	2.5	10	16	0.23	2
VQ1000P	60	5.5	2.5	10	16	0.23	2
VQ1006P	90	4.5	2.5	10	35	0.40	2
VQ1006J	90	4.5	2.5	10	35	0.40	2
SOT-23							
VN0603T	60	4	3.0	15	16	0.22	0.36
VN0605T	60	5	3.0	20	16	0.18	0.36
2N7002	60	8	2.5	20	16	0.12	0.2
2N7001	240	45	2.5	30	15	0.05	0.2
VN45350T	450	350	4.5	25	5	0.02	0.35
VN50300T	500	300	4.5	20	5	0.02	0.35
TO-205AD (TO-39)							
VN0300B	30	1.2	2.5	30	38	1.51	5
2N6659	35	1.8	2.0	10	38	1.40	6.25
2N6660JANTX	60	3	2.0	10	30	0.99	6.25
2N6660	60	3	2.0	10	38	1.10	6.25
VN67AB	60	3.5	2.5	15	35	0.79	5
2N6661JANTX	90	4	2.0	10	30	0.86	6.25
2N6661	90	4	2.0	10	35	0.90	6.25
VN90AB	90	5	2.0	10	35	0.67	5
VN1206B	120	6	2.0	16	35	0.22	5
VN1706B	170	6	2.0	16	105	0.63	6.25
VN2406B	240	6	2.0	16	110	0.63	6.25
VN4012B	400	12	1.8	40	80	0.42	0.8
TO-206AC (TO-52)							
VN10LE	60	5	2.5	10	16	0.38	1.5
VN10KE	60	5	2.5	10	38	0.17	0.3

N-CHANNEL (Cont'd)

PART #	$V_{(BR)DS}$ (V)	$r_{DS(ON)}$ (Ω)	$V_{GS(th)}$ (V)	t_{ON} (ns)	C_{iss} (pF)	I_D (mA)	PD
TO-220/TO-220SD 							
VN46AFD	40	3	2.5	15	35	1.46	15
VN40AFD	40	5	2.5	15	35	1.14	15
VN66AD	60	3	2.5	15	35	1.70	20
VN66AFD	60	3	2.5	15	35	1.46	15
VN67AD	60	3.5	2.5	15	35	1.58	20
VN67AFD	60	3.5	2.5	15	35	1.37	15
VN88AD	80	4	2.5	15	35	1.49	20
VN88AFD	80	4	2.5	15	35	1.29	15
VN1206D	120	6	2.0	16	35	0.33	20
VN1706D	170	6	2.0	16	105	1.12	20
VN2406D	240	6	2.0	16	110	1.12	20
TO-237 							
VN0300M	30	1.2	2.5	30	38	0.67	1
VN10KM	60	5	2.5	10	38	0.31	1
VN10LM	60	5	2.5	10	16	0.32	1
VN2222LM	60	7.5	2.5	10	16	0.26	1
VN2222KM	60	7.5	2.5	10	38	0.25	1
VN0808M	80	4	2.0	10	35	0.33	1
VN1206M	120	6	2.0	16	35	0.26	1
VN1210M	120	10	2.0	16	35	0.20	1
VN1706M	170	6	2.0	16	105	0.25	1
VN1710M	170	10	2.0	16	110	0.19	1
VN2406M	240	6	2.0	16	110	0.25	1
VN2410M	240	10	2.0	16	110	0.19	1
TO-92 							
VN0300L	30	1.2	2.5	30	38	0.64	0.8
VN0603L	60	3.5	3.0	15	16	0.30	0.8
2N7000	60	5	3.0	10	16	0.20	0.4
VN0610L	60	5	2.5	10	38	0.27	0.8
BS170	60	5	3.0	10	16	0.50	0.83
VN0610LL	60	5	2.5	10	16	0.28	0.8
VN2222LL	60	7.5	2.5	10	16	0.23	0.8
2N7008	60	7.5	2.5	20	16	0.15	0.4
VN2222L	60	7.5	2.5	10	38	0.23	0.8
VN0808L	80	4	2.0	10	35	0.30	0.8

N-CHANNEL (Cont'd)

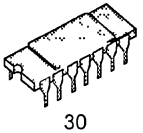
TO-92 (Cont'd)

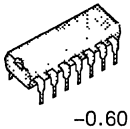


PART #	$V_{(BR)DS}$ (V)	$r_{DS(ON)}$ (Ω)	$V_{GS(th)}$ (V)	t_{ON} (ns)	C_{iss} (pF)	I_D (mA)	PD
VN1206L	120	6	2.0	16	35	0.23	0.8
VN1210L	120	10	2.0	16	35	0.18	0.8
VN1706L	170	6	2.0	16	105	0.22	0.8
VN1710L	170	10	2.0	16	110	0.17	0.8
BSS89	200	6	2.8	80	105	0.30	1
VN2010L	200	10	1.8	20	35	0.19	0.8
VN2020L	200	20	2.0	20	35	0.08	0.8
BS107	200	28	3.0	–	35	0.12	0.5
VN2406L	240	6	2.0	16	110	0.22	0.8
VN2410L	240	10	2.0	16	110	0.17	0.8
2N7007	240	45	2.5	30	15	0.07	0.4
VN3515L	350	15	1.8	40	80	0.15	0.8
VN4012L	400	12	1.8	40	80	0.16	5
VN45350L	450	350	4.5	25	5	0.03	0.8
VN50300L	500	300	4.5	20	5	0.03	0.8

P-CHANNEL

14-PIN CERAMIC (P) & PLASTIC (J)



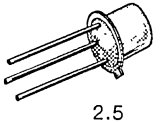
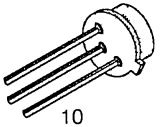
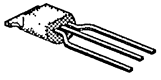
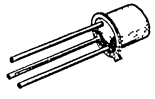
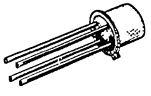


VQ2001J	–30	2	–4.5	30	130	–0.60	2.00
VQ2001P	–30	2	–4.5	30	130	–0.60	2.00
VQ2000J	–60	10	–3.0	35	15	–0.24	2.00
VQ2000P	–60	10	–3.0	35	15	–0.24	2.00
VQ2004P	–60	5	–4.5	55	75	–0.41	2.00
VQ2004J	–60	5	–4.5	55	75	–0.41	2.00
VQ2006P	–90	5	–4.5	55	75	–0.41	2.00
VQ2006J	–90	5	–4.5	55	75	–0.41	2.00

SOT-23

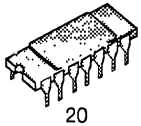
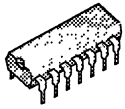
TP0610T	–60	10	–2.4	25	15	–0.12	0.36
VP0610T	–60	10	–3.5	25	15	–0.12	0.36

P-CHANNEL (Cont'd)

PART #	$V_{(BR)DS}$ (V)	$r_{DS(ON)}$ (Ω)	$V_{GS(th)}$ (V)	t_{ON} (ns)	C_{iss} (pF)	I_D (mA)	PD
TO-205AD (TO-39)							
VP0300B	-30	2.5	-4.5	30	130	-1.25	6.25
VP0808B	-80	5	-4.5	55	75	-0.88	6.25
VP1008B	-100	5	-4.5	55	75	-0.79	6.25
VP2410B	-240	10	-2.5	45	65	-0.17	0.73
TO-206AC (TO-52)							
TP0610E	-60	10	-2.4	25	15	-0.25	1.50
VP0610E	-60	10	-3.5	25	15	-0.25	1.50
VP2020E	-200	20	-2.5	25	30	-0.17	1.50
TO-237							
VP0300M	-30	2.5	-4.5	30	130	-0.50	1.00
VP0808M	-80	5	-4.5	55	75	-0.31	1.00
VP1008M	-100	5	-4.5	55	75	-0.31	1.00
TO-92							
VP0300L	-30	2.5	-4.5	30	130	-0.32	0.80
BS250	-45	14	-3.5	10	15	-0.18	0.83
VP0610L	-60	10	-3.5	25	15	-0.18	0.80
TP0610L	-60	10	-2.4	25	15	-0.18	0.80
VP0808L	-80	5	-4.5	55	75	-0.28	0.80
VP1008L	-100	5	-4.5	55	75	-0.28	0.80
BSS92	-200	20	-2.8	14	30	-0.15	1.00
VP2020L	-200	20	-2.5	25	30	-0.12	0.80
BS208	-200	14	-	14	70	-0.20	0.83
VP2410L	-240	10	-2.5	45	65	-0.18	0.80
TO-18							
MFE823	-25	180	-6	2.4	-	-0.03	0.375
TO-72							
3N164	-30	300	-5	36	2.4	-0.05	0.375
3N163	-40	250	-5	36	2.4	-0.05	0.375

3

N- & P-CHANNEL QUADS

PART #	$V_{(BR)DS}$ (V)	$r_{DS(ON)}$ (Ω)	$V_{GS(th)}$ (V)	t_{ON} (ns)	C_{lss} (pF)	I_D (mA)	PD
14-PIN CERAMIC (P) & PLASTIC (J)							
VQ7254J	±20	3	–	20	85	±2	1.75
VQ7254P	±20	3	–	20	85	±2	1.75
VQ3001J	±30	1/2	-4.5	30	85	–	2.00
VQ3001P	±30	1/2	-4.5	30	85	–	2.00

N-CHANNEL DEPLETION-MODE MOS

TO-205AD (TO-39)							
ND2406B	240	6	-4.5	90	70	0.57	5.00
ND2410B	240	10	-2.5	90	70	0.46	5.00
TO-206AC (TO-52)							
ND2012E	200	12	-4.0	40	35	0.22	1.50
ND2020E	200	20	-2.5	40	35	0.18	1.50
TO-92							
ND2012L	200	12	-4.0	40	35	0.16	0.80
ND2020L	200	20	-2.5	40	35	0.13	0.80
BSS129	230	20	–	90	70	0.15	1.00
ND2406L	240	6	-4.5	90	70	0.23	0.80
ND2410L	240	10	-2.5	90	70	0.18	0.80

JFETS

INTRODUCTION

Although junction field-effect transistors have existed for decades, the additional performance that can presently be achieved through their use is undeniable. Even in today's highly integrated world and despite numerous attempts, successful integration of the JFET has proven inconsistent at best. New markets and applications continue to open as designer's demand higher performance from their systems -- the JFET is definitely here to stay!

In addition to enhancing performance, the JFET is also often used as a versatile "problem-solver" to improve systems without compromising their key requirements. The inherent JFET characteristics--low-noise, low leakage, high-gain, and fast switching all contribute significantly to system speed. Let's now take a closer look at these benefits.

Unlike the bipolar transistor, which requires a base-drive current, a field-effect transistor is operated by the application of a gate voltage. Thus, while the bipolar transistor exhibits low input impedance, the JFET offers just the opposite -- a very high impedance gate!

The high-impedance nature of a JFET offers superb low-leakage qualities -- often specified in the low picoamp range. When this is coupled with good frequency response, JFETs ensure minimal circuit loading for such sensitive applications as sample-and-hold circuits and input devices for operational amplifiers.

An additional and fundamental advantage of the JFET is its extraordinarily low noise at 1/f frequencies -- so low that in comparative studies with bipolar transistors the JFET is considered noiseless! This advantage is most obvious in applications involving high source impedances, such as those needed for low-noise electret and capacitor microphone amplifier circuits.

Yes, JFETs are important problem solvers used to enhance the performance of a wide range of applications.

For additional technical assistance see section 9 for application notes. "An Introduction To FETs" (LPD-1) and "JFET Characteristics" (LPD-2) are especially useful reading for first-time JFET designers.

When the performance of your system is at stake, we're confident you'll turn to JFETs. When it comes to performance in manufacturing JFETs, the only place to turn is Siliconix -- the undisputed market leader. We offer the most standard part types, packaging options, and complete military processing per MIL-S-19500. We look forward to supplying JFETs for your next demanding design.

2N3819

Siliconix incorporated

N-Channel JFET

The 2N3819 is a low-cost, all purpose JFET which offers good performance at mid-to-high frequencies. If features low noise and leakage and guarantees high gain at 100 MHz. Its TO-92 package is fully compatible with various tape and reel options for automated assembly. (See Section 8.)

For additional design information please see performance curves NH and NRL, which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
2N3819	-8	-25	2	20

TO-92 BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN

SIMILAR PRODUCTS

- TO-72, See 2N4416
- SOT-23, See SST4416
- Chips, Order 2N3819CHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	
Gate Current	I_G	10	mA
Power Dissipation	P_D	200	mW
Power Derating		2	mW/°C
Operating Junction Temperature	T_J	-55 to 125	°C
Storage Temperature	T_{stg}	-65 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				2N3819		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-35	-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 2 nA	-3		-8	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V	10	2	20	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-0.002		-2	nA
		T_A = 100°C	-0.002		-2	µA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 1 mA	-20			pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 10 V, V_{GS} = -8 V	5			pA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA	150			Ω
Gate-Source Voltage	V_{GS}	V_{DS} = 15 V, I_D = 200 µA	-2.5	-0.5	-7.5	V
Gate-Source Forward Voltage	$V_{GS(f)}$	I_G = 1 mA, V_{DS} = 0 V	0.7			V
DYNAMIC						
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 kHz	5.7	2	6.5	mS
		V_{DS} = 15 V, V_{GS} = 0 V, f = 100 MHz	5.5	1.6		mS
Common-Source Output Conductance	g_{os}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 kHz	15		50	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	2.2		8	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		0.7		4	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 100 Hz	10			$nV/\sqrt{Hz}$

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

4

2N3956 SERIES

Siliconix incorporated

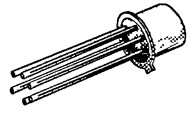
N-Channel JFET Pairs

The 2N3956 Series are monolithic JFET pairs designed for high performance differential amplification. This series features tight matching, low gate leakage for accuracy, and wide dynamic range as I_G is guaranteed at V_{DS} = 20 V. Its TO-71 package is hermetically sealed and is available with full military processing. (See Section 1.)

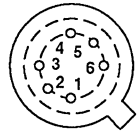
For additional design information please see performance curves NQP, which are located in Section 7.

PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G MAX (pA)	$\lvert V_{GS_1} - V_{GS_2} \rvert$ MAX (mV)
2N3956	-50	1	-50	15
2N3957	-50	1	-50	20
2N3958	-50	1	-50	25

TO-71



BOTTOM VIEW



1 SOURCE 1
2 DRAIN 1
3 GATE 1
4 SOURCE 2
5 DRAIN 2
6 GATE 2

SIMILAR PRODUCTS

- Low Noise, See U401 Series
- Low Leakage, See U421 Series
- High Gain, See 2N5911 Series
- Chips, Order 2N395XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMIT	UNITS
Gate-Drain Voltage		V_{GD}	-50	V
Gate-Source Voltage		V_{GS}	-50	
Forward Gate Current		I_G	50	mA
Power Dissipation	Per Side	P_D	250	mW
	Total		500	
Power Derating	Per Side		2.86	mW/°C
	Total		4.3	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature		T_{stg}	-65 to 200	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

ELECTRICAL CHARACTERISTICS[1]			LIMITS							
				2N3956		2N3957		2N3958		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-57	-50		-50		-50		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 20 V, I_D = 1 nA	-2	-1	-4.5	-1	-4.5	-1	-4.5	V
Saturation Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	3	0.5	5	0.5	5	0.5	5	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -30 V, V_{DS} = 0 V	-10		-100		-100		-100	pA
		V_{GS} = -30 V, V_{DS} = 0 V, T_A = 150°C	-20		-500		-500		-500	nA
Gate Operating Current	I_G	V_{DS} = 20 V, I_D = 200 µA	-5		-50		-50		-50	pA
		V_{DS} = 20 V, I_D = 200 µA, T_A = 125°C	-0.8		-250		-250		-250	nA
Gate-Source Voltage	V_{GS}	V_{DS} = 20 V, I_D = 50 µA	-1.7		-4.2		-4.2		-4.2	V
		V_{DS} = 20 V, I_D = 200 µA	-1.5	-0.5	-4	-0.5	-4	-0.5	-4	V
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7		2		2		2	V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 kHz	2.5	1	3	1	3	1	3	mS
		V_{DS} = 20 V, V_{GS} = 0 V, f = 200 MHz	2	1		1		1		mS
Common-Source Output Conductance	g_{os}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 kHz	7		35		35		35	µS
Drain-Gate Capacitance	C_{dgo}	V_{DG} = 10 V, I_S = 0 mA, f = 1 MHz	1		1.5		1.5		1.5	pF
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	3		4		4		4	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	1		1.2		1.2		1.2	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 200 µA, f = 1 kHz	10							$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DS} = 20 V, V_{GS} = 0 V, f = 100 Hz, R_G = 10 MΩ	<0.1		0.5		0.5		0.5	dB
MATCHING										
Differential Gate-Source Voltage	$\lvert V_{GS1}-V_{GS2}\rvert$	V_{DS} = 20 V, I_D = 200 µA	10		15		20		25	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	V_{DS} = 20 V, I_D = 200 µA, T = -55 to 25°C	25		50		75		100	µV/°C
		V_{DS} = 20 V, I_D = 200 µA, T = 25 to 125°C	25		50		75		100	µV/°C
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 20 V, V_{GS} = 0 V	0.97	0.95	1	0.9	1	0.85	1	
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V_{DS} = 20 V, I_D = 200 µA, f = 1 kHz	0.97	0.95	1	0.9	1	0.85	1	
Differential Gate Current	$\lvert I_{G1}-I_{G2}\rvert$	V_{DS} = 20 V, I_D = 200 µA, T_A = 125°C	0.2		10		10		10	nA

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

4

2N4091 SERIES – JANTX, JANTXV

Siliconix incorporated

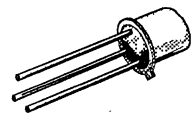
N-Channel JFET

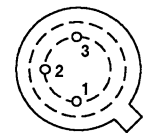
The 2N4091 Series is an all-purpose JFET analog switch which offers low on-resistance, good isolation and very fast switching. Its JAN, JANTX, and JANTXV certification make this device a perfect choice for military designs, as qualified devices can be purchased without cumbersome source-control documentation.

For further design information please consult the typical performance curves NCB which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	$I_{D(OFF)}$ MAX (pA)	t_{ON} MAX (ns)
2N4091	–10	30	200	25
2N4092	–7	50	200	35
2N4093	–5	80	200	60

TO-18 BOTTOM VIEW





1 SOURCE
2 DRAIN
3 GATE

SIMILAR PRODUCTS

- TO-92, See PN4091 Series
- SOT-23, See SST4091 Series
- Duals, See 2N5564 Series
- Chips, Order 2N409XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	–40	V
Gate-Source Voltage	V_{GS}	–40	
Gate Current	I_G	10	mA
Power Dissipation (Case 25°C)	P_D	1800	mW
Power Derating		10	mW/°C
Operating Junction Temperature	T_J	–55 to 200	°C
Storage Temperature	T_{stg}	–65 to 200	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

2N4091 SERIES – JANTX, JANTXV

ELECTRICAL CHARACTERISTICS [1]				LIMITS							
					2N4091		2N4092		2N4093		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC											
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V		-55	-40		-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 20 V, I_D = 1 nA			-5	-10	-2	-7	-1	-5	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V			30		15		8		mA
Drain Reverse Current	I_{DGO}	V_{DG} = 20 V, I_S = 0 V		-5		-200		-200		-200	pA
			T_A = 150°C	-10		-400		-400		-400	nA
Gate Operating Current[4]	I_G	V_{DG} = 15 V, I_D = 10 mA		-5							
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 20 V	V_{GS} = -6 V	5						200	pA
			V_{GS} = -8 V	5				200			
			V_{GS} = -12 V	5		200					
		V_{DS} = 20 V, T_A = 150°C	V_{GS} = -6 V	10						400	nA
			V_{GS} = -8 V	10				400			
			V_{GS} = -12 V	10		400					
Drain-Source On-Voltage	$V_{DS(ON)}$	V_{GS} = 0 V	I_D = 2.5 mA	0.15						0.2	V
			I_D = 4 mA	0.15				0.2			
			I_D = 6.6 mA	0.15		0.2					
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA				30		50		80	Ω
Gate-Source Forward Voltage[4]	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V		0.7							V
DYNAMIC											
Common-Source Forward Transconductance[4]	g_{fs}	V_{DG} = 20 V, I_D = 1 mA, f = 1 kHz		6							mS
Common-Source Output Conductance[4]	g_{os}			25							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V, f = 1 kHz				30		50		80	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz		13		16		16		16	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} = -20 V, f = 1 MHz		3.5		5		5		5	
Equivalent Input Noise Voltage[4]	$\bar{e}_n$	V_{DG} = 10 V, I_D = 10 mA, f = 1 kHz		3							$nV/\sqrt{Hz}$
SWITCHING											
Turn-on Time	$t_{d(ON)}$	V_{DD} = 3 V, $V_{GS(ON)}$ = 0 V		2		15		15		20	ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L		2		10		20		40	
Turn-off Time	t_{OFF}	2N4091 6.6 mA -12 V 425 Ω 2N4092 4 mA -8 V 700 Ω 2N4093 2.5 mA -6 V 1120 Ω		20		40		60		80	

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µS, duty cycle ≤ 3%.
4. This parameter not registered with JEDEC.

2N4117 SERIES

Siliconix incorporated

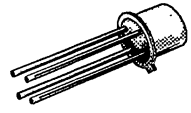
N-Channel JFET

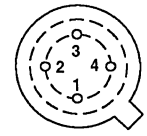
The 2N4117 and 2N4117A Series are n-channel JFETs designed to provide ultra-high input impedance. The 2N4117 features I_{GSS} of 10 pA maximum while the 2N4117A Series is specified with a 1 pA limit and typically operates at 0.2 pA. These devices, therefore, make perfect choices for use as sensitive front-end amplifiers in applications such as microphones, smoke detectors, and precision test equipment. Additionally, its hermetically sealed TO-72 package allows full military processing per MIL-S-19500. (See Section 1.)

For additional design information please consult performance curves NT which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (μS)	I_{DSS} MAX (mA)
2N4117	-1.8	-40	70	0.09
2N4118	-3	-40	80	0.24
2N4119	-6	-40	100	0.60
2N4117A	-1.8	-40	70	0.09
2N4118A	-3	-40	80	0.24
2N4119A	-6	-40	100	0.60

TO-72 **BOTTOM VIEW**





1 SOURCE
2 DRAIN
3 GATE
4 CASE

SIMILAR PRODUCTS

- TO-92, See PN4117 Series
- SOT-23, See SST4117 Series
- Dual, See U421 Series
- Chips, Order 2N411XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-40	V
Gate-Source Voltage	V_{GS}	-40	
Gate Current	I_G	50	mA
Power Dissipation	P_D	300	mW
Power Derating		2	mW/°C
Operating Junction Temperature	T_J	-55 to 175	°C
Storage Temperature	T_{stg}	-65 to 175	
Lead Temperature (1/16" from case for 10 seconds)	T_L	255	

ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				2N4117		2N4118		2N4119		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-70	-40		-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA		-0.6	-1.8	-1	-3	-2	-6	V
Saturation Drain Current [3]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V		0.03	0.09	0.08	0.24	0.2	0.6	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-0.2		-10		-10		-10	pA
		T_A = 150°C	-0.4		-25		-25		-25	nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 30 µA	-0.2							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 10 V, V_{GS} = -8 V	0.2							pA
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz		70	210	80	250	100	330	µS
Common-Source Output Conductance	g_{os}				3		5		10	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	1.2		3		3		3	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		0.3		1.5		1.5		1.5	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	15							$nV/\sqrt{Hz}$

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

4

Siliconix incorporated

ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				2N4117A		2N4118A		2N4119A		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-70	-40		-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA		-0.6	-1.8	-1	-3	-2	-6	V
Saturation Drain Current [3]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V		0.015	0.09	0.08	0.24	0.2	0.6	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-0.2		-1		-1		-1	pA
		T_A = 150°C	-0.4		-2.5		-2.5		-2.5	nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 30 µA	-0.2							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 10 V, V_{GS} = -8 V	0.2							pA
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz		70	210	80	250	100	330	µS
Common-Source Output Conductance	g_{os}				3		5		10	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	1.2		3		3		3	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		0.3		1.5		1.5		1.5	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	15							$nV/\sqrt{Hz}$

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

Siliconix incorporated

2N4220 SERIES

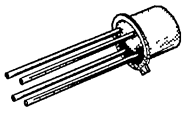
N-Channel JFETs

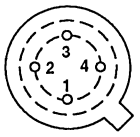
The 2N4220 Series of multi-purpose JFETs is designed for a wide range of applications. It features extremely low gate leakage and capacitance, and when coupled with its high gain, the 2N4220 Series will make a perfect broad band amplifier. The 2N4220A Series features a guaranteed noise figure of 2.5 dB. For military designs, this series is available with full high-rel processing. (See Section 1.)

For further design information please consult the typical performance curves NRL which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
2N4220	-4	-30	1	3
2N4221	-6	-30	2	6
2N4222	-8	-30	2.5	15
2N4220A	-4	-30	1	3
2N4221A	-6	-30	2	6
2N4222A	-8	-30	2.5	15

TO-72 BOTTOM VIEW





1 DRAIN
2 SOURCE
3 GATE
4 CASE

SIMILAR PRODUCTS

- TO-92, See J201 Series
- SOT-23, See SST201 Series
- Chips, Order 2N422XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-30	V
Gate-Source Voltage	V_{GS}	-30	
Gate Current	I_G	10	mA
Drain Current	I_D	15	
Power Dissipation	P_D	300	mW
Power Derating		2	mW/°C
Operating Junction Temperature	T_J	-55 to 175	°C
Storage Temperature	T_{stg}	-65 to 200	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

Siliconix incorporated

ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				2N4220		2N4221		2N4222		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = −10 µA, V_{DS} = 0 V	−57	−30		−30		−30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 0.1 nA			−4		−6		−8	
Saturation Drain Current [3]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		0.5	3	2	6	5	15	mA
Gate Reverse Current	I_{GSS}	V_{GS} = −15 V, V_{DS} = 0 V	−2		−100		−100		−100	pA
		V_{GS} = −15 V, V_{DS} = 0 V, T_A = 150°C	−4		−100		−100		−100	nA
Gate Operating Current [4]	I_G	V_{DG} = 15 V, I_D = 0.1 mA	−2							pA
Drain Cutoff Current [4]	$I_{D(OFF)}$	V_{DS} = 10 V, V_{GS} = −10 V	2							
Gate-Source Voltage	V_{GS}	V_{DS} = 15 V, I_D = 50 µA	−0.8	−0.5	−2.5					V
		V_{DS} = 15 V, I_D = 200 µA	−1.5			−1	−5			
		V_{DS} = 15 V, I_D = 500 µA	−3.5					−2	−6	
Gate-Source Forward Voltage [4]	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 kHz		1	4	2	5	2.5	6	mS
Common-Source Output Conductance	g_{os}				10		20		40	µS
Common-Source Forward Transmittance	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V, f = 100 MHz		750		750		750		
Common-Source Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	5		6		6		6	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.5		2		2		2	
Equivalent Input Noise Voltage [4]	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	6							$nV/\sqrt{Hz}$

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.
4. This parameter not registered with JEDEC.

ELECTRICAL CHARACTERISTICS[1]			LIMITS							
				2N4220A		2N4221A		2N4222A		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -10 µA, V_{DS} = 0 V	-57	-30		-30		-30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 0.1 nA			-4		-6		-8	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		0.5	3	2	6	5	15	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-2		-100		-100		-100	pA
		T_A = 150°C	-4		-100		-100		-100	nA
Gate Operating Current[4]	I_G	V_{DG} = 15 V, I_D = 0.1 mA	-2							pA
Drain Cutoff Current[4]	$I_{D(OFF)}$	V_{DS} = 10 V, V_{GS} = -10 V	2							pA
Gate-Source Voltage	V_{GS}	V_{DS} = 15 V, I_D = 50 µA	-0.8	-0.5	-2.5					V
		I_D = 200 µA	-1.5			-1	-5			
		I_D = 500 µA	-3.5					-2	-6	
Gate-Source Forward Voltage[4]	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 kHz		1	4	2	5	2.5	6	mS
Common-Source Output Conductance	g_{os}				10		20		40	µS
Common-Source Forward Transmittance	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V, f = 100 MHz		750		750		750		µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	5		6		6		6	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.5		2		2		2	pF
Equivalent Input Noise Voltage[4]	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	6							$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DS} = 15 V, V_{GS} = 0 V, f = 100 Hz, R_G = 1 MΩ, BW = 6 Hz			2.5		2.5		2.5	dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.
4. This parameter not registered with JEDEC.

4

2N4338 SERIES

Siliconix incorporated

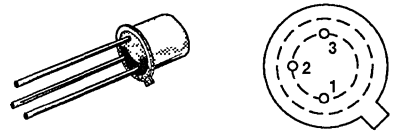
N-Channel JFETs

The 2N4338 Series of n-channel JFETs is designed for sensitive amplifier stages at low to mid frequencies. It features low cut-off voltages to accommodate low-level power supplies and low leakage for improved system accuracy. The 2N4338 and 2N4339 are ideal for low current, low battery operation. With their 1 dB max. noise figure at 1 kHz, system sensitivity will be excellent. Finally, the 2N4338 Series' TO-18 package is hermetically sealed and suitable for military processing. (See Section 1.)

For further design information please consult the typical performance curves NPA which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
2N4338	-1	-50	0.6	0.6
2N4339	-1.8	-50	0.8	1.5
2N4340	-3	-50	1.3	3.6
2N4341	-6	-50	2	9

TO-18 **BOTTOM VIEW**



1 SOURCE
2 DRAIN
3 GATE & CASE

SIMILAR PRODUCTS

- TO-92, See J201 Series
- SOT-23, See SST201 Series
- Chips, Order 2N433XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-50	V
Gate-Source Voltage	V_{GS}	-50	
Gate Current	I_G	50	mA
Power Dissipation	P_D	300	mW
Power Derating		2	mW/°C
Operating Junction Temperature	T_J	-55 to 175	°C
Storage Temperature	T_{stg}	-65 to 200	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS[1]			LIMITS					
				2N4338		2N4339		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-57	-50		-50		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 0.1 µA		-0.3	-1	-0.6	-1.8	
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		0.2	0.6	0.5	1.5	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -30 V, V_{DS} = 0 V	-2		-100		-100	pA
		V_{GS} = -30 V, V_{DS} = 0 V, T_A = 150°C	-4		-100		-100	nA
Gate Operating Current[4]	I_G	V_{DG} = 15 V, I_D = 0.1 mA	-2					pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 15 V, V_{GS} = -5 V	2		50		50	
Gate-Source Forward Voltage[4]	$V_{GS(f)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 kHz		0.6	1.8	0.8	2.4	mS
Common-Source Output Conductance	g_{os}				5		15	µS
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{DS} = 0 V, V_{GS} = 0 V, f = 1 kHz			2500		1700	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	5		7		7	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.5		3		3	
Equivalent Input Noise Voltage[4]	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	6					$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 kHz, R_G = 1 MΩ	<0.01		1		1	dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.
4. This parameter not registered with JEDEC.

4

Siliconix incorporated

ELECTRICAL CHARACTERISTICS[1]				LIMITS					
					2N4340		2N4341		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[2]	MIN	MAX	MIN	MAX	UNIT
STATIC									
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V		-57	-50		-50		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 0.1 µA			-1	-3	-2	-6	
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V			1.2	3.6	3	9	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -30 V, V_{DS} = 0 V		-2		-100		-100	pA
			T_A = 150°C	-4		-100		-100	nA
Gate Operating Current[4]	I_G	V_{DG} = 15 V, I_D = 0.1 mA		-2					pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 15 V	V_{GS} = -5 V	2		50			
			V_{GS} = -10 V	3				70	
Gate-Source Forward Voltage[4]	$V_{GS(f)}$	I_G = 1 mA, V_{DS} = 0 V		0.7					V
DYNAMIC									
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 kHz			1.3	3	2	4	mS
Common-Source Output Conductance	g_{os}					30		60	µS
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{DS} = 0 V, V_{GS} = 0 V, f = 1 kHz				1500		800	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz		5		7		7	pF
Common-Source Reverse Transfer Capacitance	C_{rss}			1.5		3		3	
Equivalent Input Noise Voltage[4]	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz		6					$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 kHz, R_G = 1 MΩ		<0.01		1		1	dB

NOTES:
1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.
4. This parameter not registered with JEDEC.

2N4391 SERIES

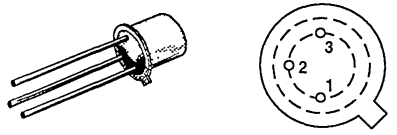
N-Channel JFET

The 2N4391 Series features many of the superior characteristics of JFETs. Its low on-resistance and fast switching make it a good choice for demanding analog switching applications, while its high-gain, low-noise, and impressive frequency response make it the choice for specialized amplifier circuits. This series also features a hermetically sealed TO-18 can which can be processed per MIL-S-19500. (See Section 1).

For additional design information please consult the typical performance curves NCB which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	$I_{D(OFF)}$ MAX (pA)	t_{ON} MAX (ns)
2N4391	-10	30	100	20
2N4392	-5	60	100	20
2N4393	-3	100	100	20

TO-18 BOTTOM VIEW



1 SOURCE
2 DRAIN
3 GATE

SIMILAR PRODUCTS

- TO-92, See PN4391 Series
- SOT-23, See SST4391 Series
- Duals, See 2N5564 Series
- Chips, Order 2N439XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-40	V
Gate-Source Voltage	V_{GS}	-40	
Gate Current	I_G	50	mA
Power Dissipation (Case 25°C)	P_D	1800	mW
Power Derating		10	mW/°C
Operating Junction Temperature	T_J	-55 to 200	°C
Storage Temperature	T_{stg}	-65 to 200	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

Siliconix incorporated

ELECTRICAL CHARACTERISTICS [1]				LIMITS							
					2N4391		2N4392		2N4393		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC											
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V		-55	-40		-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 20 V, I_D = 1 nA			-4	-10	-2	-5	-0.5	-3	V
Saturation Drain Current [3]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V			50	150	25	75	5	30	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V		-5		-100		-100		-100	pA
			T_A = 150°C	-13		-200		-200		-200	nA
Gate Operating Current [4]	I_G	V_{DG} = 15 V, I_D = 10 mA		-5							
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 20 V	V_{GS} = -5 V	5						100	pA
			V_{GS} = -7 V	5				100			
			V_{GS} = -12 V	5		100					
		V_{DS} = 20 V, T_A = 150°C	V_{GS} = -5 V	13						200	nA
			V_{GS} = -7 V	13				200			
			V_{GS} = -12 V	13		200					
Drain-Source On-Voltage	$V_{DS(ON)}$	V_{GS} = 0 V	I_D = 3 mA	0.25						0.4	V
			I_D = 6 mA	0.3				0.4			
			I_D = 12 mA	0.35		0.4					
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA				30		60		100	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V		0.7		1		1		1	V
DYNAMIC											
Common-Source Forward Transconductance [4]	g_{fs}	V_{DG} = 20 V, I_D = 1 mA, f = 1 kHz		6							mS
Common-Source Output Conductance [4]	g_{os}			25							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 mA, f = 1 kHz				30		60		100	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz		12		14		14		14	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, f = 1 MHz	V_{GS} = -5 V	3.3						3.5	
			V_{GS} = -7 V	3.2				3.5			
			V_{GS} = -12 V	2.8		3.5					
Equivalent Input Noise Voltage [4]	$\bar{e}_n$	V_{DG} = 10 V, I_D = 10 mA, f = 1 kHz		3.0							$nV/\sqrt{Hz}$
SWITCHING											
Turn-on Time	$t_{d(ON)}$	V_{DD} = 10 V, $V_{GS(ON)}$ = 0 V		2		15		15		15	ns
	t_r	P/N	$I_{D(ON)}$ $V_{GS(OFF)}$ R_L	2		5		5		5	
Turn-off Time	$t_{d(OFF)}$	2N4391	12 mA -12 V 800 Ω	6		20		35		50	
	t_f	2N4392	6 mA -7 V 1600 Ω	13		15		20		30	
		2N4393	3 mA -5 V 3000 Ω								

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.
4. This parameter not registered with JEDEC.

Siliconix incorporated

2N4416 SERIES

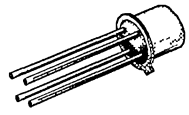
N-Channel JFETs

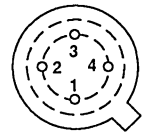
The 2N4416 and 2N4416A are n-channel JFETs designed to provide high-performance amplification, especially at high-frequency. These parts feature low noise figure (4 dB max @ 400 MHz), high gain (10 dB min @ 400 MHz) and provide wide bandwidth. Its TO-72 hermetically sealed package is available with full military processing. (See Section 1.)

For additional design information please see performance curves NH, which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
2N4416	-6	-30	4.5	15
2N4416A	-6	-35	4.5	15

TO-72 BOTTOM VIEW





1 SOURCE
2 DRAIN
3 GATE
4 SUBSTRATE

SIMILAR PRODUCTS

- TO-92, See PN4416
- SOT-23, See SST4416
- Chips, Order 2N4416CHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT		UNITS
		2N4416	2N4416A	
Gate-Drain Voltage	V_{GD}	-30	-35	V
Gate-Source Voltage	V_{GS}	-30	-35	
Gate Current	I_G	10		mA
Power Dissipation	P_D	300		mW
Power Derating		1.7		mW/°C
Operating Junction Temperature	T_J	-55 to 150		°C
Storage Temperature	T_{stg}	-65 to 200		
Lead Temperature (1/16" from case for 10 seconds)	T_L	300		

4

ELECTRICAL CHARACTERISTICS[1]			LIMITS					
				2N4416		2N4416A		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-36	-30		-35		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 1 nA	-3		-6	-2.5	-6	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V	10	5	15	5	15	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-2		-100		-100	pA
		T_A = 150°C	-4		-100		-100	nA
Gate Operating Current[4]	I_G	V_{DG} = 10 V, I_D = 1 mA	-20					pA
Drain Cutoff Current[4]	$I_{D(OFF)}$	V_{DS} = 10 V, V_{GS} = -6 V	2					pA
Drain-Source On-Resistance[4]	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA	150					Ω
Gate-Source Forward Voltage[4]	$V_{GS(f)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					V
DYNAMIC								
Common-Source Forward Transconductance[3]	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 kHz	6	4.5	7.5	4.5	7.5	mS
Common-Source Output Conductance[3]	g_{os}		15		50		50	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	2.2		4		4	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		0.7		0.8		0.8	pF
Common-Source Output Capacitance	C_{oss}		1		2		2	pF
Equivalent Input Noise Voltage[4]	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 100 Hz	9					$nV/\sqrt{Hz}$

ELECTRICAL CHARACTERISTICS[1]			LIMITS					
				100 MHz		400 MHz		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	UNIT
HIGH-FREQUENCY								
Common-Source Input Conductance	g_{iss}	V_{DS} = 15 V, V_{GS} = 0 V			100		1000	µS
Common-Source Input Susceptance	b_{iss}				2500		10,000	µS
Common-Source Output Capacitance	g_{oss}				75		100	µS
Common-Source Output Susceptance	b_{oss}				1000		4000	µS
Common-Source Forward Transconductance	g_{fs}					4000		µS
Common-Source Power Gain	G_{ps}	V_{DS} = 15 V, I_D = 5 mA		18		10		dB
Noise Figure	NF	V_{DS} = 15 V, I_D = 5 mA, R_G = 1 kΩ			2		4	dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.
4. This parameter not registered with JEDEC.

Siliconix incorporated

2N4856 SERIES – JANTX, JANTXV

N-Channel JFET

The 2N4856 Series is an all-purpose JFET analog switch which offers low on-resistance, good isolation and very fast switching. Its JAN, JANTX, and JANTXV certification make this device a perfect choice for military designs, as qualified devices can be purchased without cumbersome source-control documentation.

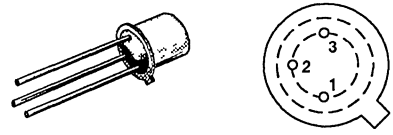
For additional design information please consult the typical performance curves NCB, which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	$I_{D(OFF)}$ MAX (pA)	t_{ON} MAX (ns)
2N4856	–10	25	250	9
2N4857	–6	40	250	10
2N4858	–4	60	250	20
2N4859	–10	25	250	9
2N4860	–6	40	250	10
2N4861	–4	60	250	20

SIMILAR PRODUCTS

- TO-92, J111 Series
- SOT-23, SST111 Series
- Dual, 2N5564 Series
- Chips, Order 2N485XCHP

TO-18 BOTTOM VIEW



1 SOURCE
2 DRAIN
3 GATE

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT		UNITS
		2N4856-58	2N4859-61	
Gate-Drain Voltage	V_{GD}	–40	–30	V
Gate-Source Voltage	V_{GS}	–40	–30	
Gate Current	I_G	50		mA
Power Dissipation (25°C Case)	P_D	1800		mW
Power Derating		10		mW/°C
Operating Junction Temperature	T_J	–55 to 200		°C
Storage Temperature	T_{stg}	–65 to 200		
Lead Temperature (1/16" from case for 10 seconds)	T_L	300		

4

ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				2N4856		2N4857		2N4858		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-55	-40		-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 0.5 nA		-4	-10	-2	-6	-0.8	-4	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		50		20	100	8	80	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-5		-250		-250		-250	pA
		V_{GS} = -20 V, V_{DS} = 0 V, T_A = 150°C	-13		-500		-500		-500	nA
Gate Operating Current[4]	I_G	V_{DG} = 15 V, I_D = 10 mA	-5							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 15 V, V_{GS} = -10 V	5		250		250		250	pA
		V_{DS} = 15 V, V_{GS} = -10 V, T_A = 150°C	13		500		500		500	nA
Drain-Source On-Voltage	$V_{DS(ON)}$	V_{GS} = 0 V, I_D = 5 mA	0.25						0.5	V
		V_{GS} = 0 V, I_D = 10 mA	0.35				0.5			V
		V_{GS} = 0 V, I_D = 20 mA	0.5		0.75					V
Drain-Source On-Resistance[4]	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA			25		40		60	Ω
Gate-Source Forward Voltage[4]	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance[4]	g_{fs}	V_{DG} = 20 V, I_D = 1 mA, f = 1 kHz	6							mS
Common-Source Output Conductance[4]	g_{os}		25							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V, f = 1 kHz			25		40		60	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = -10 V, f = 1 MHz	7		18		18		18	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		3		8		8		8	pF
Equivalent Input Noise Voltage[4]	$\bar{e}_n$	V_{DG} = 10 V, I_D = 10 mA, f = 1 kHz	3							$nV/\sqrt{Hz}$
SWITCHING										
Turn-on Time	$t_{d(ON)}$	V_{DD} = 10 V, $V_{GS(ON)}$ = 0 V	2		6		6		10	ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	2		3		4		10	ns
Turn-off Time	$t_{(OFF)}$	2N4856 20 mA -10 V 464 Ω 2N4857 10 mA -6 V 953 Ω 2N4858 5 mA -4 V 1910 Ω	19		25		50		100	ns

NOTES:
1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 100 µS, duty cycle ≤ 10%.
4. This parameter not registered with JEDEC.

2N4856 SERIES – JANTX, JANTXV

ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				2N4859		2N4860		2N4861		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-55	-30		-30		-30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 0.5 nA		-4	-10	-2	-6	-0.8	-4.0	V
Saturation Drain Current [3]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		50		20	100	8	80	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-5		-250		-250		-250	pA
		T_A = 150°C	-13		-500		-500		-500	nA
Gate Operating Current [4]	I_G	V_{DG} = 15 V, I_D = 10 mA	-5							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 15 V, V_{GS} = -10 V	5		250		250		250	pA
		V_{DS} = 15 V, V_{GS} = -10 V, T_A = 150°C	13		500		500		500	nA
Drain-Source On-Voltage	$V_{DS(ON)}$	V_{GS} = 0 V, I_D = 5 mA	0.25						0.5	V
		V_{GS} = 0 V, I_D = 10 mA	0.35				0.5			V
		V_{GS} = 0 V, I_D = 20 mA	0.5		0.75					V
Drain-Source On-Resistance [4]	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA			25		40		60	Ω
Gate-Source Forward Voltage [4]	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance [4]	g_{fs}	V_{DG} = 20 V, I_D = 1 mA, f = 1 kHz	6							mS
Common-Source Output Conductance [4]	g_{os}		25							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V, f = 1 kHz			25		40		60	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = -10 V, f = 1 MHz	7		18		18		18	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		3		8		8		8	pF
Equivalent Input Noise Voltage [4]	$\bar{e}_n$	V_{DG} = 10 V, I_D = 10 mA, f = 1 kHz	3							$nV/\sqrt{Hz}$
SWITCHING										
Turn-on Time	$t_{d(ON)}$	V_{DD} = 10 V, $V_{GS(ON)}$ = 0 V	2		6		6		10	ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	2		3		4		10	ns
Turn-off Time	$t_{(OFF)}$	2N4859 20 mA -10 V 464 Ω 2N4860 10 mA -6 V 953 Ω 2N4861 5 mA -4 V 1910 Ω	19		25		50		100	ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 100 µS, duty cycle ≤ 10%.
4. This parameter not registered with JEDEC.

4

2N4856A SERIES

Siliconix incorporated

N-Channel JFET

The 2N4856A Series is an all-purpose JFET analog switch which offers low on-resistance and good isolation. Although very similar to the 2N4856 Series, the 2N4856A Series features even lower capacitance and faster switching. Finally, its hermetically sealed TO-18 package allows full military processing. (See Section 1.)

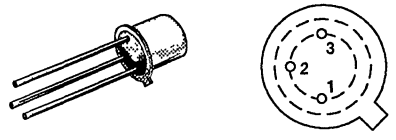
For additional design information please consult the typical performance curves NCB, which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	$I_{D(OFF)}$ MAX (pA)	t_{ON} MAX (ns)
2N4856A	–10	25	250	8
2N4857A	–6	40	250	10
2N4858A	–4	60	250	16
2N4859A	–10	25	250	8
2N4860A	–6	40	250	10
2N4861A	–4	60	250	16

SIMILAR PRODUCTS

- TO-92, J111 Series
- SOT-23, SST111 Series
- Dual, 2N5564 Series
- Chips, Order 2N485XACHP

TO-18 BOTTOM VIEW



1 SOURCE
2 DRAIN
3 GATE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT		UNITS
		2N4856A-58A	2N4859A-61A	
Gate-Drain Voltage	V_{GD}	–40	–30	V
Gate-Source Voltage	V_{GS}	–40	–30	
Gate Current	I_G	50		mA
Power Dissipation (25°C Case)	P_D	1800		mW
Power Derating		10		mW/°C
Operating Junction Temperature	T_J	–55 to 200		°C
Storage Temperature	T_{stg}	–65 to 200		
Lead Temperature (1/16" from case for 10 seconds)	T_L	300		

ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				2N4856A		2N4857A		2N4858A		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-55	-40		-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 0.5 nA		-4	-10	-2	-6	-0.8	-4	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		50		20	100	8	80	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-5		-250		-250		-250	pA
		V_{DS} = 0 V, T_A = 150°C	-13		-500		-500		-500	nA
Gate Operating Current[4]	I_G	V_{DG} = 15 V, I_D = 10 mA	-5							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 15 V, V_{GS} = -10 V	5		250		250		250	pA
		V_{DS} = 15 V, V_{GS} = -10 V, T_A = 150°C	13		500		500		500	nA
Drain-Source On-Voltage	$V_{DS(ON)}$	V_{GS} = 0 V, I_D = 5 mA	0.25						0.5	V
		V_{GS} = 0 V, I_D = 10 mA	0.35				0.5			V
		V_{GS} = 0 V, I_D = 20 mA	0.5		0.75					V
Drain-Source On-Resistance[4]	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA			25		40		60	Ω
Gate-Source Forward Voltage[4]	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance[4]	g_{fs}	V_{DG} = 20 V, I_D = 1 mA, f = 1 kHz	6							mS
Common-Source Output Conductance[4]	g_{os}		25							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V, f = 1 kHz			25		40		60	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = -10 V, f = 1 MHz	7		10		10		10	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		3		4		3.5		3.5	pF
Equivalent Input Noise Voltage[4]	$\bar{e}_n$	V_{DG} = 10 V, I_D = 10 mA, f = 1 kHz	3							$nV/\sqrt{Hz}$
SWITCHING										
Turn-on Time	$t_{d(ON)}$	V_{DD} = 10 V, $V_{GS(ON)}$ = 0 V	2		5		6		8	ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	2		3		4		8	ns
Turn-off Time	$t_{(OFF)}$	2N4856A 20 mA -10 V 464 Ω 2N4857A 10 mA -6 V 953 Ω 2N4858A 5 mA -4 V 1910 Ω	19		20		40		80	ns

NOTES:
1. T_A = 25°C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 100 µS, duty cycle ≤ 10%.
4. This parameter not registered with JEDEC.

4

Siliconix incorporated

ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				2N4859A		2N4860A		2N4861A		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-55	-30		-30		-30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 0.5 nA		-4	-10	-2	-6	-0.8	-4	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		50		20	100	8	80	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-5		-250		-250		-250	pA
		T_A = 150°C	-13		-500		-500		-500	nA
Gate Operating Current[4]	I_G	V_{DG} = 15 V, I_D = 10 mA	-5							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 15 V, V_{GS} = -10 V	5		250		250		250	pA
		V_{DS} = 15 V, V_{GS} = -10 V, T_A = 150°C	13		500		500		500	nA
Drain-Source On-Voltage	$V_{DS(ON)}$	V_{GS} = 0 V, I_D = 5 mA	0.25						0.5	V
		V_{GS} = 0 V, I_D = 10 mA	0.35				0.5			V
		V_{GS} = 0 V, I_D = 20 mA	0.5		0.75					V
Drain-Source On-Resistance[4]	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA			25		40		60	Ω
Gate-Source Forward Voltage[4]	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance[4]	g_{fs}	V_{DG} = 20 V, I_D = 1 mA, f = 1 kHz	6							mS
Common-Source Output Conductance[4]	g_{os}		25							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V, f = 1 kHz			25		40		60	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = -10 V, f = 1 MHz	7		10		10		10	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		3		4		3.5		3.5	pF
Equivalent Input Noise Voltage[4]	$\bar{e}_n$	V_{DG} = 10 V, I_D = 10 mA, f = 1 kHz	3							$nV/\sqrt{Hz}$
SWITCHING										
Turn-on Time	$t_{d(ON)}$	V_{DD} = 10 V, $V_{GS(ON)}$ = 0 V	2		5		6		8	ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	2		3		4		8	ns
Turn-off Time	$t_{(OFF)}$	2N4859A 20 mA -10 V 464 Ω 2N4860A 10 mA -6 V 953 Ω 2N4861A 5 mA -4 V 1910 Ω	19		20		40		80	ns

NOTES:
1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 100 µS, duty cycle ≤ 10%.
4. This parameter not registered with JEDEC.

2N4867 SERIES

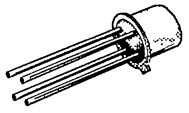
N-Channel JFETs

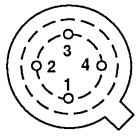
The 2N4867 Series of n-channel JFETs is designed for sensitive amplifier stages at low to mid frequencies. For applications requiring the lowest possible noise, the 2N4867A Series features $\bar{e}_n$ of 10 nV/$\sqrt{Hz}$ @ 10 Hz. Additionally, this series features low cut-off voltages to accommodate low-level power supplies and low leakage for improved system accuracy. Specifically the 2N4867 and 2N4868 are ideal for low current, low battery operation. With 1 dB max. noise figure at 1 kHz, system sensitivity will be excellent. Finally, the 2N4867 Series' TO-72 package is hermetically sealed and suitable for military processing. (See Section 1.)

For further design information please consult the typical performance curves NPA which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
2N4867	-2	-40	0.7	1.2
2N4868	-3	-40	1	3
2N4869	-5	-40	1.3	7.5
2N4867A	-2	-40	0.7	1.2
2N4868A	-3	-40	1	3
2N4869A	-5	-40	1.3	7.5

TO-72 BOTTOM VIEW





1 SOURCE
2 DRAIN
3 GATE
4 CASE

SIMILAR PRODUCTS

- TO-18, See 2N4338 Series
- TO-92, See J201 Series
- SOT-23, See SST201 Series
- Chips, Order 2N486XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-40	V
Gate-Source Voltage	V_{GS}	-40	
Gate Current	I_G	50	mA
Power Dissipation	P_D	300	mW
Power Derating		1.7	mW/°C
Operating Junction Temperature	T_J	-55 to 150	°C
Storage Temperature	T_{stg}	-65 to 200	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

Siliconix incorporated

ELECTRICAL CHARACTERISTICS[1]				LIMITS							
					2N4867		2N4868		2N4869		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC											
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V		-57	-40		-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 20 V, I_D = 1 µA			-0.7	-2	-1	-3	-1.8	-5	
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V			0.4	1.2	1	3	2.5	7.5	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -30 V, V_{DS} = 0 V		-2		-250		-250		-250	pA
			T_A = 150°C	-4		-250		-250		-250	nA
Gate Operating Current[4]	I_G	V_{DG} = 15 V, I_D = 0.1 mA		-2							pA
Drain Cutoff Current[4]	$I_{D(OFF)}$	V_{DS} = 15 V, V_{GS} = -6 V		2							
Gate-Source Forward Voltage[4]	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V		0.7							V
DYNAMIC											
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 kHz			0.7	2	1	3	1.3	4	mS
Common-Source Output Conductance	g_{os}					1.5		4		10	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz		4.5		25		25		25	pF
Common-Source Reverse Transfer Capacitance	C_{rss}			1.3		5		5		5	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V	f = 10 Hz	14		20		20		20	$nV/\sqrt{Hz}$
			f = 1 kHz	6		10		10		10	
Noise Figure	NF	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz, R_G = 20 kΩ		0.5		1		1		1	dB

NOTES:
1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.
4. This parameter not registered with JEDEC.

ELECTRICAL CHARACTERISTICS[1]				LIMITS							
				2N4867A		2N4868A		2N4869A		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-57	-40		-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 20 V, I_D = 1 µA		-0.7	-2	-1	-3	-1.8	-5	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V		0.4	1.2	1	3	2.5	7.5	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -30 V, V_{DS} = 0 V	-2		-250		-250		-250	pA
		T_A = 150°C	-4		-250		-250		-250	nA
Gate Operating Current[4]	I_G	V_{DG} = 15 V, I_D = 0.1 mA	-2							pA
Drain Cutoff Current[4]	$I_{D(OFF)}$	V_{DS} = 15 V, V_{GS} = -6 V	2							pA
Gate-Source Forward Voltage[4]	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 kHz		0.7	2	1	3	1.3	4	mS
Common-Source Output Conductance	g_{os}				1.5		4		10	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	4.5		25		25		25	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.3		5		5		5	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 10 Hz	8		10		10		10	$nV/\sqrt{Hz}$
		f = 1 kHz	3.5		5		5		5	$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz, R_G = 20 kΩ	0.5		1		1		1	dB

NOTES:
1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.
4. This parameter not registered with JEDEC.

2N5114 SERIES

Siliconix incorporated

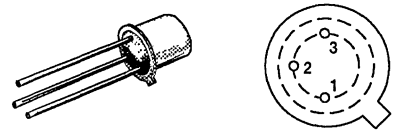
P-Channel JFETs

The 2N5114 Series is a p-channel JFET analog switch designed to complement our n-channel 2N4091 Series. They feature low on-resistance and good off-isolation as well as the fast switching associated with JFETs. They are housed in TO-18 hermetic packages and available with JAN, JANTX, or JANTXV level processing. (See 2N5114 JANTX data sheet.)

For additional design information please see performance curves PSCIA, which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	$I_{D(OFF)}$ MAX (pA)	t_{ON} MAX (ns)
2N5114	10	75	-500	16
2N5115	6	100	-500	30
2N5116	4	150	-500	60

TO-18 BOTTOM VIEW



1 SOURCE
2 DRAIN
3 GATE

SIMILAR PRODUCTS

- TO-92, See J174 Series
- SOT-23, See SST5114 Series
- Chips, Order 2N511XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	30	V
Gate-Source Voltage	V_{GS}	30	
Gate Current	I_G	50	mA
Power Dissipation	P_D	500	mW
Power Derating		3	mW/°C
Operating Junction Temperature	T_J	-55 to 200	°C
Storage Temperature	T_{stg}	-65 to 200	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

2N5114 SERIES

ELECTRICAL CHARACTERISTICS [1]				LIMITS							
					2N5114		2N5115		2N5116		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC											
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA, V_{DS} = 0 V		45	30		30		30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = −15 V, I_D = −1 nA			5	10	3	6	1	4	V
Saturation Drain Current[3]	I_{DSS}	V_{GS} = 0 V	V_{DS} = −18 V		−30	−90					mA
			V_{DS} = −15 V				−15	−60	−5	−25	mA
Gate Reverse Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V		5		500		500		500	pA
			T_A = 150°C	0.01		1		1		1	µA
Gate Operating[4] Current	I_G	V_{DG} = −15 V, I_D = −1 mA		−5							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = −15 V	V_{GS} = 12 V	−10		−500					pA
			V_{GS} = 7 V	−10				−500			pA
			V_{GS} = 5 V	−10						−500	pA
		V_{DS} = −15 V, T_A = 150°C	V_{GS} = 12 V	−0.02		−1					nA
			V_{GS} = 7 V	−0.02				−1			nA
			V_{GS} = 5 V	−0.02						−1	nA
Drain-Source On-Voltage	$V_{DS(ON)}$	V_{GS} = 0 V	I_D = −15 mA	−1.0		−1.3					V
			I_D = −7 mA	−0.7				−0.8			V
			I_D = −3 mA	−0.5						−0.6	V
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = −1 mA				75		100		150	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = −1 mA, V_{DS} = 0 V		−0.7		−1		−1		−1	V
DYNAMIC											
Common-Source[4] Forward Transconductance	g_{fs}	V_{DG} = −15 V, I_D = −1 mA, f = 1 kHz		4.5							mS
Common-Source[4] Output Conductance	g_{os}			20							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0, f = 1 kHz				75		100		150	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = −15 V, V_{GS} = 0 V, f = 1 MHz		20		25		25		25	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, f = 1 MHz	V_{GS} = 12 V	5		7					pF
			V_{GS} = 7 V	6				7			pF
			V_{GS} = 5 V	6						7	pF
Equivalent Input[4] Noise Voltage	$\bar{e}_n$	V_{DG} = −10 V, I_D = −1 mA, f = 1 kHz		20							$nV/\sqrt{Hz}$
SWITCHING											
Turn-on Time	$t_{d(ON)}$	$V_{GS(ON)}$ = 0 V				6		10		25	ns
	t_r	P/N V_{DD} $I_{D(ON)}$ $V_{GS(OFF)}$ R_L				10		20		35	ns
Turn-off Time	$t_{d(OFF)}$	2N5114 −10 V −15 mA 20 V 130 Ω				6		8		20	ns
	t_f	2N5115 −6 V −7 mA 12 V 900 Ω 2N5116 −6 V −3 mA 8 V 2000 Ω				15		30		60	ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.
4. This parameter not registered with JEDEC.

4

2N5114 SERIES – JANTX, JANTXV

Siliconix incorporated

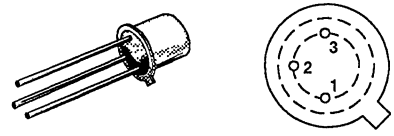
P-Channel JFETs

The 2N5114 Series is a p-channel JFET analog switch designed to complement our n-channel 2N4091 Series. They feature low on-resistance and good off-isolation as well as the fast switching associated with JFETs. They are housed in TO-18 hermetic packages and available with JAN, JANTX, or JANTXV level processing.

For additional design information please see performance curves PSCIA, which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	$I_{D(OFF)}$ MAX (pA)	t_{ON} MAX (ns)
2N5114	10	75	–500	16
2N5115	6	100	–500	30
2N5116	4	175	–500	42

TO-18 BOTTOM VIEW



1 SOURCE
2 DRAIN
3 GATE

SIMILAR PRODUCTS

- TO-92, See J174 Series
- SOT-23, See SST5114 Series
- Chips, Order 2N511XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	30	V
Gate-Source Voltage	V_{GS}	30	
Gate Current	I_G	50	mA
Power Dissipation	P_D	500	mW
Power Derating		3	mW/°C
Operating Junction Temperature	T_J	–55 to 200	°C
Storage Temperature	T_{stg}	–65 to 200	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

2N5114 SERIES – JANTX, JANTXV

ELECTRICAL CHARACTERISTICS [1]				LIMITS							
					2N5114		2N5115		2N5116		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC											
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA, V_{DS} = 0 V		45	30		30		30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = -15 V, I_D = -1 nA			5	10	3	6	1	4	
Saturation Drain Current[3]	I_{DSS}	V_{GS} = 0 V	V_{DS} = -18 V		-30	-90					mA
			V_{DS} = -15 V				-15	-60	-5	-25	
Gate Reverse Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V		5		500		500		500	pA
			T_A=150°C	0.01		1		1		1	µA
Gate Operating Current	I_G	V_{DG} = -15 V, I_D = -1 mA		5							
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = -15 V	V_{GS} = 12 V	-10		-500					pA
			V_{GS} = 7 V	-10				-500			
			V_{GS} = 5 V	-10						-500	
		V_{DS} = -15 V, T_A=150°C	V_{GS} = 12 V	-0.02		-1					nA
			V_{GS} = 7 V	-0.02				-1			
			V_{GS} = 5 V	-0.02						-1	
Drain-Source On-Voltage	$V_{DS(ON)}$	V_{GS} = 0 V	I_D = -15 mA	-1.0		-1.3					V
			I_D = -7 mA	-0.7				-0.8			
			I_D = -3 mA	-0.5						-0.6	
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = -1 mA				75		100		175	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = -1 mA, V_{DS} = 0 V		-0.7							V
DYNAMIC											
Common-Source Forward Transconductance	g_{fs}	V_{DG} = -15 V, I_D = -1 mA, f = 1 kHz		4.5							mS
Common-Source Output Conductance	g_{os}			20							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0, f = 1 kHz				75		100		175	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = -15 V, V_{GS} = 0 V, f = 1 MHz		20		25		25		27	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, f = 1 MHz	V_{GS} = 12 V	5		7					
			V_{GS} = 7 V	6				7			
			V_{GS} = 5 V	6						7	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = -10 V, I_D = -1 mA, f = 1 kHz		20							$nV/\sqrt{Hz}$
SWITCHING											
Turn-on Time	$t_{d(ON)}$	$V_{GS(ON)}$ = 0 V				6		10		12	ns
	t_r					10		20		30	
Turn-off Time	$t_{d(OFF)}$					6		8		10	
	t_f					15		30		50	

P/N	V_{DD}	$I_{D(ON)}$	$V_{GS(OFF)}$	R_L	R_G
2N5114	-10 V	-15 mA	20 V	430 Ω	100 Ω
2N5115	-6 V	-7 mA	12 V	900 Ω	220 Ω
2N5116	-6 V	-3 mA	8 V	2000 Ω	390 Ω

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

4

2N5196 SERIES

Siliconix incorporated

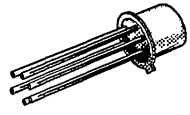
N-Channel JFET Pairs

The 2N5196 Series of monolithic JFET pairs is designed for high performance differential amplification for a wide range of precision test instrumentation applications. This series features tight matching specs, low gate leakage for accuracy, and wide dynamic range as I_G is guaranteed at V_{DG} = 20 V. Its TO-71 package is hermetically sealed and is available with full military processing. (See Section 1.)

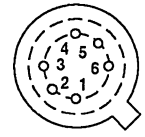
For additional design information please see performance curves NQP, which are located in Section 7.

PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G MAX (pA)	$\lvert V_{GS_1} - V_{GS_2} \rvert$ MAX (mV)
2N5196	-50	1	-15	5
2N5197	-50	1	-15	5
2N5198	-50	1	-15	10
2N5199	-50	1	-15	15

TO-71



BOTTOM VIEW



1 SOURCE 1
2 DRAIN 1
3 GATE 1
4 SOURCE 2
5 DRAIN 2
6 GATE 2

SIMILAR PRODUCTS

- Low Noise, See U401 Series
- Low Leakage, See U421 Series
- High Gain, See 2N5911 Series
- Chips, Order 2N519XCHP Series

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMIT	UNITS
Gate-Drain Voltage		V_{GD}	-50	V
Gate-Source Voltage		V_{GS}	-50	
Forward Gate Current		I_G	50	mA
Power Dissipation (T_A = 85°)	Per Side	P_D	250	mW
	Total		500	
Power Derating (T_A = 85°)	Per Side		2.56	mW/°C
	Total		4.3	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature		T_{stg}	-65 to 200	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

ELECTRICAL CHARACTERISTICS [1]			LIMITS					
				2N5196		2N5197		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-57	-50		-50		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 20 V, I_D = 1 nA	-2	-0.7	-4	-0.7	-4	
Saturation Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	3	0.7	7	0.7	7	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -30 V, V_{DS} = 0 V	-10		-25		-25	pA
		T_A = 150°C	-20		-50		-50	nA
Gate Operating Current	I_G	V_{DG} = 20 V, I_D = 200 µA	-5		-15		-15	pA
		T_A = 125°C	-0.8		-15		-15	nA
Gate-Source Voltage	V_{GS}	V_{DG} = 20 V, I_D = 200 µA	-1.5	-0.2	-3.8	-0.2	-3.8	V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 kHz	2.5	1	4	1	4	mS
Common-Source Output Conductance	g_{os}		2		50		50	µS
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 20 V, I_D = 200 µA, f = 1 kHz	0.8	0.7	1.6	0.7	1.6	mS
Common-Source Output Conductance	g_{os}		1		4		4	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	3		6		6	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1		2		2	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 kHz	9		20		20	$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DS} = 20 V, V_{GS} = 0 V, f = 100 Hz, R_G = 10 MΩ	<0.1		0.5		0.5	dB
MATCHING								
Differential Gate-Source Voltage	$\lvert V_{GS1}-V_{GS2}\rvert$	V_{DG} = 20 V, I_D = 200 µA	3		5		5	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	V_{DG} = 20 V, I_D = 200 µA, T = -55 to 25°C	3		5		10	µV/°C
		T = 25 to 125°C	3		5		10	
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 20 V, V_{GS} = 0 V	0.98	0.95	1	0.95	1	
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V_{DG} = 20 V, I_D = 200 µA, f = 1 kHz	0.99	0.97	1	0.97	1	
Differential Output Conductance	$\lvert g_{os1}-g_{os2}\rvert$		0.1		1		1	µS
Differential Gate Current	$\lvert I_{G1}-I_{G2}\rvert$	V_{DG} = 20 V, I_D = 200 µA, T_A = 125°C	0.1		5		5	nA
Common Mode Rejection Ratio	CMRR	V_{DD} = 10 to 20 V, I_D = 200 µA	100					dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

4

Siliconix incorporated

ELECTRICAL CHARACTERISTICS [1]			LIMITS					
				2N5198		2N5199		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-57	-50		-50		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 20 V, I_D = 1 nA	-2	-0.7	-4	-0.7	-4	
Saturation Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	3	0.7	7	0.7	7	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -30 V, V_{DS} = 0 V	-10		-25		-25	pA
		T_A = 150°C	-20		-50		-50	nA
Gate Operating Current	I_G	V_{DG} = 20 V, I_D = 200 µA	-5		-15		-15	pA
		T_A = 125°C	-0.8		-15		-15	nA
Gate-Source Voltage	V_{GS}	V_{DG} = 20 V, I_D = 200 µA	-1.5	-0.2	-3.8	-0.2	-3.8	V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 kHz	2.5	1	4	1	4	mS
Common-Source Output Conductance	g_{os}		2		50		50	µS
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 20 V, I_D = 200 µA, f = 1 kHz	0.8	0.7	1.6	0.7	1.6	mS
Common-Source Output Conductance	g_{os}		1		4		4	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	3		6		6	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1		2		2	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 kHz	9		20		20	$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DS} = 20 V, V_{GS} = 0 V, f = 100 Hz, R_G = 10 MΩ	<0.1		0.5		0.5	dB
MATCHING								
Differential Gate-Source Voltage	$\lvert V_{GS1}-V_{GS2} \rvert$	V_{DG} = 20 V, I_D = 200 µA	7		10		15	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta \lvert V_{GS1}-V_{GS2} \rvert}{\Delta T}$	V_{DG} = 20 V, I_D = 200 µA, T = -55 to 25°C	10		20		40	µV/°C
		T = 25 to 125°C	10		20		40	
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 20 V, V_{GS} = 0 V	0.97	0.95	1	0.95	1	
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V_{DG} = 20 V, I_D = 200 µA, f = 1 kHz	0.97	0.95	1	0.95	1	
Differential Output Conductance	$\lvert g_{os1}-g_{os2} \rvert$		0.2		1		1	µS
Differential Gate Current	$\lvert I_{G1}-I_{G2} \rvert$	V_{DG} = 20 V, I_D = 200 µA, T_A = 125°C	0.1		5		5	nA
Common Mode Rejection Ratio	CMRR	V_{DD} = 10 to 20 V, I_D = 200 µA	97					dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

2N5432 SERIES

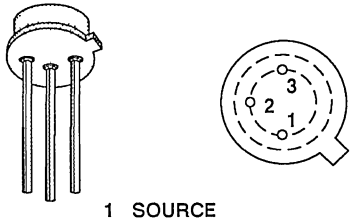
N-Channel JFET

The 2N5432 Series offers the designer an alternative for true high performance analog switching applications. Good breakdown voltage characteristics coupled with low on-resistance and very fast switching make these devices suitable for a wide range of applications. For military designs, the TO-52 package is hermetically sealed and suitable for processing per MIL-S-19500. (See Section 1.)

For further design information please consult the typical performance curves NIP which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	$I_{D(OFF)}$ MAX (pA)	t_{ON} MAX (ns)
2N5432	–25	5	200	5
2N5433	–25	7	200	5
2N5434	–25	10	200	5

TO-206AC (TO-52) BOTTOM VIEW



1 SOURCE
2 DRAIN
3 GATE

SIMILAR PRODUCTS

- SOT-23, See SST108 Series
- TO-92, See J108 Series
- Chips, Order 2N543XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	–25	V
Gate-Source Voltage	V_{GS}	–25	
Gate Current	I_G	100	mA
Power Dissipation	P_D	300	mW
Power Derating		2.4	mW/°C
Operating Junction Temperature	T_J	–55 to 150	°C
Storage Temperature	T_{stg}	–65 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

Siliconix incorporated

ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				2N5432		2N5433		2N5434		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-32	-25		-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 5 V, I_D = 3 nA		-4	-10	-3	-9	-1	-4	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		150		100		30		mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-5		-200		-200		-200	pA
		V_{DS} = 0 V, T_A = 150°C	-10		-200		-200		-200	nA
Gate Operating Current[4]	I_G	V_{DG} = 10 V, I_D = 10 mA	-10							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 5 V, V_{GS} = -10 V	10		200		200		200	pA
		V_{DS} = 5 V, V_{GS} = -10 V, T_A = 150°C	20		200		200		200	nA
Drain-Source On-Voltage	$V_{DS(ON)}$	V_{GS} = 0 V, I_D = 10 mA			50		70		100	mV
Drain-Source On-Resistance	$r_{DS(ON)}$			2	5		7		10	Ω
Gate-Source Forward Voltage[4]	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance[4]	g_{fs}	V_{DG} = 5 V, I_D = 10 mA, f = 1 kHz	17							mS
Common-Source Output Conductance[4]	g_{os}		600							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V, f = 1 kHz			5		7		10	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = -10 V, f = 1 MHz	20		30		30		30	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		11		15		15		15	pF
Equivalent Input Noise Voltage[4]	$\bar{e}_n$	V_{DG} = 5 V, I_D = 10 mA, f = 1 kHz	3.5							$nV/\sqrt{Hz}$
SWITCHING										
Turn-on Time	$t_{d(ON)}$	V_{DD} = 1.5 V, $V_{GS(ON)}$ = 0 V	2		4		4		4	ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	0.5		1		1		1	ns
Turn-off Time	$t_{d(OFF)}$	2N5432 10 mA -12 V 145 Ω	4		6		6		6	ns
	t_f	2N5433 10 mA -12 V 143 Ω 2N5434 10 mA -12 V 140 Ω	18		30		30		30	ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µS, duty cycle ≤ 3%.
4. This parameter not registered with JEDEC.

2N5460 SERIES

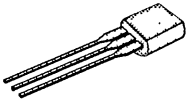
P-Channel JFETs

The 2N5460 Series are low cost p-channel JFETs designed to provide all-around performance in a wide range of amplifier and analog switch applications. This series features two ranges of gate-source breakdown voltage, good gain, and low capacitance. Its p-channel construction also affords the designer simplicity for many applications. Its TO-92 package is compatible with a wide range of tape and reel options for automated assembly. (See Section 8.)

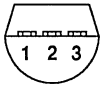
For additional design information please see performance curves PSCIB, which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
2N5460	6	40	1	-5
2N5461	7.5	40	1.5	-9
2N5462	9	40	2	-16
2N5463	6	60	1	-5
2N5464	7.5	60	1.5	-9
2N5465	9	60	2	-16

TO-92



BOTTOM VIEW



1 SOURCE
2 DRAIN
3 GATE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT		UNITS
		2N5460-2	2N5463-5	
Gate-Drain Voltage	V_{GD}	40	60	V
Gate-Source Voltage	V_{GS}	40	60	
Gate Current	I_G	10		mA
Power Dissipation	P_D	310		mW
Power Derating		2.8		mW/°C
Operating Junction Temperature	T_J	-55 to 135		°C
Storage Temperature	T_{stg}	-65 to 150		
Lead Temperature (1/16" from case for 10 seconds)	T_L	300		

4

ELECTRICAL CHARACTERISTICS[1]				LIMITS							
				2N5460		2N5461		2N5462		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 10 µA, V_{DS} = 0 V	55	40		40		40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = −15 V, I_D = −1 µA		0.75	6	1	7.5	1.8	9	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = −15 V, V_{GS} = 0 V		−1	−5	−2	−9	−4	−16	mA
Gate Reverse Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	0.003		5		5		5	nA
		T_A = 100°C	0.0003		1		1		1	µA
Gate Operating Current	I_G	V_{DG} = −20 V, I_D = −0.1 mA	3							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = −15 V, V_{GS} = 10 V	−5							pA
Gate-Source Voltage	V_{GS}	V_{DS} = −15 V, I_D = −0.1 mA	1.3	0.5	4					V
		V_{DS} = −15 V, I_D = −0.2 mA	2.3			0.8	4.5			V
		V_{DS} = −15 V, I_D = −0.4 mA	3.8					1.5	6	V
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = −1 mA, V_{DS} = 0 V	−0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = −15 V, V_{GS} = 0 V, f = 1 kHz		1	4	1.5	5	2	6	mS
Common-Source Output Conductance	g_{os}	V_{DS} = −15 V, V_{GS} = 0 V, f = 1 kHz			75		75		75	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = −15 V, V_{GS} = 0 V, f = 1 MHz	4.5		7		7		7	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = −15 V, V_{GS} = 0 V, f = 1 MHz	1.2							pF
Common-Source Output Capacitance	C_{oss}	V_{DS} = −15 V, V_{GS} = 0 V, f = 1 MHz	1.5		2		2		2	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = −15 V, V_{GS} = 0 V, f = 100 Hz	15		115		115		115	$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DS} = −15 V, V_{GS} = 0 V, f = 100 Hz, R_G = 1 MΩ, BW = 1 Hz	0.2		2.5		2.5		2.5	dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				2N5463		2N5464		2N5465		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 10 µA, V_{DS} = 0 V	65	60		60		60		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = −15 V, I_D = −1 µA		0.75	6	1	7.5	1.8	9	V
Saturation Drain Current [3]	I_{DSS}	V_{DS} = −15 V, V_{GS} = 0 V		−1	−5	−2	−9	−4	−16	mA
Gate Reverse Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	0.003		5		5		5	nA
		T_A = 100°C	0.0003		1		1		1	µA
Gate Operating Current	I_G	V_{DG} = −20 V, I_D = −0.1 mA	3							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = −15 V, V_{GS} = 10 V	−5							pA
Gate-Source Voltage	V_{GS}	V_{DS} = −15 V, I_D = −0.1 mA	1.3	0.5	4					V
		I_D = −0.2 mA	2.3			0.8	4.5			V
		I_D = −0.4 mA	3.8					1.5	6	V
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = −1 mA, V_{DS} = 0 V	−0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = −15 V, V_{GS} = 0 V, f = 1 kHz		1	4	1.5	5	2	6	mS
Common-Source Output Conductance	g_{os}	V_{DS} = −15 V, V_{GS} = 0 V, f = 1 kHz			75		75		75	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = −15 V, V_{GS} = 0 V, f = 1 MHz	4.5		7		7		7	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = −15 V, V_{GS} = 0 V, f = 1 MHz	1.2							pF
Common-Source Output Capacitance	C_{oss}	V_{DS} = −15 V, V_{GS} = 0 V, f = 1 MHz	1.5		2		2		2	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = −15 V, V_{GS} = 0 V, f = 100 Hz	15		115		115		115	$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DS} = −15 V, V_{GS} = 0 V, f = 100 Hz, R_G = 1 MΩ, BW = 1 Hz	0.2		2.5		2.5		2.5	dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

2N5484 SERIES

Siliconix incorporated

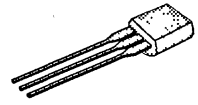
N-Channel JFETs

The 2N5484 Series of n-channel JFETs is designed to provide high-performance amplification, especially at high-frequency. These parts feature low noise (4 dB max @ 400 MHz), high gain (5.5 mS typical @ 400 MHz) and provide wide bandwidth. Additionally, its low-cost TO-92 package is available with tape and reel to support automated assembly. (See Section 8.)

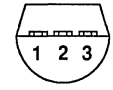
For additional design information please see performance curves NH, which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
2N5484	-3	-25	3	5
2N5485	-4	-25	3.5	10
2N5486	-6	-25	4	20

TO-92



BOTTOM VIEW



1 DRAIN
2 SOURCE
3 GATE

SIMILAR PRODUCTS

- SOT-23, See SST5484 Series
- Chips, Order 2N548XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	
Gate Current	I_G	10	mA
Drain Current	I_D	30	
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature	T_J	-65 to 135	°C
Storage Temperature	T_{stg}	-65 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS[1]				LIMITS							
					2N5484		2N5485		2N5486		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC											
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V		-35	-25		-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 10 nA			-0.3	-3	-0.5	-4	-2	-6	
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V			1	5	4	10	8	20	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V		-0.002		-1		-1		-1	nA
			T_A = 100°C	-0.2		-200		-200		-200	
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 1 mA		-20							pA
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 10 mA, V_{DS} = 0 V		0.8							V
DYNAMIC											
Common-Source Forward Transconductance	g_{fs}	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 kHz			3	6	3.5	7	4	8	mS
Common-Source Output Conductance	g_{os}					50		60		75	µS
Common-Source Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		2.2		5		5		5	pF
Common-Source Reverse Transfer Capacitance	C_{rss}			0.7		1		1		1	
Common-Source Output Capacitance	C_{oss}			1		2		2		2	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{GS} = 0 V, V_{DS} = 15 V, f = 100 Hz		10							$nV/\sqrt{Hz}$
HIGH FREQUENCY											
Common-Source Forward Transconductance	y_{fs}	V_{DS} = 15 V, V_{GS} = 0 V	f = 100 MHz	4.5	2.5						mS
			f = 400 MHz	5.5			3		3.5		
Common-Source Output Conductance	y_{os}		f = 100 MHz	30		75					µS
			f = 400 MHz	50				100		100	
Common-Source Input Conductance	y_{is}		f = 100 MHz			0.1					mS
			f = 400 MHz					1		1	
Common-Source Power Gain	G_{ps}	V_{DS} = 15 V, f = 100 MHz	I_D = 1 mA	20	16	25					dB
			I_D = 4 mA	21			18	30	18	30	
		V_{DS} = 15 V, f = 400 MHz	I_D = 4 mA	13			10	20	10	20	
Noise Figure	NF	V_{DS} = 15 V, V_{GS} = 0 V, R_G = 1 MΩ, f = 1 kHz		0.3		2.5		2.5		2.5	
		V_{DS} = 15 V, I_D = 1 mA, R_G = 1 kΩ, f = 100 MHz		2		3					
		V_{DS} = 15 V, I_D = 4 mA, R_G = 1 kΩ	f = 100 MHz	1				2		2	
			f = 400 MHz	2.5				4		4	

NOTES: 1. T_A = 25°C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

2N5564 SERIES

Siliconix incorporated

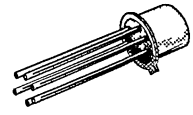
N-Channel JFET Pairs

The 2N5564 Series are matched pairs of JFETs mounted in a single TO-71 package. This two-chip design reduces parasitic performance at high frequency while ensuring extremely tight matching. The 2N5564 features high breakdown voltage ($V_{(BR)GSS}$ typically > 55 V), high gain (typically > 9 mS), and less than 5 mV offset between the two die. Additionally, its TO-71 package is hermetically sealed and can be processed per MIL-S-19500. (See Section 1.)

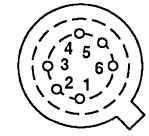
For additional design information please see performance curves NCB, which are located in Section 7.

PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G MAX (pA)	$\lvert V_{GS_1} - V_{GS_2} \rvert$ MAX (mV)
2N5564	-40	7.5	-100	5
2N5565	-40	7.5	-100	10
2N5566	-40	7.5	-100	20

TO-71



BOTTOM VIEW



1 SOURCE 1
2 DRAIN 1
3 GATE 1
4 SOURCE 2
5 DRAIN 2
6 GATE 2

SIMILAR PRODUCTS

- Low Noise, See U401 Series
- Low Leakage, See U421 Series
- Chips, Order 2N556XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMIT	UNITS
Gate-Drain Voltage		V_{GD}	-40	V
Gate-Source Voltage		V_{GS}	-40	
Gate-Gate Voltage		V_{GG}	± 80	
Forward Gate Current		I_G	50	mA
Power Dissipation	Per Side	P_D	325	mW
	Total		650	
Power Derating	Per Side		2.2	mW/°C
	Total		3.3	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature		T_{stg}	-65 to 200	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

ELECTRICAL CHARACTERISTICS[1]			LIMITS							
				2N5564		2N5565		2N5566		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-55	-40		-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 1 nA	-2	-0.5	-3	-0.5	-3	-0.5	-3	V
Saturation Drain Current	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V	20	5	30	5	30	5	30	mA
Gate Reverse Current[3]	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-5		-100		-100		-100	pA
		T_A = 150°C	-10		-200		-200		-200	nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 2 mA	-3							pA
		T_A = 125°C	-1							nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA	50		100		100		100	Ω
Gate-Source Voltage	V_{GS}	V_{DS} = 15 V, I_D = 2 mA	-1.2							V
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 2 mA, V_{DS} = 0 V	0.7		1		1		1	V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 15 V, I_D = 2 mA, f = 1 kHz	9	7.5	12.5	7.5	12.5	7.5	12.5	mS
Common-Source Output Conductance	g_{os}		35		45		45		45	µS
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 15 V, I_D = 2 mA, f = 100 MHz	8.5	7		7		7		mS
Common-Source Input Capacitance	C_{iss}	V_{DG} = 15 V, I_D = 2 mA, f = 1 MHz	10		12		12		12	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		2.5		3		3		3	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 15 V, I_D = 2 mA, f = 10 Hz	12		50		50		50	$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DG} = 15 V, I_D = 2 mA, f = 10 Hz, R_G = 1 MΩ	0.1		1		1		1	dB
MATCHING										
Differential Gate-Source Voltage	$\lvert V_{GS1}-V_{GS2}\rvert$	V_{DS} = 15 V, I_D = 2 mA			5		10		20	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	V_{DS} = 15 V, I_D = 2 mA, T = -55 to 25°C			10		25		50	µV/°C
		T = 25 to 125°C			10		25		50	
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 15 V, V_{GS} = 0 V	0.98	0.95	1	0.95	1	0.95	1	
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V_{DS} = 15 V, I_D = 2 mA, f = 1 kHz	0.98	0.95	1	0.90	1	0.90	1	
Common Mode Rejection Ratio	CMRR	V_{DD} = 10 to 20 V, I_D = 2 mA	76							dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

4

2N5638 SERIES

Siliconix incorporated

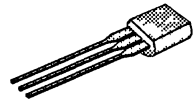
N-Channel JFET

The 2N5638 Series is a multi-purpose n-channel JFET designed to economically enhance circuit performance. These devices are especially well suited for analog switching applications and feature very fast switching speeds, but function efficiently as high-gain amplifiers, particularly at high-frequency. Our low-cost TO-92 packaging offers affordable performance with flexibility for designers, as these devices can be ordered with a variety of lead forms or tape and reel for automated insertion. (See Section 8.)

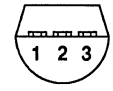
For additional design information please consult the typical performance curves NCB which are located in Section 7.

PART NUMBER	$V_{(BR)DSS}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	$I_{D(OFF)}$ MAX (nA)	t_{ON} MAX (ns)
2N5638	-30	30	1	9
2N5639	-30	60	1	14
2N5640	-30	100	1	18

TO-92



BOTTOM VIEW



1 DRAIN
2 SOURCE
3 GATE

SIMILAR PRODUCTS

- TO-18, See 2N4391 Series
- SOT-23, See SST4391 Series
- Duals, See 2N5564 Series
- Chips, Order 2N563XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-30	V
Gate-Source Voltage	V_{GS}	-30	
Gate Current	I_G	10	mA
Power Dissipation	P_D	625	mW
Power Derating		5.68	mW/°C
Operating Junction Temperature	T_J	-65 to 135	°C
Storage Temperature	T_{stg}	-65 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				2N5638		2N5639		2N5640		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -10 µA, V_{DS} = 0 V	-55	-30		-30		-30		V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V		50		25		5		mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-0.005		-1		-1		-1	nA
		V_{DS} = 0 V, T_A=100°C	-0.01		-1		-1		-1	µA
Gate Operating Current[4]	I_G	V_{DG} = 15 V, I_D = 10 mA	-5							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 15 V, V_{GS} = -6 V	0.005						1	nA
		V_{DS} = 15 V, V_{GS} = -8 V	0.005				1			
		V_{DS} = 15 V, V_{GS} = -12 V	0.005		1					
		V_{DS} = 15 V, T_A=100°C, V_{GS} = -6 V	0.01						1	µA
		V_{DS} = 15 V, T_A=100°C, V_{GS} = -8 V	0.01				1			
		V_{DS} = 15 V, T_A=100°C, V_{GS} = -12 V	0.01		1					
Drain-Source On-Voltage	$V_{DS(ON)}$	V_{GS} = 0 V, I_D = 3 mA	0.25						0.5	V
		V_{GS} = 0 V, I_D = 6 mA	0.30				0.5			
		V_{GS} = 0 V, I_D = 12 mA	0.35		0.5					
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA			30		60		100	Ω
Gate-Source Forward Voltage[4]	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance[4]	g_{fs}	V_{DG} = 20 V, I_D = 1 mA, f = 1 kHz	6							mS
Common-Source Output Conductance[4]	g_{os}		25							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 mA, f = 1 kHz			30		60		100	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = -12 V, f = 1 MHz	7		10		10		10	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		3		4		4		4	
Equivalent Input Noise Voltage[4]	$\bar{e}_n$	V_{DG} = 10 V, I_D = 10 mA, f = 1 kHz	3.0							$nV/\sqrt{Hz}$
SWITCHING										
Turn-on Time	$t_{d(ON)}$	V_{DD} = 10 V, $V_{GS(ON)}$ = 0 V	2		4		6		8	ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	2		5		8		10	
Turn-off Time	$t_{d(OFF)}$	2N5638 12 mA -10 V 800 Ω	6		5		10		15	
	t_f	2N5639 6 mA -10 V 1600 Ω 2N5640 3 mA -10 V 3200 Ω	13		10		20		30	

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µS, duty cycle ≤ 3%.
4. This parameter not registered with JEDEC.

4

2N5911 SERIES

Siliconix incorporated

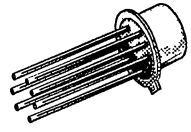
N-Channel JFET Pairs

The 2N5911 Series are JFET matched pairs mounted in a single TO-78 package. This two chip design reduces parasitic performance at high frequency while ensuring extremely tight matching. The 2N5911 features high speed amplification (slew rate), high gain (typically > 6 mS), and low gate leakage (typically < 1 pA). This performance makes these devices perfect for use as wideband differential amplifiers in demanding test and measurement applications. Finally, its TO-78 hermetically sealed package is available with military screening per MIL-S-19500. (See Section 1.)

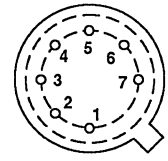
For additional design information please see performance curves NZF, which are located in Section 7.

PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G MAX (pA)	$\|V_{GS_1} - V_{GS_2}\|$ MAX (mV)
2N5911	-25	5	-100	10
2N5912	-25	5	-100	15

TO-78



BOTTOM VIEW



1 SOURCE 1
2 DRAIN 1
3 GATE 1
4 CASE
5 SOURCE 2
6 DRAIN 2
7 GATE 2

SIMILAR PRODUCTS

- SO-8, See SST5912
- Monolithic, See M5911 Series
- Low Noise, See U401 Series
- Low Leakage, See U421 Series
- Chips, Order 2N591XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMIT	UNITS
Gate-Drain Voltage		V_{GD}	-25	V
Gate-Source Voltage		V_{GS}	-25	
Gate-Gate Voltage		V_{GG}	± 80	
Forward Gate Current		I_G	50	mA
Power Dissipation	Per Side	P_D	367	mW
	Total		500	
Power Derating	Per Side		3	mW/°C
	Total		4	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature		T_{stg}	-65 to 200	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

ELECTRICAL CHARACTERISTICS[1]			LIMITS					
				2N5911		2N5912		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-35	-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA	-3.5	-1	-5	-1	-5	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	15	7	40	7	40	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-1		-100		-100	pA
		T_A = 150°C	-2		-250		-250	nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 5 mA	-1		-100		-100	pA
		T_A = 125°C	-0.3		-100		-100	nA
Gate-Source Voltage	V_{GS}	V_{DG} = 10 V, I_D = 5 mA	-1.5	-0.3	-4	-0.3	-4	V
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 5 mA, f = 1 kHz	6	5	10	5	10	mS
Common-Source Output Conductance	g_{os}		70		100		100	µS
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 5 mA, f = 100 MHz	5.8	5	10	5	10	mS
Common-Source Output Conductance	g_{os}		90		150		150	µS
Common-Source Input Capacitance	C_{iss}	V_{DG} = 10 V, I_D = 5 mA, f = 1 MHz	3		5		5	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1		1.2		1.2	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 5 mA, f = 10 kHz	4		20		20	$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DG} = 10 V, I_D = 5 mA, f = 10 kHz, R_G = 100 kΩ	0.1		1		1	dB
MATCHING								
Differential Gate-Source Voltage	$\lvert V_{GS1}-V_{GS2} \rvert$	V_{DG} = 10 V, I_D = 5 mA	4		10		15	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta \lvert V_{GS1}-V_{GS2} \rvert}{\Delta T}$	V_{DG} = 10 V, I_D = 5 mA, T = -55 to 25°C	15		20		40	µV/°C
		T = 25 to 125°C	15		20		40	µV/°C
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 10 V, V_{GS} = 0 V	0.98	0.95	1	0.95	1	
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V_{DG} = 10 V, I_D = 5 mA, f = 1 kHz	0.98	0.95	1	0.95	1	
Differential Gate Current	$\lvert I_{G1}-I_{G2} \rvert$	V_{DG} = 10 V, I_D = 5 mA, T_A = 125°C	0.005		20		20	nA
Common Mode Rejection Ratio	CMRR	V_{DD} = 5 to 10 V, I_D = 5 mA	85					dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

4

2N6905 SERIES

Siliconix incorporated

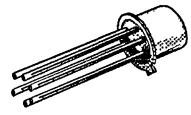
N-Channel JFET Pairs

The 2N6905 Series of high-performance monolithic dual JFETs features extremely low noise, tight offset voltage and drift over temperature specifications. It is targeted for use in a wide range of precision instrumentation applications. The 2N6905 Series has a wide selection of both offset and drift ranges with the prime device, the 2N6905, featuring 5 mV offset and 10 μV/°C drift. The three devices allow designers to make important cost/benefit decisions. This series is available in a TO-71 hermetically sealed package and is available with military screening. (See Section 1.)

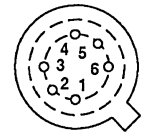
For additional design information please see performance curves NNR, which are located in Section 7.

PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G MAX (pA)	$\lvert V_{GS_1} - V_{GS_2} \rvert$ MAX (mV)
2N6905	–35	2	–5	5
2N6906	–35	2	–5	10
2N6907	–35	2	–5	25

TO-71



BOTTOM VIEW



1 SOURCE 1
2 DRAIN 1
3 GATE 1
4 SOURCE 2
5 DRAIN 2
6 GATE 2

SIMILAR PRODUCTS

- High-Gain, See 2N5911 Series
- SO-8, See SST404 Series
- Chips, Order 2N690XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMIT	UNITS
Gate-Drain Voltage		V_{GD}	–35	V
Gate-Source Voltage		V_{GS}	–35	
Forward Gate Current		I_G	10	mA
Power Dissipation	Per Side	P_D	300	mW
	Total		500	
Power Derating	Per Side		2.6	mW/°C
	Total		5	
Operating Junction Temperature		T_J	–55 to 150	°C
Storage Temperature		T_{stg}	–65 to 200	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

ELECTRICAL CHARACTERISTICS[1]			LIMITS							
				2N6905		2N6906		2N6907		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-55	-35		-35		-35		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 1 nA	-1.5	-0.2	-3	-0.2	-3	-0.2	-3	V
Saturation Drain[3] Current	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	3.5	0.5	10	0.5	10	0.5	10	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-2		-15		-15		-15	pA
		T_A = 125°C	-1							nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 200 µA	-2		-5		-5		-5	pA
		T_A = 125°C	-0.8		-5		-5		-5	nA
Drain-Source On-Resistance[4]	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 0.1 mA	250							Ω
Gate-Source Voltage	V_{GS}	V_{DG} = 15 V, I_D = 200 µA	-1		-2.3		-2.3		-2.3	V
Gate-Source Forward Voltage[4]	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	4	2	7	2	7	2	7	mS
Common-Source Output Conductance	g_{os}		4		20		20		20	µS
Common-Source Input Capacitance	C_{iss}	V_{DG} = 15 V, I_D = 200 µA, f = 1 MHz	4		8		8		8	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.5		3		3		3	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 10 Hz	10		15		15		15	$nV/\sqrt{Hz}$
MATCHING										
Differential Gate-Source Voltage	$\lvert V_{GS1}-V_{GS2}\rvert$	V_{DG} = 10 V, I_D = 200 µA			5		10		25	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	V_{DG} = 10 V, I_D = 200 µA, T = -55 to 25°C			10		25		25	µV/°C
		T = 25 to 125°C			10		25		50	
Saturation Drain Current Ratio[4]	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 10 V, V_{GS} = 0 V	0.97							
Transconductance Ratio[4]	$\frac{g_{fs1}}{g_{fs2}}$	V_{DG} = 10 V, I_D = 0.2 mA, f = 1 kHz	0.97							
Differential Output Conductance[4]	$\lvert g_{os1}-g_{os2}\rvert$		0.1							µS
Differential Gate Current[4]	$\lvert I_{G1}-I_{G2}\rvert$	V_{DG} = 15 V, I_D = 0.2 mA, T_A = 25°C	1							pA
Common Mode Rejection Ratio	CMRR	V_{DG} = 10 to 20 V, I_D = 200 µA	102	95		95		95		dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.
4. This parameter not registered with JEDEC.

4

2N6908 SERIES

Siliconix incorporated

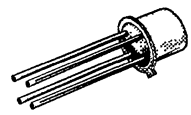
N-Channel JFET Circuits

The 2N6908 Series is much more than a JFET. The addition of back-to-back diodes effectively clamps input "over-voltage" while a high-performance JFET provides an effective amplification stage. With the addition of a source resistor, a complete common-source amplifier is created which provides both low leakage and very low noise. This performance is especially effective as a small signal pre-amplifier as well as impedance matching between low and high impedance sources. Finally, its TO-72 package is hermetically sealed and is available with full military screening per MIL-S-19500. (See Section 1.)

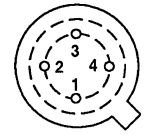
For additional design information please see performance curves NBB, which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (μS)	I_{DSS} MAX (mA)
2N6908	-1.8	-30	100	2
2N6909	-2.3	-30	400	3.5
2N6910	-3.5	-30	1200	5

TO-72



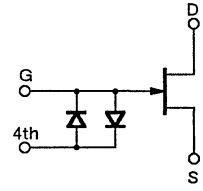
BOTTOM VIEW



1 SOURCE
2 DRAIN
3 GATE
4 DIODES

SIMILAR PRODUCTS

- SOT-143, See SST6908 Series
- Chips, Order 2N69XXCHP



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-30	V
Gate-Source Voltage	V_{GS}	-30	
Forward Gate Current	I_G	10	mA
Power Dissipation	P_D	300	mW
Power Derating		2.4	mW/°C
Operating Junction Temperature	T_J	-55 to 150	°C
Storage Temperature	T_{stg}	-55 to 200	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS[1]			LIMITS							
				2N6908		2N6909		2N6910		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = −1 µA, V_{DS} = 0 V, V_{G4} = 0 V	−50	−30		−30		−30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA, V_{G4} = 0 V		−0.3	−1.8	−0.6	−2.3	−0.9	−3.5	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V, V_{G4} = 0 V		0.05	2	0.2	3.5	0.6	5	mA
Gate Reverse Current	I_{GSS}	V_{GS} = −15 V, V_{DS} = 0 V, V_{G4} = 0 V	−2		−25		−25		−25	pA
		T_A = 125°C	−1							nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 50 µA	−2							pA
Forward Gate Diode Current 4	I_{G4}	V_{G4} = ± 100 mV	± 1		± 10		± 10		± 10	pA
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = ± 0.5 mA, V_{DS} = 0 V, V_{G4} = 0 V	± 0.7		± 1.2		± 1.2		± 1.2	V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V, V_{G4} = 0 V, f = 1 kHz		0.1	3	0.4	3.5	1.2	4	mS
Common-Source Output Conductance	g_{os}				50		75		100	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, V_{G4} = 0 V, f = 1 MHz	3.2		5		5		5	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.5		2		2		2	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 100 Hz	12		25		25		25	$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 kHz, R_G = 1 MΩ	0.1		1		1		1	dB

NOTES:
1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.
4. Forward diode current when a voltage is applied between gate and fourth lead.

4

BF244 SERIES

Siliconix incorporated

N-Channel JFETs

The BF244 Series of n-channel JFETs is selected into narrow current ranges to simplify design and biasing requirements of high performance JFET amplifier stages. The BF244A, BF244B, and BF244C have been selected into I_{DSS} ranges of 2 to 6.5 mA, 6 to 15 mA, and 12 to 25 mA respectively. Additionally, this series features high gain (>3 mS) and low capacitance. Finally, its TO-92 package offers the designer low cost and compatibility with automated assembly. (See Section 8.)

For additional design information please see performance curves NH, which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
BF244A	-8	-30	3	6.5
BF244B	-8	-30	3	15
BF244C	-8	-30	3	25

TO-92 BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-30	V
Gate-Source Voltage	V_{GS}	-30	
Gate Current	I_G	10	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature	T_J	-55 to 135	°C
Storage Temperature	T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				BF244A		BF244B		BF244C		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-35	-30		-30		-30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 10 µA		-0.5	-8	-0.5	-8	-0.5	-8	V
Saturation Drain Current [3]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		2	6.5	6	15	12	25	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-0.002		-5		-5		-5	nA
		T_A = 125°C	-1							
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 1 mA	-20							pA
Gate-Source Voltage	V_{GS}	V_{DS} = 15 V, I_D = 200 µA		-0.4	-2.2	-1.6	-3.8	-3.2	-7.5	V
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 kHz		3	6.5	3	6.5	3	6.5	mS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = -1 V, f = 1 MHz	2							pF
Common-Source Reverse Transfer Capacitance	C_{rss}		0.8							
Common-Source Output Capacitance	C_{oss}		1							
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 100 Hz	10							$nV/\sqrt{Hz}$

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

4

BF245 SERIES

Siliconix incorporated

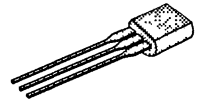
N-Channel JFETs

The BF245 Series of n-channel JFETs is selected into narrow current ranges to simplify design and biasing requirements of high performance JFET amplifier stages. The BF245A, BF245B, and BF245C have been selected into I_{DSS} ranges of 2 to 6.5 mA, 6 to 15 mA, and 12 to 25 mA respectively. Additionally, this series features high gain (>3 mS) and low capacitance. Finally, its TO-92 package offers the designer low cost and compatibility with automated assembly. (See Section 8.)

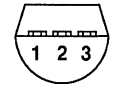
For additional design information please see performance curves NH, which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
BF245A	-8	-30	3	6.5
BF245B	-8	-30	3	15
BF245C	-8	-30	3	25

TO-92



BOTTOM VIEW



1 GATE
2 SOURCE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-30	V
Gate-Source Voltage	V_{GS}	-30	
Gate Current	I_G	10	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature	T_J	-55 to 135	°C
Storage Temperature	T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS[1]			LIMITS							
				BF245A		BF245B		BF245C		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-35	-30		-30		-30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 10 µA		-0.5	-8	-0.5	-8	-0.5	-8	
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		2	6.5	6	15	12	25	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-0.002		-5		-5		-5	nA
		T_A = 125°C	-1							
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 1 mA	-20							pA
Gate-Source Voltage	V_{GS}	V_{DG} = 15 V, I_D = 200 µA		-0.4	-2.2	-1.6	-3.8	-3.2	-7.5	V
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 kHz		3	6.5	3	6.5	3	6.5	mS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = -1 V, f = 1 MHz	2							pF
Common-Source Reverse Transfer Capacitance	C_{rss}		0.8							
Common-Source Output Capacitance	C_{oss}		1							
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 100 Hz	10							$nV/\sqrt{Hz}$

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

4

BSR56 SERIES

Siliconix incorporated

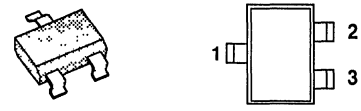
N-Channel JFETs

The BSR56 Series is a n-channel JFET mounted in our popular SOT-23 package. Its low cost and $r_{DS(ON)}$ make it a good choice for an all-purpose analog switch, while its high g_{fs} and good high-frequency response also make this product useful in a high-gain amplifier mode. Like all SOT-23 products available from Siliconix, tape and reel capabilities exist for automated assembly. (See Section 8.)

For further design information please consult the typical performance curves NCB which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	$I_{D(OFF)}$ TYP (pA)	t_{ON} TYP (ns)
BSR56	-10	25	5	4
BSR57	-6	40	5	4
BSR58	-4	60	5	4

SOT-23 TOP VIEW



1 GATE
2 SOURCE
3 DRAIN

SIMILAR PRODUCTS

- TO-18, See 2N4856 Series
- TO-92, See PN4391 Series
- Duals, See 2N5564 Series

PRODUCT MARKING	
BSR56	M4
BSR57	M5
BSR58	M6

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain, Drain-Source Voltage	V_{GD}	-40	V
Gate-Source Voltage	V_{GS}	-40	
Gate Current	I_G	50	mA
Power Dissipation (T_A = 65°C)	P_D	350	mW
Power Derating		2.8	mW/°C
Operating Junction Temperature	T_J	-55 to 175	°C
Storage Temperature	T_{stg}	-55 to 175	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				BSR56		BSR57		BSR58		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-55	-40		-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 0.5 nA		-4	-10	-2	-6	-0.8	-4	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		50		20	100	8	80	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-0.005		-1		-1		-1	nA
		V_{DS} = 0 V, T_A = 125°C	-3							
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 15 V, V_{GS} = -10 V	0.005		1		1		1	nA
		V_{DS} = 15 V, V_{GS} = -10 V, T_A = 125°C	3							
Drain-Source On-Voltage	$V_{DS(ON)}$	V_{GS} = 0 V, I_D = 20 mA	500		750					mV
		V_{GS} = 0 V, I_D = 10 mA	350				500			mV
		V_{GS} = 0 V, I_D = 5 mA	250						400	mV
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA			25		40		60	Ω
DYNAMIC										
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 mA, f = 1 kHz			25		40		60	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	13							pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} = -10 V, f = 1 MHz	3.5		5		5		5	pF
SWITCHING										
Turn-on Time	t_{ON}	V_{DD} = 10 V, $V_{GS(ON)}$ = 0 V; P/N: BSR56 $I_{D(ON)}$ 20 mA $V_{GS(OFF)}$ -10 V; BSR57 10 mA -6 V; BSR58 5 mA -4 V	4							ns
Turn-off Time	t_{OFF}		19		25		50		100	ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 100 ms, duty cycle ≤ 3%.

CR022 SERIES

Siliconix incorporated

Current Regulator Diodes

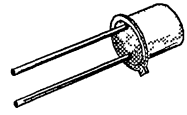
The CR022 Series is a family of precision current regulators designed for demanding applications in test equipment and instrumentation. These devices combine the proven performance of a JFET with an integrated resistor to produce a single two-leaded device which is extremely simple to operate. With nominal current ranges from 0.22 mA to 5.30 mA, the CR022 Series will meet a wide array of design requirements. In addition to its two-lead construction, this series features 10% current ranges, improved current control over wide temperature ranges, and simple "floating" operation as no power supplies are required for biasing. Finally, its TO-18 hermetically sealed package is available with military processing per MIL-S-19500. (See Section 1.)

For additional design information please see typical performance curves (Section 7) as follows:

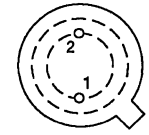
CR022 - CR062 .... NKL
CR068 - CR150 .... NKM
CR160 - CR530 .... NKO

PART	I_F (mA)	PART	I_F (mA)	PART	I_F (mA)
CR022	0.22	CR075	0.75	CR200	2.00
CR024	0.24	CR082	0.82	CR220	2.20
CR027	0.27	CR091	0.91	CR240	2.40
CR030	0.30	CR100	1.00	CR270	2.70
CR033	0.33	CR110	1.10	CR300	3.00
CR039	0.39	CR120	1.20	CR330	3.30
CR043	0.43	CR130	1.30	CR360	3.60
CR047	0.47	CR140	1.40	CR390	3.90
CR056	0.56	CR150	1.50	CR430	4.30
CR062	0.62	CR160	1.60	CR470	4.70
CR068	0.68	CR180	1.80	CR530	5.30

TO-18 2 LEADS



BOTTOM VIEW



1 ANODE
2 CATHODE

SIMILAR PRODUCTS

- TO-92, See J500 Series
- 20% Ranges, See CRR0240 Series
- Chips, Order CRXXXCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Peak Operating Voltage	P_{OV}	100	V
Reverse Current	I_R	50	mA
Thermal Resistance	R_{thJC}	100	°C/W
Power Dissipation at T_C = 25°C	P_D	1.25	W
Operating Junction Temperature	T_J	-55 to 150	°C
Storage Temperature	T_{stg}	-55 to 200	

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

SYMBOL	I_F			Z_d		Z_k		V_L		POV		C_F	θ_1
PARAMETER	REGULATOR CURRENT			DYNAMIC IMPEDANCE		KNEE IMPEDANCE		LIMITING VOLTAGE		PEAK OPERATING VOLTAGE		CAPACITANCE	TEMPERATURE COEFFICIENT
TEST CONDITIONS	V_F = 25 V (Note 1)			V_F = 25 V (Note 2)		V_F = 6 V		I_F = 0.8 $I_{F(MIN)}$ (Note 3)		I_F = 1.1 $I_{F(MAX)}$ (Note 4)		V_F = 25 V f = 1 MHz	V_F = 25 V 0°C ≤ T_A ≤ 100°C
UNITS	mA			MΩ		MΩ		V		V		pF	ppm/°C
	NOM	MIN	MAX	MIN	TYP	MIN	TYP	MAX	TYP	MIN	TYP	TYP	TYP
CR022	0.22	0.198	0 242	9 000	18.00	2.750	3.50	1.00	0.40				2200
CR024	0.24	0.216	0.264	8.000	15.50	2.350	3.00	1.00	0.45				1800
CR027	0.27	0.243	0.297	7.000	13.00	1.950	2.50	1.00	0.50				1450
CR030	0.30	0.270	0.330	6.000	11.50	1.600	2.00	1.00	0.55				1100
CR033	0.33	0.297	0.363	5 000	10.00	1.350	1.80	1.00	0.60	100	180	2.2	800
CR039	0.39	0.351	0 429	4 100	9.00	1.000	1.50	1.05	0.65	(All)	(All)	(All)	500
CR043	0.43	0.387	0.473	3.300	8.00	0.870	1.30	1.05	0.70				250
CR047	0.47	0.423	0.517	2.700	7.00	0.750	1.20	1.10	0.75				0
CR056	0.56	0.504	0.616	1.900	6.00	0.560	0 90	1.20	0.82				-200
CR062	0.62	0.558	0.682	1 550	4 50	0.470	0.70	1.30	0.90				-600
CR068	0.68	0.612	0.748	1 350	10.00	0.400	1.80	1.15	0.85				-350
CR075	0.75	0.675	0.825	1 150	9.00	0.335	1.60	1.20	0.90				-450
CR082	0.82	0.738	0.902	1.000	7.80	0.290	1.40	1.25	0.95				-550
CR091	0.91	0.819	1.001	0 880	6 60	0.240	1.20	1.29	1.00				-650
CR100	1.00	0.900	1.100	0.800	5.50	0.205	1.00	1.35	1.06	100	180	4.2	-750
CR110	1.10	0.990	1.210	0.700	4.80	0.180	0.90	1.40	1.12	(All)	(All)	(All)	-875
CR120	1.20	1.080	1.320	0 640	4 10	0.155	0.80	1.45	1.18				-1000
CR130	1.30	1.170	1.430	0.580	3.50	0.135	0.80	1.50	1.25				-1100
CR140	1.40	1.260	1.540	0.540	3.10	0.115	0.70	1.55	1.32				-1200
CR150	1.50	1.350	1.650	0.510	2.70	0.105	0.60	1.60	1.40				-1300
CR160	1.60	1.440	1.760	0.475	1.10	0 092	0.40	1.65	0.70				1000
CR180	1.80	1.620	1.980	0 420	1 00	0.074	0.34	1.75	0.75				650
CR200	2.00	1.800	2.200	0 395	0.90	0.061	0.28	1.85	0.80				300
CR220	2.20	1.980	2.420	0.370	0.83	0.052	0.25	1.95	0.85				100
CR240	2.40	2.160	2.640	0 345	0.76	0.044	0.22	2.00	0.90				0
CR270	2.70	2.430	2.970	0.320	0 70	0.035	0.19	2.15	0.95	100	175	6	-200
CR300	3.00	2.700	3.300	0 300	0 65	0.029	0.16	2.25	1.00	(All)	(All)	(All)	-400
CR330	3 30	2.970	3.630	0.280	0.60	0.024	0 14	2.35	1.05				-550
CR360	3.60	3.240	3.960	0 265	0.54	0.020	0.13	2.50	1.10				-730
CR390	3.90	3.510	4.290	0 255	0.47	0.017	0.12	2.60	1 17				-820
CR430	4.30	3.870	4 730	0 245	0.40	0.014	0.10	2.75	1.25				-1000
CR470	4.70	4.230	5 170	0 235	0 35	0.012	0.09	2.90	1.32				-1125
CR530	5 30	4 770	5.830	0.220	0.30	0.010	0.07	3.10	1.40				-1250

NOTES:
1. Pulse test - steady state currents may vary.
2. Pulse test - steady state impedances may vary.
3. Min V_F required to insure $I_F > 0.8\ I_{F(MIN)}$.
4. Max V_F where $I_F < 1.1\ I_{F(MAX)}$ is guaranteed.

CRR0240 SERIES

Siliconix incorporated

Current Regulator Diodes

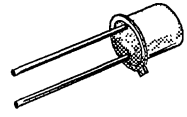
The CRR0240 Series is a family of precision current regulators designed for demanding applications in test equipment and instrumentation. These devices combine the proven performance of a JFET with an integrated resistor to produce a single two-leaded device which is extremely simple to operate. With nominal current ranges from 0.24 mA to 4.3 mA, the CRR0240 Series will meet a wide array of design requirements. In addition to its two-lead construction, this series features ± 25% current ranges, current control over wide temperature ranges, and simple "floating" operation as no power supplies are required for biasing. Finally, its TO-18 hermetically sealed package is available with military processing per MIL-S-19500. (See Section 1.)

For additional design information please see typical performance curves as follows (Section 7):

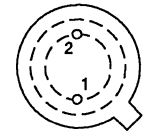
CRR0240–CRR0560 . . NKL
CRR0800–CRR1250 . . NKM
CRR1950–CRR4300 . . NKO

PART	I_F (mA)
CRR0240	0.24
CRR0360	0.36
CRR0560	0.56
CRR0800	0.80
CRR1250	1.25
CRR1950	1.95
CRR2900	2.90
CRR4300	4.30

TO-18 2 LEADS



BOTTOM VIEW



1 ANODE
2 CATHODE

SIMILAR PRODUCTS

- TO-92, See J500 Series
- 10% Ranges, See CR022 Series
- Chips, Order CRRXXXXCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Peak Operating Voltage	P_{OV}	100	V
Reverse Current	I_R	50	mA
Thermal Resistance	θ_{JC}	100	°C/W
Power Dissipation at T_C = 25°C	P_D	1.25	W
Operating Junction Temperature	T_J	-55 to 150	°C
Storage Temperature	T_{stg}	-55 to 200	

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

SYMBOL	I_F			Z_d		Z_k	V_L		POV		C_F	θ_1
PARAMETER	REGULATOR CURRENT			DYNAMIC IMPEDANCE		KNEE IMPEDANCE	LIMITING VOLTAGE		PEAK OPERATING VOLTAGE		CAPACITANCE	TEMPERATURE COEFFICIENT (TYPICALS)
TEST CONDITIONS	V_F = 25 V (Note 1)			V_F = 25 V (Note 2)		V_F = 6 V	$I_F = 0.8\ I_{F(MIN)}$ (Note 3)		$I_F = 1.1\ I_{F(MAX)}$ (Note 4)		V_F = 25 V f = 1 MHz	V_F = 25 V 0°C ≤ T_A ≤ 100°C
UNITS	mA			MΩ		MΩ	V		V		pF	ppm/°C
	NOM	MIN	MAX	MIN	TYP	TYP	MAX	TYP	MIN	TYP	TYP	TYP
CRR0240	0.24	0.180	0 300	5.00	15.50	3.00	1.00	0 45	100	180	2.2	1800
CRR0360	0.36	0.270	0.450	2.50	9.50	1.70	1 05	0.65	100	180	2.2	650
CRR0560	0.56	0.420	0.700	1.20	6.00	0 90	1.30	0.82	100	180	2.2	-200
CRR0800	0 80	0 600	1.000	0 80	7.80	1.40	1 35	0.95	100	180	4 2	-550
CRR1250	1.25	0.937	1.560	0.50	3.70	0.80	1.60	1.20	100	180	4.2	-1050
CRR1950	1 95	1 460	2 440	0.37	0 90	0.28	1 95	0 80	100	175	6 0	300
CRR2900	2 90	2.160	3.600	0.28	0.65	0.16	2.35	1.00	100	175	6 0	-400
CRR4300	4.30	3.240	5.400	0.22	0 40	0.10	3.00	1.25	100	175	6.0	-1125

NOTES:
1. Pulse test - steady state currents may very.
2. Pulse test - steady state impedances may vary.
3. Min V_F required to insure $I_F > 0.8\ I_{F(MIN)}$.
4. Max V_F where $I_F > 1\ 1\ I_{F(MAX)}$ is guaranteed.

DPAD1 SERIES

Siliconix incorporated

Dual Low-Leakage Pico-Amp Diodes

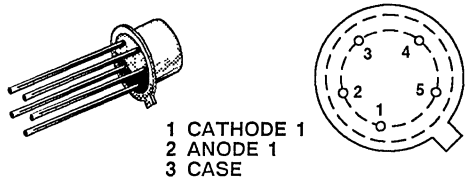
The DPAD1 Series of extremely low-leakage diodes provides a superior alternative to conventional diode technology when reverse current (leakage) must be minimized. These devices feature leakage currents ranging from −1 pA (DPAD1) to −100 pA (DPAD100) to support a wide range of applications. With two diodes per package, the DPAD1 Series is well suited for use in applications such as input protection for operational amplifiers. Its hermetically sealed metal can is available with full military processing per MIL-S-19500. (See Section 1.)

PART NO.	I_R (pA)
DPAD1	−1
DPAD2	−2
DPAD5	−5
DPAD10	−10
DPAD20	−20
DPAD50	−50
DPAD100	−100

SIMILAR PRODUCTS

- TO-92, See JPAD5 Series
- SOT-23, See SSTPAD5 Series
- TO-18, See PAD1 Series
- Chips, Order DPADXXCHP

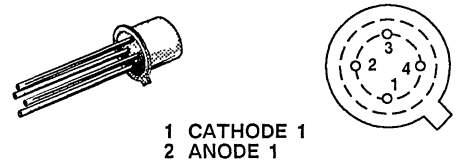
TO-78 (MODIFIED) **BOTTOM VIEW**



1 CATHODE 1
2 ANODE 1
3 CASE
4 CATHODE 2
5 ANODE 2

(DPAD1)

TO-71 (MODIFIED) **BOTTOM VIEW**



1 CATHODE 1
2 ANODE 1
3 CATHODE 2
4 ANODE 2

(DPAD2, 5, 10, 20, 50, 100)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Forward Current	I_F	50	mA
Total Device Dissipation	P_D	400	mW
Storage Temperature	T_{stg}	−55 to 125	°C
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS [1]

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS TYP [2]	LIMITS MIN	LIMITS MAX	UNIT
STATIC							
Reverse Current	I_R	V_R = -20 V	DPAD1	-0.2		-1	pA
			DPAD2	-1		-2	
			DPAD5	-2		-5	
			DPAD10	-3		-10	
			DPAD20	-5		-20	
			DPAD50	-10		-50	
			DPAD100	-15		-100	
Reverse Breakdown Voltage	BV_R	I_R = -1 µA	DPAD1, 2, 5	-60	-45	-120	V
			DPAD10, 20 DPAD50, 100	-55	-35		
Forward Voltage Drop	V_F	I_F = 1 mA		0.7		1.5	
DYNAMIC							
Reverse Capacitance	C_R	V_R = -5 V f = 1 MHz	DPAD1, 2,5	0.6		0.8	pF
			DPAD10, 20 DPAD50, 100	1		2	
Differential Capacitance	$\lvert C_{R1} - C_{R2} \rvert$	$V_{R1} = V_{R2}$ = -5 V, f = 1 MHz		0.07		0.2	

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.

4

J105 SERIES

Siliconix incorporated

N-Channel JFET

The J105 Series is a high-performance JFET analog switch designed to offer low on-resistance and fast switching. $r_{DS(ON)}$ <3 Ω is guaranteed with the J105 which makes this device the lowest of any commercially available JFET. This device is housed in a low-cost TO-92 package and offers a wide range of lead-forms and/or tape and reel options. (See Section 8.)

For further design information please consult the typical performance curves NVA which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	$I_{D(OFF)}$ TYP (pA)	t_{ON} TYP (ns)
J105	-10	3	10	14
J106	-6	6	10	14
J107	-4.5	8	10	14

SIMILAR PRODUCTS

- TO-52, See U290 Series
- Chips, Order J10XCHP

TO-92 BOTTOM VIEW

1 DRAIN
2 SOURCE
3 GATE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	
Gate Current	I_G	50	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature	T_J	-55 to 135	°C
Storage Temperature	T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				J105		J106		J107		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-35	-25		-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 5 V, I_D = 1 µA		-4.5	-10	-2	-6	-0.5	-4.5	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		500		200		100		mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-0.02		-3		-3		-3	nA
		T_A = 125°C	-10							
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 25 mA	-0.01							nA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 5 V, V_{GS} = -10 V	0.01		3		3		3	nA
		V_{DS} = 5 V, V_{GS} = -10 V, T_A = 125°C	5							nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, V_{DS} ≤ 0.1 V			3		6		8	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 25 mA, f = 1 kHz	55							mS
Common-Source Output Conductance	g_{os}	V_{DG} = 10 V, I_D = 25 mA, f = 1 kHz	5							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 mA, f = 1 kHz			3		6		8	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = 0 V, f = 1 MHz	120		160		160		160	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} = -10 V, f = 1 MHz	20		35		35		35	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 25 mA, f = 1 kHz	3							$nV/\sqrt{Hz}$
SWITCHING										
Turn-on Time	$t_{d(ON)}$	V_{DD} = 1.5 V, $V_{GS(ON)}$ = 0 V	6							ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	8							ns
Turn-off Time	$t_{d(OFF)}$	J105 28 mA -12 V 50 Ω J106 27 mA -7 V 50 Ω	5							ns
	t_f	J107 26 mA -5 V 50 Ω	9							ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

4

J108 SERIES

Siliconix incorporated

N-Channel JFET

The J108 Series is designed with high-performance analog switching applications in mind. It features low on-resistance, good off-isolation, and fast switching. The TO-92 package affords low-cost and a wide range of lead-forms and tape and reel options. (See Section 8.)

For further design information please consult the typical performance curves NIP which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	$I_{D(OFF)}$ TYP (pA)	t_{ON} TYP (ns)
J108	–10	8	20	4
J109	–6	12	20	4
J110	–4	18	20	4
J110A	–4	25	20	4

SIMILAR PRODUCTS

- SOT-23, See SST108 Series
- TO-52, See 2N5432 Series
- Chips, Order J1XXCHP

TO-92 BOTTOM VIEW

1 DRAIN
2 SOURCE
3 GATE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	–25	V
Gate-Source Voltage	V_{GS}	–25	
Gate Current	I_G	50	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature	T_J	–55 to 135	°C
Storage Temperature	T_{stg}	–55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS [1]			LIMITS					
				J108		J109		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-32	-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 5 V, I_D = 1 µA		-3	-10	-2	-6	V
Saturation Drain Current [3]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		80		40		mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-0.01		-3		-3	nA
		V_{GS} = -15 V, V_{DS} = 0 V, T_A = 125°C	-5					nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 10 mA	-0.01					nA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 5 V, V_{GS} = -10 V	0.02		3		3	nA
		V_{DS} = 5 V, V_{GS} = -10 V, T_A = 125°C	10					nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, V_{DS} = ≤ 0.1 V			8		12	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 5 V, I_D = 10 mA, f = 1 kHz	17					mS
Common-Source Output Conductance	g_{os}	V_{DG} = 5 V, I_D = 10 mA, f = 1 kHz	600					µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 mA, f = 1 kHz			8		12	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = 0 V, f = 1 MHz	60		85		85	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} = -10 V, f = 1 MHz	11		15		15	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 5 V, I_D = 10 mA, f = 1 kHz	3.5					$nV/\sqrt{Hz}$
SWITCHING								
Turn-on Time	$t_{d(ON)}$	V_{DD} = 1.5 V, $V_{GS(ON)}$ = 0 V	3					ns
	t_r	P/N: J108 — $I_{D(ON)}$ 10 mA, $V_{GS(OFF)}$ -12 V, R_L 150 Ω; J109 — 10 mA, -7 V, 150 Ω	1					ns
Turn-off Time	$t_{d(OFF)}$		4					ns
	t_f		18					ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

4

ELECTRICAL CHARACTERISTICS [1]			LIMITS					
				J110		J110A		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-32	-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 5 V, I_D = 1 µA		-0.5	-4	-0.5	-4	V
Saturation Drain Current [3]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		10		10		mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-0.01		-3		-3	nA
		V_{GS} = -15 V, V_{DS} = 0 V, T_A = 125°C	-5					
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 10 mA	-0.01					nA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 5 V, V_{GS} = -10 V	0.02		3		3	nA
		V_{DS} = 5 V, V_{GS} = -10 V, T_A = 125°C	10					nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, V_{DS} ≤ 0.1 V			18		25	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 5 V, I_D = 10 mA, f = 1 kHz	17					mS
Common-Source Output Conductance	g_{os}	V_{DG} = 5 V, I_D = 10 mA, f = 1 kHz	600					µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0, f = 1 kHz			18		25	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = 0 V, f = 1 MHz	60		85		85	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} = -10 V, f = 1 MHz	11		15		15	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 5 V, I_D = 10 mA, f = 1 kHz	3.5					$nV/\sqrt{Hz}$
SWITCHING								
Turn-on Time	$t_{d(ON)}$	V_{DD} = 1.5 V, $V_{GS(ON)}$ = 0 V	3					ns
	t_r	P/N: J110, J110A; $I_{D(ON)}$: 10 mA, 10 mA; $V_{GS(OFF)}$: -5 V, -5 V; R_L: 150 Ω, 150 Ω	1					ns
Turn-off Time	$t_{d(OFF)}$		4					ns
	t_f		20					ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

J111 SERIES

N-Channel JFET

The J111 Series is a low-cost, all-purpose analog switch designed to support a wide range of applications. It features low on-resistance, capacitance and good off-isolation. Additionally, our TO-92 package allows a variety of lead-forms or tape and reel combinations. (See Section 8.)

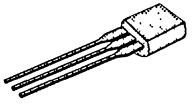
For further design information please consult the typical performance curves NCB which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	$I_{D(OFF)}$ TYP (pA)	t_{ON} TYP (ns)
J111	–10	30	5	4
J112	–5	50	5	4
J113	–3	100	5	4

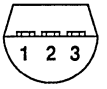
SIMILAR PRODUCTS

- SOT-23, See SST111 Series
- TO-18, See 2N4391 Series
- Duals, See 2N5564 Series
- Chips, Order J11XCHP

TO-92



BOTTOM VIEW



1 DRAIN
2 SOURCE
3 GATE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	–35	V
Gate-Source Voltage	V_{GS}	–35	
Gate Current	I_G	50	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature	T_J	–55 to 135	°C
Storage Temperature	T_{stg}	–55 to 200	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				J111		J112		J113		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-55	-35		-35		-35		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 5 V, I_D = 1 µA		-3	-10	-1	-5		-3	V
Saturation Drain Current [3]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		20		5		2		mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-0.005		-1		-1		-1	nA
		T_A = 125°C	-3							
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 10 mA	-5							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 5 V, V_{GS} = -10 V	0.005		1		1		1	nA
		V_{DS} = 5 V, V_{GS} = -10 V, T_A = 125°C	3							
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, V_{DS} = 0.1 V			30		50		100	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 20 V, I_D = 1 mA, f = 1 kHz	6							mS
Common-Source Output Conductance	g_{os}		25							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V, f = 1 kHz			30		50		100	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = -10 V, f = 1 MHz	7		12		12		12	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		3		5		5		5	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 1 mA, f = 1 kHz	4							$nV/\sqrt{Hz}$
SWITCHING										
Turn-on Time	$t_{d(ON)}$	V_{DD} = 10 V, $V_{GS(ON)}$ = 0 V	2							ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	2							
Turn-off Time	$t_{d(OFF)}$	J111 12 mA -12 V 800 Ω J112 6 mA -7 V 1600 Ω	6							
	t_f	J113 3 mA -5 V 3200 Ω	15							

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

Siliconix incorporated

J111A SERIES

N-Channel JFET

The J111A Series is a low-cost, all-purpose analog switch designed to support a wide range of applications. In addition to low on-resistance and capacitance, this series guarantees higher breakdown voltage and significantly lower leakage than its counterpart, the J111 Series. Finally, its TO-92 package allows a variety of lead-forms or tape and reel combinations. (See Section 8.)

For further design information please consult the typical performance curves NCB which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	$I_{D(OFF)}$ MAX (pA)	t_{ON} TYP (ns)
J111A	-10	30	200	4
J112A	-7	50	200	4
J113A	-5	80	200	4

TO-92 BOTTOM VIEW

1 DRAIN
2 SOURCE
3 GATE

SIMILAR PRODUCTS

- SOT-23, See SST111 Series
- TO-18, See 2N4391 Series
- Duals, See 2N5564 Series
- Chips, Order J11XACHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-40	V
Gate-Source Voltage	V_{GS}	-40	
Gate Current	I_G	50	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature	T_J	-55 to 135	°C
Storage Temperature	T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

4

ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				J111A		J112A		J113A		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-55	-40		-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 5 V, I_D = 1 µA		-5	-10	-2	-7	-1	-5	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		30		15		8		mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-5		-200		-200		-200	pA
		T_A = 125°C	-3							nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 10 mA	-5							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 5 V, V_{GS} = -10 V	5		200		200		200	pA
		V_{DS} = 5 V, V_{GS} = -10 V, T_A = 125°C	3							nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, V_{DS} = 0.1 V			30		50		80	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 20 V, I_D = 1 mA, f = 1 kHz	6							mS
Common-Source Output Conductance	g_{os}		25							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V, f = 1 kHz			30		50		80	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = -10 V, f = 1 MHz	7		12		12		12	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		3		5		5		5	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 1 mA, f = 1 kHz	4							$nV/\sqrt{Hz}$
SWITCHING										
Turn-on Time	$t_{d(ON)}$	V_{DD} = 10 V, $V_{GS(ON)}$ = 0 V	2							ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	2							ns
Turn-off Time	$t_{d(OFF)}$	J111A 12 mA -12 V 800 Ω J112A 6 mA -7 V 1600 Ω	6							ns
	t_f	J113A 3 mA -5 V 3200 Ω	15							ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

Siliconix incorporated

J174 SERIES

P-Channel JFET

The J174 Series is a low-cost p-channel analog switch designed to provide low on-resistance and fast switching. It also works well in conjunction with Siliconix' J111 Series for complimentary switching applications. It features a TO-92 package which is available with various lead-forms and/or tape and reel options. (See Section 8.)

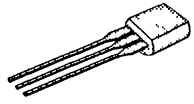
For further design information please consult the typical performance curves PSCIA which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	$I_{D(OFF)}$ MAX (nA)	t_{ON} TYP (ns)
J174	10	85	–1	25
J175	6	125	–1	25
J176	4	250	–1	25
J177	2.25	300	–1	25

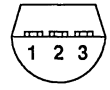
SIMILAR PRODUCTS

- TO-18, See 2N5114 Series
- SOT-23, See SST174 Series
- Chips, Order J17XCHP

TO-92



BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	30	V
Gate-Source Voltage	V_{GS}	30	
Gate Current	I_G	–50	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature	T_J	–55 to 135	°C
Storage Temperature	T_{stg}	–55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

4

ELECTRICAL CHARACTERISTICS [1]			LIMITS					
				J174		J175		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA, V_{DS} = 0 V	45	30		30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = −15 V, I_D = −10 nA		5	10	3	6	V
Saturation Drain Current [3]	I_{DSS}	V_{DS} = −15 V, V_{GS} = 0 V		−20	−135	−7	−70	mA
Gate Reverse Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	0.01		1		1	nA
		T_A = 125°C	5					
Gate Operating Current	I_G	V_{DG} = −15 V, I_D = −1 mA	0.01					nA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = −15 V, V_{GS} = 10 V	−0.01		−1		−1	nA
		V_{DS} = −15 V, V_{GS} = 10 V, T_A = 125°C	−5					nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, V_{DS} = −0.1 V			85		125	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = −1 mA, V_{DS} = 0 V	−0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = −15 V, I_D = −1 mA, f = 1 kHz	4.5					mS
Common-Source Output Conductance	g_{os}		20					µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 mA, f = 1 kHz			85		125	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = 0 V, f = 1 MHz	20					pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} = 10 V, f = 1 MHz	5					pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = −10 V, I_D = −1 mA, f = 1 kHz	20					$nV/\sqrt{Hz}$
SWITCHING								
Turn-on Time	$t_{d(ON)}$	$V_{GS(ON)}$ = 0 V	10					ns
	t_r	P/N: J174 / J175; V_{DD}: −10 V / −6 V; $V_{GS(OFF)}$: 12 V / 8 V; R_L: 560 Ω / 1200 Ω	15					ns
Turn-off Time	$t_{d(OFF)}$		10					ns
	t_f		20					ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

J174 SERIES

ELECTRICAL CHARACTERISTICS [1]			LIMITS					
				J176		J177		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA, V_{DS} = 0 V	45	30		30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = −15 V, I_D = −10 nA		1	4	0.8	2.25	V
Saturation Drain Current [3]	I_{DSS}	V_{DS} = −15 V, V_{GS} = 0 V		−2	−35	−1.5	−20	mA
Gate Reverse Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	0.01		1		1	nA
		V_{GS} = 20 V, V_{DS} = 0 V, T_A = 125°C	5					nA
Gate Operating Current	I_G	V_{DG} = −15 V, I_D = −1 mA	0.01					nA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = −15 V, V_{GS} = 10 V	−0.01		−1		−1	nA
		V_{DS} = −15 V, V_{GS} = 10 V, T_A = 125°C	−5					nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, V_{DS} = −0.1 V			250		300	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = −1 mA, V_{DS} = 0 V	−0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = −15 V, I_D = −1 mA, f = 1 kHz	4.5					mS
Common-Source Output Conductance	g_{os}	V_{DS} = −15 V, I_D = −1 mA, f = 1 kHz	20					µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 mA, f = 1 kHz			250		300	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = 0 V, f = 1 MHz	20					pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} = 10 V, f = 1 MHz	5					pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = −10 V, I_D = −1 mA, f = 1 kHz	20					$nV/\sqrt{Hz}$
SWITCHING								
Turn-on Time	$t_{d(ON)}$	$V_{GS(ON)}$ = 0 V	10					ns
	t_r		15					ns
Turn-off Time	$t_{d(OFF)}$		10					ns
	t_f		20					ns

P/N	V_{DD}	$V_{GS(OFF)}$	R_L
J176	−6 V	6 V	5600 Ω
J177	−6 V	3 V	10000 Ω

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

4

J201 SERIES

Siliconix incorporated

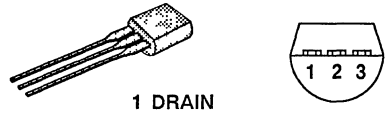
N-Channel JFETs

The J201 Series of popular, low-cost JFETs offers high performance in a wide range of applications. With features such as 100 pA gate leakage, –40 V breakdown voltage, and 5 nV/√Hz noise, these devices are especially characterized for sensitive amplifier stages. The J201 and J204 with low cut off voltages, are ideal for battery operated equipment and low current amplifiers. The J201 Series in the TO-92 package offers both value and compatibility with automated assembly.

For further design information please consult the typical performance curves NPA which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
J201	–1.5	–40	0.5	1
J202	–4	–40	1	4.5
J203	–10	–40	1.5	20
J204	–2	–25	0.5	3

TO-92 BOTTOM VIEW



1 DRAIN
2 SOURCE
3 GATE

SIMILAR PRODUCTS

- TO-18, See 2N4338 Series
- SOT-23, See SST201 Series
- Chips, Order J20XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT		UNITS
		J201-3	J204	
Gate-Drain Voltage	V_{GD}	–40	–25	V
Gate-Source Voltage	V_{GS}	–40	–25	
Gate Current	I_G	50		mA
Power Dissipation	P_D	360		mW
Power Derating		3.27		mW/°C
Operating Junction Temperature	T_J	–55 to 135		°C
Storage Temperature	T_{stg}	–55 to 150		
Lead Temperature (1/16" from case for 10 seconds)	T_L	300		

ELECTRICAL CHARACTERISTICS [1]			LIMITS					
				J201		J202		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-57	-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 20 V, I_D = 10 nA		-0.3	-1.5	-0.8	-4	
Saturation Drain Current [3]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V		0.2	1	0.9	4.5	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-2		-100		-100	pA
		T_A = 125°C	-1					nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 0.1 mA	-2					pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 15 V, V_{GS} = -10 V	2					
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 kHz		0.5		1		mS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	4.5					pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.3					
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	6					$nV/\sqrt{Hz}$

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

4

ELECTRICAL CHARACTERISTICS [1]			LIMITS					
				J203		J204		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-57	-40		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 20 V, I_D = 10 nA		-2	-10	-0.3	-2	V
Saturation Drain Current [3]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V		4	20	0.2	3	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-2		-100		-100	pA
		T_A = 125°C	-1					nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 0.1 mA	-2					pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 15 V, V_{GS} = -10 V	2					pA
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 kHz		1.5		0.5		mS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	4.5					pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.3					pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	6					$nV/\sqrt{Hz}$

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

J210 SERIES

N-Channel JFETs

The J210 Series of n-channel JFETs provides good general purpose amplifiers for a wide range of test and instrumentation applications. This series features low-leakage (I_{GSS} < 100 pA), high gain (g_{fs} > 7 mS for J212), and low noise. Additionally, its low cost TO-92 package ensures value as well as compatibility with automated assembly techniques. (See Section 8.)

For additional design information please see performance curves NZF, which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
J210	-3	-25	4	15
J211	-4.5	-25	6	20
J212	-6	-25	7	40

SIMILAR PRODUCTS

- Duals, See 2N5911 Series
- Chips, Order J21XCHP

TO-92 BOTTOM VIEW

1 DRAIN
2 SOURCE
3 GATE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	
Gate Current	I_G	10	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature	T_J	-55 to 135	°C
Storage Temperature	T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

4

ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				J210		J211		J212		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-35	-25		-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 1 nA		-1	-3	-2.5	-4.5	-4	-6	
Saturation Drain Current [3]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		2	15	7	20	15	40	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-1		-100		-100		-100	pA
		T_A = 125°C	-0.5							nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 1 mA	-1							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 10 V, V_{GS} = -8 V	1							
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 kHz		4	12	6	12	7	12	mS
Common-Source Output Conductance	g_{os}				150		200		200	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	4							pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.5							
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 kHz	5							$nV/\sqrt{Hz}$

NOTES:
1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

Siliconix incorporated

J230 SERIES

N-Channel JFETs

The J230 Series of popular, low-cost JFETs offers high performance in a wide range of applications. It features low leakage, noise and cutoff voltage for use with low level power supplies. Its TO-92 package offers both value and compatibility with automated assembly.

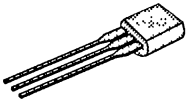
For further design information please consult the typical performance curves NPA which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
J230	-3	-40	1	3
J231	-5	-40	1.5	6
J232	-6	-40	2.5	10

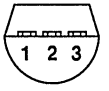
SIMILAR PRODUCTS

- TO-18, See 2N4338 Series
- SOT-23, See SST201 Series
- Chips, Order J23XCHP

TO-92



BOTTOM VIEW



1 DRAIN
2 SOURCE
3 GATE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-40	V
Gate-Source Voltage	V_{GS}	-40	
Gate Current	I_G	50	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature	T_J	-55 to 135	°C
Storage Temperature	T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

4

ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				J230		J231		J232		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-57	-40		-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 20 V, I_D = 1 µA		-0.5	-3	-1.5	-5	-3	-6	V
Saturation Drain Current [3]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V		0.7	3	2	6	5	10	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -30 V, V_{DS} = 0 V	-2		-250		-250		-250	pA
		T_A = 125°C	-1							nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 0.5 mA	-1							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 15 V, V_{GS} = -10 V	2							pA
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 kHz		1	3.5	1.5	4	2.5	5	mS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	4.5							pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.3							pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 10 Hz	14		30		30		30	$nV/\sqrt{Hz}$

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

Siliconix incorporated

J270 SERIES

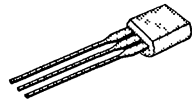
P-Channel JFET

The J270 Series is an all-purpose amplifier for designs requiring p-channel operation. These devices feature high gain, low noise and tight $V_{GS(OFF)}$ limits for simple circuit design. They are available in low-cost TO-92 packages and are fully compatible with automatic insertion techniques. (See Section 8 for details.)

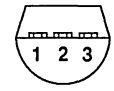
For further design information please consult the typical performance curves PSCIA which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
J270	2.0	30	6	-15
J271	4.5	30	8	-50

TO-92



BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

SIMILAR PRODUCTS

- SOT-23, See SST270 Series
- Chips, Order J27XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	30	V
Gate-Source Voltage	V_{GS}	30	
Gate Current	I_G	-50	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature	T_J	-55 to 135	°C
Storage Temperature	T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

4

ELECTRICAL CHARACTERISTICS [1]			LIMITS					
				J270		J271		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA, V_{DS} = 0 V	45	30		30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = −15 V, I_D = −1 nA		0.5	2.0	1.5	4.5	
Saturation Drain Current [3]	I_{DSS}	V_{DS} = −15 V, V_{GS} = 0 V		−2	−15	−6	−50	mA
Gate Reverse Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	10		200		200	pA
		V_{DS} = 0 V, T_A = 125°C	5					nA
Gate Operating Current	I_G	V_{DG} = −15 V, I_D = −1 mA	10					pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = −15 V, V_{GS} = 10 V	−10					
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = −1 mA, V_{DS} = 0 V	−0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = −15 V, V_{GS} = 0 V, f = 1 kHz		6	15	8	18	mS
Common-Source Output Conductance	g_{os}				200		500	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = −15 V, V_{GS} = 0 V, f = 1 MHz	20					pF
Common-Source Reverse Transfer Capacitance	C_{rss}		4					
Equivalent Input Noise Voltage	$\overline{e}_n$	V_{DS} = −10 V, V_{GS} = 0 V, f = 1 kHz	20					$nV/\sqrt{Hz}$

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

J304 SERIES

N-Channel JFETs

The J304 Series of n-channel JFETs is designed to provide high-performance amplification, especially at high-frequency. These parts feature low noise, high gain and provide wide bandwidth.

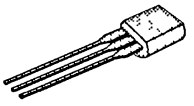
For additional design information please see performance curves NH, which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
J304	-6	-30	4.5	15
J305	-3	-30	3	8

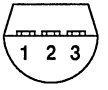
SIMILAR PRODUCTS

- SOT-23, See SST5484 Series
- TO-72, See PN4416 Series
- Chips, Order J30XCHP

TO-92



BOTTOM VIEW



1 DRAIN
2 SOURCE
3 GATE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-30	V
Gate-Source Voltage	V_{GS}	-30	
Gate Current	I_G	10	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature	T_J	-55 to 135	°C
Storage Temperature	T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

4

ELECTRICAL CHARACTERISTICS[1]			LIMITS					
				J304		J305		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-35	-30		-30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 1 nA		-2	-6	-0.5	-3	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		5	15	1	8	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-2		-100		-100	pA
		V_{GS} = -20 V, V_{DS} = 0 V, T_A = 100°C	-0.2					nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 1 mA	-20					pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 10 V, V_{GS} = -6 V	2					pA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 1 V, I_D = 1 mA	200					Ω
Gate-Source Forward Voltage	$V_{GS(f)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 kHz		4.5	7.5	3		mS
Common-Source Output Conductance	g_{os}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 kHz			50		50	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	2.2					pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	0.7					pF
Common-Source Output Capacitance	C_{oss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	1					pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 100 Hz	10					$nV/\sqrt{Hz}$

ELECTRICAL CHARACTERISTICS[1]			LIMITS (Typical)				
			J304		J305		
PARAMETER	SYMBOL	TEST CONDITIONS	100 MHz	400 MHz	100 MHz	400 MHz	UNIT
HIGH-FREQUENCY							
Common-Source Input Conductance	g_{iss}	V_{DS} = 15 V, V_{GS} = 0 V	80	800	80		µS
Common-Source Input Susceptance	b_{iss}	V_{DS} = 15 V, V_{GS} = 0 V	2	7.5	2		mS
Common-Source Output Conductance	g_{oss}	V_{DS} = 15 V, V_{GS} = 0 V	60	80	60		µS
Common-Source Output Susceptance	b_{oss}	V_{DS} = 15 V, V_{GS} = 0 V	0.8	3.6	0.8		mS
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V		4.2	3		mS
Common-Source Power Gain	G_{ps}	V_{DS} = 15 V, I_D = 5 mA	20	11			dB
Noise Figure	NF	V_{DS} = 15 V, I_D = 5 mA, R_G = 1 kΩ	1.7	3.8			dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

Siliconix incorporated

J308 SERIES

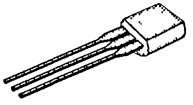
N-Channel JFETs

The J308 Series is a popular, low-cost device which offers superb amplification characteristics. It features high-gain, low noise (typically < 6 $nV\sqrt{Hz}$) and low gate leakage (typically < 2 pA). Of special interest, however, is performance at high frequency. Even at 450 MHz the J308 Series offers high power gain and low noise. Like all TO-92 packages offered by Siliconix, tape and reel options are available to support automated assembly. (See Section 8.)

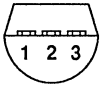
For additional design information and a closer look at high-frequency characteristics, please consult performance curves NZB which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
J308	-6.5	-25	8	60
J309	-4.0	-25	10	30
J310	-6.5	-25	8	60

TO-92



BOTTOM VIEW



1 DRAIN
2 SOURCE
3 GATE

SIMILAR PRODUCTS

- TO-52, See U308 Series
- SOT-23, See SST308 Series
- Dual, See U430 Series
- Chips, Order J30XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	
Gate Current	I_G	10	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature	T_J	-55 to 135	°C
Storage Temperature	T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS [1]				LIMITS							
					J308		J309		J310		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP [2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC											
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V		-35	-25		-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA			-1	-6.5	-1	-4	-2	-6.5	
Saturation Drain Current [3]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V			12	60	12	30	24	60	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V		-0.002		-1		-1		-1	nA
			T_A = 125°C	-0.008		-1		-1		-1	µA
Gate Operating Current	I_G	V_{DG} = 9 V, I_D = 10 mA		-15							pA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA		35							Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V		0.7		1		1		1	V
DYNAMIC											
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 10 mA, f = 1 kHz		14	8		10		8		mS
Common-Source Output Conductance	g_{os}			110		250		250		250	µS
Common-Source Input Capacitance	C_{iss}	V_{GS} = -10 V, V_{DS} = 10 V, f = 1 MHz		4		5		5		5	pF
Common-Source Reverse Transfer Capacitance	C_{rss}			1.9		2.5		2.5		2.5	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, I_D = 10 mA, f = 100 Hz		6							$nV/\sqrt{Hz}$
HIGH FREQUENCY											
Common-Gate Foward Transconductance	g_{fg}	V_{DS} = 10 V, I_D = 10 mA	f = 105 MHz	15							mS
			f = 450 MHz	13							
Common-Gate Output Conductance	g_{og}		f = 105 MHz	0.16							
			f = 450 MHz	0.55							
Common-Gate Power Gain [4]	G_{pg}		f = 105 MHz	16							dB
			f = 450 MHz	11.5							
Noise Figure	NF		f = 105 MHz	1.5							
			f = 450 MHz	2.7							

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.
4. Gain (G_{pg}) measured at optimum input noise match.

Siliconix incorporated

J500 SERIES

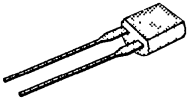
Current Regulator Diodes

The J500 Series is a family of current regulators designed for demanding applications in test equipment and instrumentation. These devices utilize the JFET techniques to produce a single two-leaded device which is extremely simple to operate. With nominal current ranges from 0.24 mA to 4.7 mA, the J500 Series will meet a wide array of design requirements. In addition to its two-lead construction, this series features 20% current ranges, improved current control over wide temperature ranges, and simple "floating" operation as no power supplies are required for biasing. Several of the devices provide effective current control operating down to even 1 volt. Finally, its low-cost TO-92 package ensures a cost effective design solution.

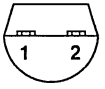
For additional design information please see performance curves NCL, which are located in Section 7.

PART	I_F (mA)	PART	I_F (mA)
J500	0.24	J506	1.40
J501	0.33	J507	1.80
J502	0.43	J508	2.40
J503	0.56	J509	3.00
J504	0.75	J510	3.60
J505	1.00	J511	4.70

TO-92



BOTTOM VIEW



1 ANODE
2 CATHODE

SIMILAR PRODUCTS

- TO-18, See CR022 Series
- Chips, Order J5XXCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Peak Operating Voltage	P_{OV}	50	V
Forward Current	I_F	20	mA
Reverse Current	I_R	50	
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/ °C
Operating Junction Temperature	T_J	-55 to 150	°C
Storage Temperature	T_{stg}	-55 to 200	

4

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

SYMBOL	I_F			Z_d		Z_k	V_L		POV		C_F	θ_1
PARAMETER	REGULATOR CURRENT			DYNAMIC IMPEDANCE		KNEE IMPEDANCE	LIMITING VOLTAGE		PEAK OPERATING VOLTAGE		CAPACITANCE	TEMPERATURE COEFFICIENT (TYPICALS)
TEST CONDITIONS	V_F = 25 V (Note 1)			V_F = 25 V (Note 2)		V_F = 6 V	I_F = 0.8 $I_{F(MIN)}$ (Note 3)		I_F = 1.1 $I_{F(MAX)}$ (Note 4)		V_F = 25 V f = 1 MHz	V_F = 25 V 0°C ≤ T_A ≤ 100°C
UNITS	mA			MΩ		MΩ	V		V		pF	ppm/°C
	NOM	MIN	MAX	MIN	TYP	TYP	MAX	TYP	MIN	TYP	TYP	TYP
J500	0.24	0.192	0.288	4.00	40 0	2.50	1.20	0.4	50	100	2.2	1300
J501	0.33	0.264	0 396	2.20	25 0	1.60	1.30	0.5	50	100	2.2	600
J502	0.43	0.344	0.516	1.50	15.0	1.10	1.50	0.6	50	100	2.2	0
J503	0.56	0.448	0.672	1.20	12.0	0.80	1.70	0.7	50	100	2 2	-400
J504	0.75	0.600	0.900	0.80	7 0	0 55	1.90	0.8	50	100	2.2	-1000
J505	1.00	0 800	1.200	0.50	5.0	0.40	2.10	0.9	50	100	2.2	-1300
J506	1.40	1.120	1.680	0.33	3 0	0.25	2.50	1.1	50	100	2.2	-1900
J507	1.80	1.440	2.160	0.20	2 0	0.19	2.80	1.3	50	100	2.2	-2200
J508	2.40	1.900	2.900	0.20	1 5	0.13	3.10	1 5	50	100	2 2	-2600
J509	3.00	2.400	3.600	0.15	1.0	0.09	3.50	1.7	50	100	2.2	-2800
J510	3.60	2.900	4.300	0.15	0.8	0.07	3.90	1.9	50	100	2 2	-3000
J511	4.70	3.800	5.600	0.12	0 6	0.05	4.20	2.1	50	100	2 2	-3000

NOTES:
1. Pulse test - steady state currents may very.
2. Pulse test - steady state impedances may vary.
3. Min V_F required to insure $I_F > 0.8\ I_{F(MIN)}$.
4. Max V_F where $I_F > 1.1\ I_{F(MAX)}$ is guaranteed

J552

Current Regulator Diode

The J552 is a current regulator designed for applications in test equipment and instrumentation. With forward current between 0.2 and 0.7 mA, the J552 will meet a wide array of design requirements. In addition to its two-lead construction, it features current control over wide temperature ranges and simple "floating" operation as no power supplies are required for biasing. Finally, the low-cost TO-92 package ensures a cost effective design solution.

For additional design information please see performance curves NKL, which are located in Section 7.

PART	I_F (mA)
J552	0.77

TO-92 BOTTOM VIEW

1 ANODE
2 CATHODE

SIMILAR PRODUCTS

- TO-18, See CR022 Series
- Chips, Order J5XXCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Peak Operating Voltage	P_{OV}	100	V
Forward Current	I_F	20	mA
Reverse Current	I_R	50	
Power Dissipation	P_D	350	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature	T_J	-55 to 135	°C
Storage Temperature	T_{stg}	-55 to 135	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				J552		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Forward Current [3]	I_{F1}	V_F = 100 V	400		770	μA
		V_F = 25 V	400	250	700	
		V_F = 1 V	390	200		
Peak Operating Voltage [3, 4]	P_{OV}	I_F = 100 V $I_{F1(MAX)}$	160	100		V
Limiting Voltage [5]	V_L	I_F = 0.9 $I_{F1(MIN)}$	1		1.5	
DYNAMIC						
Small-Signal Dynamic Impedance [3]	Z_{F1}	V_F = 25 V, f = 1 kHz	8	1		MΩ
Anode-Cathode Capacitance	C_F	V_F = 25 V, f = 1 MHz	2			pF

NOTES:
1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 μs, duty cycle ≤ 3%.
4. Maximum $V_F < 1.1\ I_{F1(MAX)}$ is guaranteed.
5. Maximum V_F required to insure $I_F > 0.9\ I_{F1(MIN)}$.

J553 SERIES

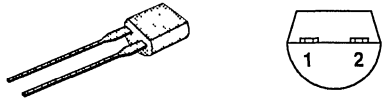
Current Regulator Diodes

The J553 Series is a low cost family of current regulators designed for demanding applications in test equipment and instrumentation. These devices utilize the proven JFET techniques to produce a single two-leaded device which is extremely simple to operate. With nominal current ranges from 0.5 mA to 4.5 mA, the J553 Series will meet a wide array of design requirements. In addition to its two-lead construction, this series feature improved current control over wide temperature ranges and simple "floating" operation as no power supplies are required for biasing. Several of the devices provide effective current control operating down to even 2 volts. Finally, its low-cost TO-92 package ensures a cost effective design solution.

For additional design information please see performance curves NCL, which are located in Section 7.

PART	I_F (mA)
J553	0.50
J554	1.00
J555	2.00
J556	3.00
J557	4.50

TO-92 BOTTOM VIEW



1 ANODE
2 CATHODE

SIMILAR PRODUCTS

- TO-18, See CR022 Series
- Chips, Order J5XXCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Peak Operating Voltage	P_{OV}	50	V
Forward Current	I_F	20	mA
Reverse Current	I_R	50	
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature	T_J	-55 to 150	°C
Storage Temperature	T_{stg}	-55 to 200	

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

SYMBOL	I_F			Z_d	Z_k	V_L		POV		C_F	θ_1
PARAMETER	REGULATOR CURRENT			DYNAMIC IMPEDANCE	KNEE IMPEDANCE	LIMITING VOLTAGE		PEAK OPERATING VOLTAGE		CAPACITANCE	TEMPERATURE COEFFICIENT (TYPICALS)
TEST CONDITIONS	V_F = 25 V (Note 1)			V_F = 25 V (Note 2)	V_F = 6 V	$I_F = 0.8\ I_{F(MIN)}$ (Note 3)		$I_F = 1.1\ I_{F(MAX)}$ (Note 4)		V_F = 25 V f = 1 MHz	V_F = 25 V 0°C ≤ T_A ≤ 100°C
UNITS	mA			MΩ	MΩ	V		V		pF	ppm/°C
	NOM	MIN	MAX	TYP	TYP	MAX	TYP	MIN	TYP	TYP	TYP
J553	0.50	0.180	0.750	13.0	1.00	1.30	0 7	50	100	2.2	-200
J554	1.00	0.600	1.600	5.0	0.40	1.75	0 9	50	100	2.2	-1300
J555	2.00	1.400	2.600	1.8	0.17	2.15	1.4	50	100	2.2	-2300
J556	3.00	2.400	3 800	1.0	0 09	2.60	1.7	50	100	2.2	-2800
J557	4.50	3.600	5.300	0.6	0.06	3.00	2.1	50	100	2.2	-3100

NOTES:
1. Pulse test - steady state currents may very.
2. Pulse test - steady state impedances may vary.
3. Min V_F required to insure $I_F > 0.8\ I_{F(MIN)}$.
4. Max V_F where $I_F > 1.1\ I_{F(MAX)}$ is guaranteed.

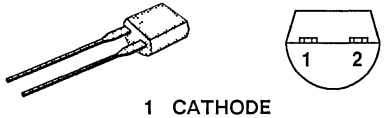
JPAD5 SERIES

Low-Leakage Pico-Amp Diodes

The JPAD5 Series of low-leakage diodes provides a superior alternative to conventional diode technology when reverse current (leakage) must be minimized. These devices feature leakage currents ranging from -5 pA (JPAD5) to -500 pA (JPAD500) to support varying system requirements. Its TO-92 package allows designers to maximize circuit performance while maintaining the objectives of low cost and compact packaging. Tape and reel is available for use with automated assembly techniques. (See Section 8.)

PART NO.	I_R (pA)
JPAD5	-5
JPAD10	-10
JPAD20	-20
JPAD50	-50
JPAD100	-100
JPAD200	-200
JPAD500	-500

TO-92 BOTTOM VIEW



1 CATHODE
2 ANODE

SIMILAR PRODUCTS

- SOT-23, See SSTPAD5 Series
- TO-18, See PAD1 Series
- Duals, See DPAD1 Series
- Chips, Order JPADXXCHP

4

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Forward Current	I_F	10	mA
Total Device Dissipation	P_D	360	mW
Storage Temperature	T_{stg}	-55 to 135	°C
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS [1]							
PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS TYP [2]	LIMITS MIN	LIMITS MAX	UNIT
STATIC							
Reverse Current	I_R	V_R = -20 V	JPAD5	-1		-5	pA
			JPAD10	-2		-10	
			JPAD20	-2		-20	
			JPAD50	-5		-50	
			JPAD100	-5		-100	
			JPAD200	-20		-200	
			JPAD500	-20		-500	
Reverse Breakdown Voltage	BV_R	I_R = -1 µA		-60	-35		V
Forward Voltage Drop	V_F	I_F = 5 mA		0.8		1.5	
DYNAMIC							
Reverse Capacitance	C_R	V_R = -5 V, f = 1 MHz		1.5		2	pF

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.

JR135V SERIES

High-Voltage Current Limiting Diodes

The JR135V Series of high-voltage diodes utilizes a MOS process to provide active current limiting over a voltage range from 1 V up to 240 V. These devices feature two-terminal construction and require no additional circuitry or power supplies. Additionally, it is housed in a low-cost TO-92 package and is available with tape and reel to support automated assembly.

For additional design information please see performance curves VRMA, which are located in Section 7.

PART NO.	P_{OV} (V)
JR135V	135
JR170V	170
JR200V	200
JR220V	220
JR240V	240

TO-92 BOTTOM VIEW

1 ANODE
2 CATHODE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMIT	UNITS
Peak Anode-Cathode Voltage	JR135V	P_{OV}	135	V
	JR170V		170	
	JR200V		200	
	JR220V		220	
	JR240V		240	
Reverse Current		I_R	50	mA
Power Dissipation		P_D	360	mW
Power Derating			3.27	mW/°C
Operating Junction Temperature		T_J	-55 to 135	°C
Storage Temperature		T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

4

ELECTRICAL CHARACTERISTICS [1]							
PARAMETER	SYMBOL	TEST CONDITIONS		TYP [2]	LIMITS MIN	LIMITS MAX	UNIT
STATIC							
Peak Operating Voltage	P_{OV}	I_F = 1 mA	JR135V	165	135		V
			JR170V	190	170		
			JR200V	215	200		
			JR220V	230	220		
			JR240V	260	240		
Forward Current	I_F	V_F = 2 V		440	200		μA
		V_F = 100 V		450	200	770	
Limiting Voltage	V_L	I_F = 0.8 I_F @ 2 V min		0.7		0.9	V
DYNAMIC							
Dynamic Impedance	Z_D	V_F = 25 V		2			MΩ
Temperature Coefficient	$\frac{\Delta I_F}{\Delta T}$	V_F = 2 to 100 V T_A = −20 to 85°C		0.6			%/°C

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.

Siliconix incorporated

M440 SERIES

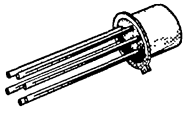
N-Channel JFET Pairs

The M440 Series are monolithic pairs of JFETs mounted in a single TO-71 package. The M440 features high speed amplification (slew rate), high gain (typically > 6 mS), and low gate leakage (typically < 1 pA). This performance makes these devices perfect for use as wideband differential amplifiers in demanding test and measurement applications. Finally, its TO-71 hermetically sealed package is available with military screening per MIL-S-19500. (See Section 1.)

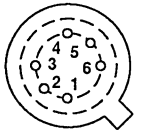
For additional design information please see performance curves NNZ, which are located in Section 7.

PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G TYP (pA)	$\lvert V_{GS_1} - V_{GS_2} \rvert$ MAX (mV)
M440	-25	5	-1	10
M441	-25	5	-1	20

TO-71



BOTTOM VIEW



1 SOURCE 1
2 DRAIN 1
3 GATE 1
4 SOURCE 2
5 DRAIN 2
6 GATE 2

SIMILAR PRODUCTS

- TO-78, See U443 Series
- SO-8, See SST440 Series
- Low Noise, See U401 Series
- Low Leakage, See U421 Series
- Chips, Order M44XCHP

4

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMIT	UNITS
Gate-Drain Voltage		V_{GD}	-25	V
Gate-Source Voltage		V_{GS}	-25	
Forward Gate Current		I_G	50	mA
Power Dissipation	Per Side	P_D	325	mW
	Total		650	
Power Derating	Per Side		2.2	mW/°C
	Total		3.3	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature		T_{stg}	-65 to 200	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

Siliconix incorporated

ELECTRICAL CHARACTERISTICS[1]			LIMITS					
				M440		M441		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-35	-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA	-3.5	-1	-6	-1	-6	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	15	6	30	6	30	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-1		-500		-500	pA
		T_A = 125°C	-0.2					nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 5 mA	-1		-500		-500	pA
		T_A = 125°C	-0.2					nA
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 5 mA, f = 1 kHz	6	4.5	9	4.5	9	mS
Common-Source Output Conductance	g_{os}		20		200		200	µS
Common-Source Input Capacitance	C_{iss}	V_{DG} = 10 V, I_D = 5 mA, f = 1 MHz	3.5					pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1					pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 5 mA, f = 10 kHz	4					$nV/\sqrt{Hz}$
MATCHING								
Differential Gate-Source Voltage	$\lvert V_{GS1}-V_{GS2} \rvert$	V_{DG} = 10 V, I_D = 5 mA	7		10		20	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta \lvert V_{GS1}-V_{GS2} \rvert}{\Delta T}$	V_{DG} = 10 V, I_D = 5 mA, T = -55 to 25°C	10					µV/°C
		V_{DG} = 10 V, I_D = 5 mA, T = 25 to 125°C	10					µV/°C
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 10 V, V_{GS} = 0 V	0.98					
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V_{DG} = 10 V, I_D = 5 mA, f = 1 kHz	0.98					
Common Mode Rejection Ratio	CMRR	V_{DD} = 5 to 10 V, I_D = 5 mA	90					dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

Siliconix incorporated

M5911 SERIES

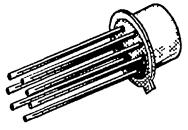
N-Channel JFET Pairs

The M5911 Series are monolithic pairs of JFETs mounted in a single TO-78 package. The M5911 features high speed amplification (slew rate), high gain (typically > 6 mS), and low gate leakage (typically < 1 pA). This performance makes these devices perfect for use as wideband differential amplifiers in demanding test and measurement applications. Finally, its TO-78 hermetically sealed package is available with military screening per MIL-S-19500. (See Section 1.)

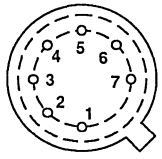
For additional design information please see performance curves NNZ, which are located in Section 7.

PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G MAX (pA)	$\lvert V_{GS_1} - V_{GS_2} \rvert$ MAX (mV)
M5911	-25	5	-100	10
M5912	-25	5	-100	15

TO-78



BOTTOM VIEW



1 SOURCE 1
2 DRAIN 1
3 GATE 1
4 CASE
5 SOURCE 2
6 DRAIN 2
7 GATE 2

SIMILAR PRODUCTS

- SO-8, See SST5912
- Two-Chip, See 2N5911 Series
- Low Noise, See U401 Series
- Low Leakage, See U421 Series
- Chips, Order M591XCHP

4

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMIT	UNITS
Gate-Drain Voltage		V_{GD}	-25	V
Gate-Source Voltage		V_{GS}	-25	
Forward Gate Current		I_G	50	mA
Power Dissipation	Per Side	P_D	367	mW
	Total		500	
Power Derating	Per Side		3	mW/°C
	Total		4	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature		T_{stg}	-65 to 200	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

Siliconix incorporated

ELECTRICAL CHARACTERISTICS[1]			LIMITS					
				M5911		M5912		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-35	-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA	-3.5	-1	-5	-1	-5	V
Saturation Drain Current	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	15	7	40	7	40	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-1		-100		-100	pA
		T_A = 150°C	-2		-250		-250	nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 5 mA	-1		-100		-100	pA
		T_A = 125°C	-0.3		-100		-100	nA
Gate-Source Voltage	V_{GS}	V_{DG} = 10 V, I_D = 5 mA	-1.5	-0.3	-4	-0.3	-4	V
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 5 mA, f = 1 kHz	6	5	10	5	10	mS
Common-Source Output Conductance	g_{os}		20		100		100	µS
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 5 mA, f = 100 MHz	6	5	10	5	10	mS
Common-Source Output Conductance	g_{os}		30		150		150	µS
Common-Source Input Capacitance	C_{iss}	V_{DG} = 10 V, I_D = 5 mA, f = 1 MHz	3.5		5		5	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1		1.2		1.2	pF
Equivalent Input Noise Voltage	$\overline{e}_n$	V_{DG} = 10 V, I_D = 5 mA, f = 10 kHz	4		20		20	$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DG} = 10 V, I_D = 5 mA, f = 10 kHz, R_G = 100 kΩ	0.1		1		1	dB
MATCHING								
Differential Gate-Source Voltage	$\lvert V_{GS1}-V_{GS2} \rvert$	V_{DG} = 10 V, I_D = 5 mA	7		10		15	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta \lvert V_{GS1}-V_{GS2} \rvert}{\Delta T}$	V_{DG} = 10 V, I_D = 5 mA, T = -55 to 25°C	10		20		40	µV/°C
		T = 25 to 125°C	10		20		40	
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 10 V, V_{GS} = 0 V	0.98	0.95	1	0.95	1	
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V_{DG} = 10 V, I_D = 5 mA, f = 1 kHz	0.98	0.95	1	0.95	1	
Differential Gate Current	$\lvert I_{G1}-I_{G2} \rvert$	V_{DG} = 10 V, I_D = 5 mA, T_A = 125°C	0.005		20		20	nA
Common Mode Rejection Ratio	CMRR	V_{DD} = 5 to 10 V, I_D = 5 mA	90					dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

Siliconix incorporated

P1086 SERIES

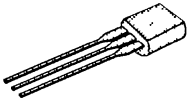
P-Channel JFETs

The P1086 Series of low-cost p-channel analog switches is designed to provide low on-resistance and fast switching. It also works well in conjunction with Siliconix' J111 Series for complementary switching applications. The P1086 Series features a TO-92 package which is available with various lead-forms and/or tape and reel options. (See Section 8.)

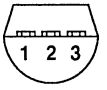
For further design information please consult the typical performance curves PSCIA which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	$I_{D(OFF)}$ TYP (pA)	t_{ON} TYP (ns)
P1086	10	75	–10	25
P1087	5	150	–10	25

TO-92



BOTTOM VIEW



1 SOURCE
2 DRAIN
3 GATE

SIMILAR PRODUCTS

- TO-18, See 2N5114 Series
- SOT-23, See SST174 Series
- Chips, Order P108XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	30	V
Gate-Source Voltage	V_{GS}	30	
Gate Current	I_G	–50	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature	T_J	–55 to 135	°C
Storage Temperature	T_{stg}	–55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

4

Siliconix incorporated

ELECTRICAL CHARACTERISTICS [1]			LIMITS					
				P1086		P1087		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA, V_{DS} = 0 V	45	30		30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = -15 V, I_D = -1 µA			10		5	V
Saturation Drain Current [3]	I_{DSS}	V_{DS} = -20 V, V_{GS} = 0 V		-10		-5		mA
Gate Reverse Current	I_{GSS}	V_{GS} = 15 V, V_{DS} = 0 V	0.01		2		2	nA
		V_{GS} = 15 V, V_{DS} = 0 V, T_A = 85°C	0.6					
Gate Operating Current	I_G	V_{DG} = -15 V, I_D = -1 mA	0.01					nA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = -15 V, V_{GS} = 10 V	-0.01		-10		-10	nA
		V_{DS} = -15 V, V_{GS} = 10 V, T_A = 85°C	-0.001		-0.5		-0.5	µA
Drain-Source On-Resistance	$r_{DS(ON)}$	I_G = -1 mA, V_{GS} = 0 V			75		150	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = -1 mA, V_{DS} = 0 V	-0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = -15 V, I_D = -1 mA, f = 1 kHz	4.5					mS
Common-Source Output Conductance	g_{os}		20					µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 mA, f = 1 kHz			75		150	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = -15 V, V_{GS} = 0 V, f = 1 MHz	20		45		45	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} = 10 V, f = 1 MHz	5		10		10	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = -10 V, I_D = -1 mA, f = 1 kHz	20					$nV/\sqrt{Hz}$
SWITCHING								
Turn-on Time	$t_{d(ON)}$	$V_{GS(ON)}$ = 0 V	10		15		15	ns
	t_r	P/N: P1086 — V_{DD} = -6 V, $V_{GS(OFF)}$ = 12 V, R_L = 910 Ω; P1087 — V_{DD} = -6 V, $V_{GS(OFF)}$ = 7 V, R_L = 1800 Ω	15		20		75	ns
Turn-off Time	$t_{d(OFF)}$		10		15		25	ns
	t_f		20		50		100	ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

PAD1 SERIES

Low-Leakage Pico-Amp Diodes

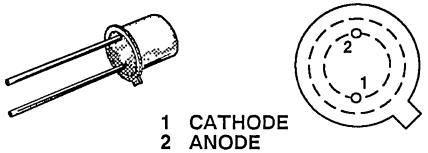
The PAD1 Series of extremely low-leakage diodes provides a superior alternative to conventional diode technology when reverse current (leakage) must be minimized. These devices feature leakage currents ranging from −1 pA (PAD1) to −100 pA (PAD100) to support a wide range of applications. The PAD1 Series is well suited for use in applications such as input protection for operational amplifiers. Its hermetically sealed metal can is available with full military processing per MIL-S-19500. (See Section 1.)

PART NO.	I_R (pA)
PAD1	−1
PAD2	−2
PAD5	−5
PAD10	−10
PAD20	−20
PAD50	−50
PAD100	−100

SIMILAR PRODUCTS

- TO-92, See JPAD5 Series
- SOT-23, See SSTPAD5 Series
- Duals, See DPAD1 Series
- Chips, Order PADXXCHP

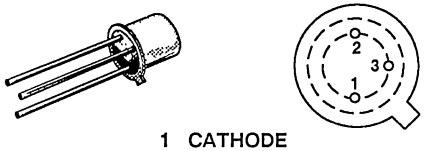
TO-18 (MODIFIED) **BOTTOM VIEW**



1 CATHODE
2 ANODE

(PAD10, 20, 50 100)

TO-18 **BOTTOM VIEW**



1 CATHODE
2 ANODE
3 CASE

(PAD1, 2, 5)

4

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Forward Current	I_F	50	mA
Total Device Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	−55 to 125	°C
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS [1]							
PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS TYP [2]	MIN	MAX	UNIT
STATIC							
Reverse Current	I_R	V_R = -20 V	PAD1	-0.3		-1	pA
			PAD2	-0.7		-2	
			PAD5	-1		-5	
			PAD10	-2		-10	
			PAD20	-2		-20	
			PAD50	-5		-50	
			PAD100	-5		-100	
Reverse Breakdown Voltage	BV_R	I_R = -1 µA	PAD1, 2, 5	-60	-45	-120	V
			PAD10, 20 PAD50, 100	-50	-35		
Forward Voltage Drop	V_F	I_F = 5 mA		0.8		1.5	
DYNAMIC							
Reverse Capacitance	C_R	V_R = -5 V f = 1 MHz	PAD1, 2, 5	0.5		0.8	pF
			PAD10, 20 PAD50, 100	1.5		2	

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.

Siliconix incorporated

PN4091 SERIES

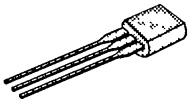
N-Channel JFET

The PN4091 Series is the plastic equivalent of our popular 2N4091 Series. These devices are especially well suited for analog switching applications but function efficiently as high-gain amplifiers, particularly at high-frequency. Our low-cost TO-92 packaging offers affordable performance with flexibility for designers, as these devices can be ordered with a variety of lead forms or tape and reel for automated insertion. (See Section 8.)

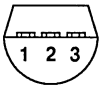
For additional design information please consult the typical performance curves NCB which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	$I_{D(OFF)}$ MAX (pA)	t_{ON} MAX (ns)
PN4091	–10	30	200	25
PN4092	–7	50	200	35
PN4093	–5	80	200	60

TO-92



BOTTOM VIEW



1 DRAIN
2 SOURCE
3 GATE

SIMILAR PRODUCTS

- SOT-23, See SST4091 Series
- TO-18, See 2N4091 Series
- Duals, See 2N5564 Series
- Chips, Order PN409XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	–40	V
Gate-Source Voltage	V_{GS}	–40	
Gate Current	I_G	10	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature	T_J	–55 to 135	°C
Storage Temperature	T_{stg}	–55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

4

Siliconix incorporated

ELECTRICAL CHARACTERISTICS [1]				LIMITS							
					PN4091		PN4092		PN4093		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC											
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V		-55	-40		-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 20 V, I_D = 1 nA			-5	-10	-2	-7	-1	-5	
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V			30		15		8		mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V		-5		200		200		200	pA
			T_A = 125°C	-3		100		100		100	nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 10 mA		-5							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 20 V	V_{GS} = -6 V	5						200	
			V_{GS} = -8 V	5				200			
			V_{GS} = -12 V	5		200					
		V_{DS} = 20 V, T_A = 125°C	V_{GS} = -6 V	3						100	nA
			V_{GS} = -8 V	3				100			
			V_{GS} = -12 V	3		100					
Drain-Source On-Voltage	$V_{DS(ON)}$	V_{GS} = 0 V	I_D = 2.5 mA	0.15						0.2	V
			I_D = 4 mA	0.15				0.2			
			I_D = 6.6 mA	0.15		0.2					
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA				30		50		80	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V		0.7							V
DYNAMIC											
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 20 V, I_D = 1 mA, f = 1 kHz		6							mS
Common-Source Output Conductance	g_{os}			25							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 mA, f = 1 kHz				30		50		80	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz		13		16		16		16	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} = -20 V, f = 1 MHz		3.5		5		5		5	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 1 mA, f = 1 kHz		4							$nV/\sqrt{Hz}$
SWITCHING											
Turn-on Time	$t_{d(ON)}$	V_{DD} = 3 V, $V_{GS(ON)}$ = 0 V		2		15		15		20	ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L		2		10		20		40	
Turn-off Time	t_{OFF}	PN4091 6.6 mA -12 V 425 Ω PN4092 4 mA -8 V 700 Ω PN4093 2.5 mA -6 V 1120 Ω		20		40		60		80	

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

Siliconix incorporated

PN4117 SERIES

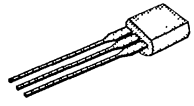
N-Channel JFETs

The PN4117 and PN4117A Series are n-channel JFETs designed to provide ultra-high input impedance. The PN4117 Series features I_{GSS} of 10 pA maximum. The PN4117A is specified with a 1 pA limit and typically operates at 0.2 pA. These devices, therefore, make perfect choices for use as sensitive front-end amplifiers in applications such as microphones, smoke detectors, and precision test equipment. Additionally, its TO-92 plastic package provides a low-cost device compatible with today's automated assembly techniques. (See Section 8.)

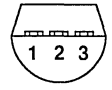
For additional design information please consult performance curves NT which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (μS)	I_{DSS} MAX (mA)
PN4117	-1.8	-40	70	0.09
PN4118	-3	-40	80	0.24
PN4119	-6	-40	100	0.60
PN4117A	-1.8	-40	70	0.09
PN4118A	-3	-40	80	0.24
PN4119A	-6	-40	100	0.60

TO-92



BOTTOM VIEW



1 DRAIN
2 SOURCE
3 GATE

SIMILAR PRODUCTS

- TO-72, See 2N4117 Series
- SOT-23, See SST4117 Series
- Dual, See U421 Series
- Chips, Order PN411XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-40	V
Gate-Source Voltage	V_{GS}	-40	
Gate Current	I_G	10	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature	T_J	-55 to 135	°C
Storage Temperature	T_{stg}	-65 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

4

Siliconix incorporated

ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				PN4117		PN4118		PN4119		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-70	-40		-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA		-0.6	-1.8	-1	-3	-2	-6	V
Saturation Drain Current [3]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V		0.03	0.09	0.08	0.24	0.2	0.6	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -10 V, V_{DS} = 0 V	-0.2		-10		-10		-10	pA
		T_A = 100°C	-0.03		-25		-25		-25	nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 30 µA	-0.2							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 10 V, V_{GS} = -8 V	0.2							pA
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz		70	210	80	250	100	330	µS
Common-Source Output Conductance	g_{os}				3		5		10	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	1.3		3		3		3	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		0.4		1.5		1.5		1.5	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	15							$nV/\sqrt{Hz}$

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

PN4117 SERIES

ELECTRICAL CHARACTERISTICS[1]			LIMITS							
				PN4117A		PN4118A		PN4119A		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-70	-40		-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA		-0.6	-1.8	-1	-3	-2	-6	
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V		0.03	0.09	0.08	0.24	0.2	0.6	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -10 V, V_{DS} = 0 V	-0.2		-1		-1		-1	pA
		T_A = 100°C	-0.03		-2.5		-2.5		-2.5	nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 30 µA	-0.2							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 10 V, V_{GS} = -8 V	0.2							
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz		70	210	80	250	100	330	µS
Common-Source Output Conductance	g_{os}				3		5		10	
Common-Source Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	1.3		3		3		3	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		0.4		1.5		1.5		1.5	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	15							$nV/\sqrt{Hz}$

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

4

PN4302 SERIES

Siliconix incorporated

N-Channel JFETs

The PN4302 Series of multi-purpose JFETs is designed for a wide range of low cost applications. It features low gate leakage and capacitance, which makes these devices ideal for high-frequency amplifiers. This series is packaged in TO-92 for low cost and compatibility with automated assembly.

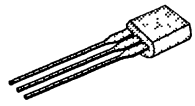
For further design information please consult the typical performance curves NPA which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
PN4302	-4	-30	1	5
PN4303	-6	-30	2	10
PN4304	-10	-30	1	15

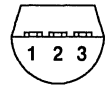
SIMILAR PRODUCTS

- TO-18, See 2N4338 Series
- SOT-23, See SST201 Series
- Chips, Order PN430XCHP

TO-92



BOTTOM VIEW



1 DRAIN
2 SOURCE
3 GATE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-30	V
Gate-Source Voltage	V_{GS}	-30	
Gate Current	I_G	50	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature	T_J	-55 to 135	°C
Storage Temperature	T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS[1]			LIMITS							
				PN4302		PN4303		PN4304		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-57	-30		-30		-30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 20 V, I_D = 10 nA			-4		-6		-10	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V		0.5	5	4	10	0.5	15	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -10 V, V_{DS} = 0 V	-0.001		-1		-1		-1	nA
		T_A = 85°C	-0.03		-100		-100		-100	
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 kHz		1		2		1		mS
Common-Source Output Conductance	g_{os}				50		50		50	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	4.5		6		6		6	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.3		3		3		3	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	6							$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz, R_G = 1 MΩ	<0.1		2		2		3	dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

4

PN4391 SERIES

Siliconix incorporated

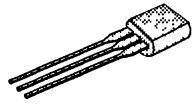
N-Channel JFET

The PN4391 Series is the plastic equivalent of our popular 2N4391 Series. These devices are especially well suited for analog switching applications but function efficiently as high-gain amplifiers, particularly at high-frequency. Our low-cost TO-92 packaging offers affordable performance with flexibility for designers, as these devices can be ordered with a variety of lead forms or tape and reel for automated insertion. (See Section 8.)

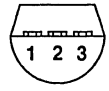
For additional design information please consult the typical performance curves NCB which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	$I_{D(OFF)}$ MAX (nA)	t_{ON} MAX (ns)
PN4391	–10	30	1	20
PN4392	–5	60	1	20
PN4393	–3	100	1	20

TO-92



BOTTOM VIEW



1 DRAIN
2 SOURCE
3 GATE

SIMILAR PRODUCTS

- SOT-23, See SST4391 Series
- TO-18, See 2N4391 Series
- Duals, See 2N5564 Series
- Chips, Order PN439XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	–40	V
Gate-Source Voltage	V_{GS}	–40	
Gate Current	I_G	50	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature	T_J	–55 to 135	°C
Storage Temperature	T_{stg}	–55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS [1]

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS TYP[2]	PN4391 MIN	PN4391 MAX	PN4392 MIN	PN4392 MAX	PN4393 MIN	PN4393 MAX	UNIT
STATIC											
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V		-55	-40		-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 20 V, I_D = 1 nA			-4	-10	-2	-5	-0.5	-3	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V			50	150	25	100	5	60	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V		-0.005		-1		-1		-1	nA
			T_A=100°C	-1.0		-200		-200		-200	
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 10 mA		-5							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 20 V	V_{GS} = -5 V	0.005						1	nA
			V_{GS} = -7 V	0.005				1			
			V_{GS} = -12 V	0.005		1					
		V_{DS} = 20 V, T_A=100°C	V_{GS} = -5 V	1						200	
			V_{GS} = -7 V	1				200			
			V_{GS} = -12 V	1		200					
Drain-Source On-Voltage	$V_{DS(ON)}$	V_{GS} = 0 V	I_D = 3 mA	0.25						0.4	V
			I_D = 6 mA	0.30				0.4			
			I_D = 12 mA	0.35		0.4					
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA				30		60		100	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V		0.7							V
DYNAMIC											
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 20 V, I_D = 1 mA, f = 1 kHz		6							mS
Common-Source Output Conductance	g_{os}			25							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0, f = 1 kHz				30		60		100	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz		12		16		16		16	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, f = 1 MHz	V_{GS} = -5 V	3.5						5	
			V_{GS} = -7 V	3.5				5			
			V_{GS} = -12 V	3.5		5					
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 10 mA, f = 1 kHz		3.0							nV/√Hz
SWITCHING											
Turn-on Time	$t_{d(ON)}$	V_{DD} = 10 V, $V_{GS(ON)}$ = 0 V		2		15		15		15	ns
	t_r	P/N — $I_{D(ON)}$ — $V_{GS(OFF)}$ — R_L		2		5		5		5	
Turn-off Time	$t_{d(OFF)}$	PN4391 — 12 mA — -12 V — 800 Ω		6		20		35		50	
	t_f	PN4392 — 6 mA — -7 V — 1600 Ω PN4393 — 3 mA — -5 V — 3200 Ω		13		15		20		30	

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

4

PN4416

Siliconix incorporated

N-Channel JFET

The PN4416 is a n-channel JFET designed to provide high-performance amplification, especially at high-frequency. These parts feature low noise (4 dB max @ 400 MHz), high gain (10 dB min @ 400 MHz) and provide a wide bandwidth. Its low cost TO-92 package is available with a wide range of lead form and tape and reel opitons. (See Section 8.)

For additional design information please see performance curves NH, which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
PN4416	-6	-30	4.5	15

TO-92 BOTTOM VIEW

1 SOURCE
2 DRAIN
3 GATE

SIMILAR PRODUCTS

- TO-72, See 2N4416
- SOT-23, See SST4416
- Chips, Order PN4416CHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-30	V
Gate-Source Voltage	V_{GS}	-30	
Gate Current	I_G	10	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature	T_J	-55 to 135	°C
Storage Temperature	T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS [1]			LIMITS			
				PN4416		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	UNIT
STATIC						
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-36	-30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 1 nA	-3		-6	V
Saturation Drain Current [3]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V	10	5	15	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-0.002		-1	nA
		T_A = 125°C	-0.6			
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 1 mA	-20			pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 10 V, V_{GS} = -6 V	5			pA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA	150			Ω
Gate-Source Forward Voltage	$V_{GS(f)}$	I_G = 1 mA, V_{DS} = 0 V	0.7			V
DYNAMIC						
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 kHz	6	4.5	7.5	mS
Common-Source Output Conductance	g_{os}		15		50	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	2.2		4	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		0.7		0.8	pF
Common-Source Output Capacitance	C_{oss}		1		2	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 100 Hz	9			$nV/\sqrt{Hz}$

ELECTRICAL CHARACTERISTICS [1]			LIMITS					
				100 MHz		400 MHz		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	MIN	MAX	UNIT
HIGH-FREQUENCY								
Common-Source Input Conductance	g_{iss}	V_{DS} = 15 V, V_{GS} = 0 V			100		1000	µS
Common-Source Input Susceptance	b_{iss}				2500		10000	µS
Common-Source Output Conductance	g_{oss}				75		100	µS
Common-Source Output Susceptance	b_{oss}				1000		4000	µS
Common-Source Forward Transconductance	g_{fs}					4000		µS
Common-Source Power Gain	G_{ps}	V_{DS} = 15 V, I_D = 5 mA		18		10		dB
Noise Figure	NF	V_{DS} = 15 V, I_D = 5 mA, R_G = 1 kΩ			2		4	dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

4

SST108 SERIES

Siliconix incorporated

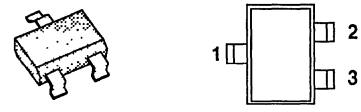
N-Channel JFET

The SST108 Series is the surface mount equivalent of our J108 device types. It features the lowest $r_{DS(ON)}$ of any SOT-23 JFET device, which makes it especially well suited for analog switching applications. Siliconix' surface mount commitment features low cost performance for a wide range of commercial applications as well as tape and reel options for automatic insertion and high-volume assembly. (See Section 8.)

For further design information please consult the typical performance curves NIP which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	$I_{D(OFF)}$ TYP (pA)	t_{ON} TYP (ns)
SST108	-10	8	20	4
SST109	-6	12	20	4
SST110	-4	18	20	4

SOT-23 TOP VIEW



1 GATE
2 DRAIN
3 SOURCE

SIMILAR PRODUCTS

- TO-92, See J108 Series
- TO-52, See 2N5432 Series
- Chips, Order J1XXCHP

PRODUCT MARKING	
SST108	I08
SST109	I09
SST110	I10

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	
Gate Current	I_G	50	mA
Power Dissipation	P_D	350	mW
Power Derating		2.8	mW/°C
Operating Junction Temperature	T_J	-55 to 150	°C
Storage Temperature	T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				SST108		SST109		SST110		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-32	-25		-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 5 V, I_D = 1 µA		-3	-10	-2	-6	-0.5	-4	V
Saturation Drain Current [3]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		80		40		10		mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-0.01		-3		-3		-3	nA
		V_{GS} = -15 V, V_{DS} = 0 V, T_A = 125°C	-5							
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 10 mA	-0.01							nA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 5 V, V_{GS} = -10 V	0.02		3		3		3	nA
		V_{DS} = 5 V, V_{GS} = -10 V, T_A = 125°C	1.0							nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, V_{DS} ≤ 0.1 V			8		12		18	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 5 V, I_D = 10 mA, f = 1 kHz	17							mS
Common-Source Output Conductance	g_{os}	V_{DG} = 5 V, I_D = 10 mA, f = 1 kHz	600							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V, f = 1 kHz			8		12		18	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = 0 V, f = 1 MHz	60		85		85		85	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} = -10 V, f = 1 MHz	11		15		15		15	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 5 V, I_D = 10 mA, f = 1 kHz	3.5							$nV/\sqrt{Hz}$
SWITCHING										
Turn-on Time	$t_{d(ON)}$	V_{DD} = 1.5 V, $V_{GS(ON)}$ = 0 V	3							ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	1							ns
Turn-off Time	$t_{d(OFF)}$	SST108 10 mA -12 V 150 Ω	4							ns
	t_f	SST109 10 mA -7 V 150 Ω SST110 10 mA -5 V 150 Ω	18							ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

4

SST111 SERIES

Siliconix incorporated

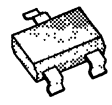
N-Channel JFET

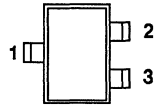
The SST111 Series is the surface mount equivalent of our J111 device types. Its low cost and $r_{DS(on)}$ make it a good choice for an all-purpose analog switch, while its high g_{fs} and good high-frequency response also make this product useful in a high-gain amplifier mode. Like all SOT-23 products available from Siliconix, tape and reel capabilities exist for automated assembly. (See Section 8.)

For further design information please consult the typical performance curves NCB which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	$I_{D(OFF)}$ TYP (pA)	t_{ON} TYP (ns)
SST111	–10	30	5	4
SST112	–5	50	5	4
SST113	–3	100	5	4

SOT-23 **TOP VIEW**





1 GATE
2 DRAIN
3 SOURCE

PRODUCT MARKING	
SST111	C11
SST112	C12
SST113	C13

SIMILAR PRODUCTS

- TO-92, See J111 Series
- TO-18, See 2N4391 Series
- Duals, See 2N5564 Series
- Chips, Order J11XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	–35	V
Gate-Source Voltage	V_{GS}	–35	
Gate Current	I_G	50	mA
Power Dissipation	P_D	350	mW
Power Derating		2.8	mW/°C
Operating Junction Temperature	T_J	–55 to 150	°C
Storage Temperature	T_{stg}	–55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				SST111		SST112		SST113		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-55	-35		-35		-35		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 5 V, I_D = 1 µA		-3	-10	-1	-5		-3	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		20		5		2		mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-0.005		-1		-1		-1	nA
		T_A = 125°C	-3							
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 10 mA	-5							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 10 V, V_{GS} = -12 V	0.005		1		1		1	nA
		V_{DS} = 10 V, V_{GS} = -12 V, T_A = 125°C	3							
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, V_{DS} = 0.1 V			30		50		100	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 20 V, I_D = 1 mA, f = 1 kHz	6							mS
Common-Source Output Conductance	g_{os}		25							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V, f = 1 kHz			30		50		100	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = -10 V, f = 1 MHz	7		12		12		12	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		3		5		5		5	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 1 mA, f = 1 kHz	4							$nV/\sqrt{Hz}$
SWITCHING										
Turn-on Time	$t_{d(ON)}$	V_{DD} = 10 V, $V_{GS(ON)}$ = 0 V	2							ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	2							
Turn-off Time	$t_{d(OFF)}$	SST111 12.5 mA -12 V 800 Ω	6							
	t_f	SST112 6.25 mA -7 V 1600 Ω SST113 3.1 mA -5 V 3200 Ω	15							

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

4

SST174 SERIES

Siliconix incorporated

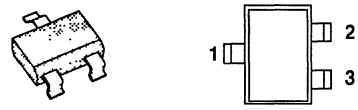
P-Channel JFET

The SST174 Series is a low-cost p-channel analog switch designed to provide low on-resistance and fast switching. It works well in conjunction with Siliconix' J111 Series for complimentary switching applications. It features a SOT-23 package and is available tape and reeled to support automated assembly. (See Section 8.)

For further design information please consult the typical performance curves PSCIA which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	I_{GSS} MAX (nA)	t_{ON} TYP (ns)
SST174	10	85	1	25
SST175	6	125	1	25
SST176	4	250	1	25
SST177	2.25	300	1	25

SOT-23 TOP VIEW



1 GATE
2 DRAIN
3 SOURCE

PRODUCT MARKING	
SST174	S74
SST175	S75
SST176	S76
SST177	S77

SIMILAR PRODUCTS

- TO-18, See 2N5114 Series
- TO-92, See J174 Series
- Chips, Order J17XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	30	V
Gate-Source Voltage	V_{GS}	30	
Gate Current	I_G	–50	mA
Power Dissipation	P_D	350	mW
Power Derating		2.8	mW/°C
Operating Junction Temperature	T_J	–55 to 150	°C
Storage Temperature	T_{stg}	–55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS [1]			LIMITS					
				SST174		SST175		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA, V_{DS} = 0 V	45	30		30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = -15 V, I_D = -10 nA		5	10	3	6	V
Saturation Drain Current [3]	I_{DSS}	V_{DS} = -15 V, V_{GS} = 0 V		-20	-135	-7	-70	mA
Gate Reverse Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	0.01		1		1	nA
		V_{GS} = 20 V, V_{DS} = 0 V, T_A = 125°C	5					nA
Gate Operating Current	I_G	V_{DG} = -15 V, I_D = -1 mA	10					pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = -15 V, V_{GS} = 10 V	-10					pA
		V_{DS} = -15 V, V_{GS} = 10 V, T_A = 125°C	-5					nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, V_{DS} = -0.1 V			85		125	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = -1 mA, V_{DS} = 0 V	-0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = -15 V, I_D = -1 mA, f = 1 kHz	4.5					mS
Common-Source Output Conductance	g_{os}		20					µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 mA, f = 1 kHz			85		125	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = 0 V, f = 1 MHz	20					pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} = 10 V, f = 1 MHz	5					pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = -10 V, I_D = -1 mA, f = 1 kHz	20					$nV/\sqrt{Hz}$
SWITCHING								
Turn-on Time	$t_{d(ON)}$	$V_{GS(ON)}$ = 0 V	10					ns
	t_r	P/N: SST174 V_{DD} = -10 V, $V_{GS(OFF)}$ = 12 V, R_L = 560 Ω; SST175 V_{DD} = -6 V, $V_{GS(OFF)}$ = 8 V, R_L = 1200 Ω	15					ns
Turn-off Time	$t_{d(OFF)}$		10					ns
	t_f		20					ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

4

Siliconix incorporated

ELECTRICAL CHARACTERISTICS [1]			LIMITS					
				SST176		SST177		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA, V_{DS} = 0 V	45	30		30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = −15 V, I_D = −10 nA		1	4	0.8	2.25	V
Saturation Drain Current [3]	I_{DSS}	V_{DS} = −15 V, V_{GS} = 0 V		−2	−35	−1.5	−20	mA
Gate Reverse Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	0.01		1		1	nA
		T_A = 125°C	5					
Gate Operating Current	I_G	V_{DG} = −15 V, I_D = −1 mA	10					pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = −15 V, V_{GS} = 10 V	−10					pA
		V_{DS} = −15 V, V_{GS} = 10 V, T_A = 125°C	−5					nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, V_{DS} = −0.1 V			250		300	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = −1 mA, V_{DS} = 0 V	−0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = −15 V, I_D = −1 mA, f = 1 kHz	4.5					mS
Common-Source Output Conductance	g_{os}		20					µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 mA, f = 1 kHz			250		300	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = 0 V, f = 1 MHz	20					pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} = 10 V, f = 1 MHz	5					pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = −10 V, I_D = −1 mA, f = 1 kHz	20					$nV/\sqrt{Hz}$
SWITCHING								
Turn-on Time	$t_{d(ON)}$	$V_{GS(ON)}$ = 0 V	10					ns
	t_r	P/N: SST176 — V_{DD} = −6 V, $V_{GS(OFF)}$ = 6 V, R_L = 5600 Ω; SST177 — V_{DD} = −6 V, $V_{GS(OFF)}$ = 3 V, R_L = 10000 Ω	15					ns
Turn-off Time	$t_{d(OFF)}$		10					ns
	t_f		20					ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

Siliconix incorporated

SST201 SERIES

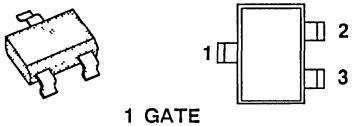
N-Channel JFETs

The SST201 Series is the SOT-23 equivalent of our popular J201 Series. It features low leakage, very low noise, and low cutoff voltage for use with low level power supplies. The SST201 and SST204 are excellent for battery operated equipment and low current amplifiers. The SST201 Series' SOT-23 package affords low cost and compatibility with automated assembly techniques. (See Section 8.)

For further design information please consult the typical performance curves NPA which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
SST201	-1.5	-40	0.5	1
SST202	-4	-40	1	4.5
SST203	-10	-40	1.5	20
SST204	-2	-25	0.5	3

SOT-23 TOP VIEW



1 GATE
2 SOURCE
3 DRAIN

SIMILAR PRODUCTS

- TO-18, See 2N4338 Series
- TO-92, See J201 Series
- Chips, Order J20XCHP

PRODUCT MARKING	
SST201	P01
SST202	P02
SST203	P03
SST204	P04

4

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-40	V
Gate-Source Voltage	V_{GS}	-40	
Gate Current	I_G	50	mA
Power Dissipation	P_D	350	mW
Power Derating		2.8	mW/°C
Operating Junction Temperature	T_J	-55 to 150	°C
Storage Temperature	T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS [1]			LIMITS					
				SST201		SST202		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-57	-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 20 V, I_D = 10 nA		-0.3	-1.5	-0.8	-4	V
Saturation Drain Current [3]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V		0.2	1.0	0.9	4.5	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-2		-100		-100	pA
		T_A = 125°C	-1					nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 0.1 mA	-2					pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 15 V, V_{GS} = -10 V	2					pA
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 kHz		0.5		1		mS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	4.5					pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.3					pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	6					$nV/\sqrt{Hz}$

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

ELECTRICAL CHARACTERISTICS [1]			LIMITS					
				SST203		SST204		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-57	-40		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 20 V, I_D = 10 nA		-2	-10	-0.3	-2	
Saturation Drain Current [3]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V		4	20	0.2	3	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-2		-100		-100	pA
		V_{GS} = -20 V, V_{DS} = 0 V, T_A = 125°C	-1					nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 0.1 mA	-2					pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 15 V, V_{GS} = -10 V	2					
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 kHz		1.5		0.5		mS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	4.5					pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.3					
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	6					$nV/\sqrt{Hz}$

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

4

SST270 SERIES

Siliconix incorporated

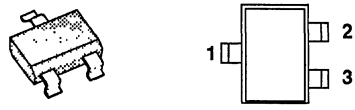
P-Channel JFET

The SST270 Series is an all-purpose amplifier for designs requiring p-channel operation. These devices feature high gain, low noise and tight $V_{GS(OFF)}$ limits for simple circuit design. They are available in low-cost SOT-23 packages and are fully compatible with automatic insertion techniques. (See Section 8 for details.)

For further design information please consult the typical performance curves PSCIA which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
SST270	2.0	30	6	-15
SST271	4.5	30	8	-50

SOT-23 TOP VIEW



1 GATE
2 DRAIN
3 SOURCE

SIMILAR PRODUCTS

- TO-92, See J270 Series
- Chips, Order J27XCHP

PRODUCT MARKING	
SST270	S70
SST271	S71

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	30	V
Gate-Source Voltage	V_{GS}	30	
Gate Current	I_G	-50	mA
Power Dissipation	P_D	350	mW
Power Derating		2.8	mW/°C
Operating Junction Temperature	T_J	-55 to 150	°C
Storage Temperature	T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS [1]			LIMITS					
				SST270		SST271		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA, V_{DS} = 0 V	45	30		30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = −15 V, I_D = −1 nA		0.5	2.0	1.5	4.5	V
Saturation Drain Current [3]	I_{DSS}	V_{DS} = −15 V, V_{GS} = 0 V		−2	−15	−6	−50	mA
Gate Reverse Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	10		200		200	pA
		T_A = 125°C	5					nA
Gate Operating Current	I_G	V_{DG} = −15 V, I_D = −1 mA	10					pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = −15 V, V_{GS} = 10 V	−10					pA
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = −1 mA, V_{DS} = 0 V	−0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = −15 V, V_{GS} = 0 V, f = 1 kHz		6	15	8	18	mS
Common-Source Output Conductance	g_{os}				200		500	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = −15 V, V_{GS} = 0 V, f = 1 MHz	20					pF
Common-Source Reverse Transfer Capacitance	C_{rss}		4					pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = −10 V, V_{GS} = 0 V, f = 1 kHz	20					$nV/\sqrt{Hz}$

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

4

SST308 SERIES

Siliconix incorporated

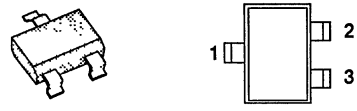
N-Channel JFETs

The SST308 Series is the surface mount equivalent of our popular J308 Series. It features high-gain (> 8000 μS), low noise (typically < 6 nV√Hz) and low gate leakage (typically < 2 pA). Of special interest, however, is performance at high frequency. Even at 450 MHz, the SST308 Series offers high power gain and low noise. Tape and reel options are available to support automated assembly. (See Section 8.)

For additional design information and a closer look at high-frequency characteristics, please consult performance curves NZB which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
SST308	-6.5	-25	8	60
SST309	-4	-25	10	30
SST310	-6.5	-25	8	60

SOT-23 TOP VIEW



1 GATE
2 DRAIN
3 SOURCE

PRODUCT MARKING	
SST308	Z08
SST309	Z09
SST310	Z10

SIMILAR PRODUCTS

- TO-92, See J308 Series
- TO-52, See U308 Series
- Dual, See U430 Series
- Chips, Order J30XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	
Gate Current	I_G	10	mA
Power Dissipation	P_D	350	mW
Power Derating		2.8	mW/°C
Operating Junction Temperature	T_J	-55 to 150	°C
Storage Temperature	T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS[1]				LIMITS							
				SST308		SST309		SST310		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-35	-25		-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA		-1	-6.5	-1	-4	-2	-6.5	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V		12	60	12	30	24	60	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-0.002		-1		-1		-1	nA
		V_{DS} = 0 V, T_A = 125°C	-0.008		-1		-1		-1	µA
Gate Operating Current	I_G	V_{DG} = 9 V, I_D = 10 mA	-15							pA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA	35							Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 10 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 10 mA, f = 1 kHz	14	8		10		8		mS
Common-Source Output Conductance	g_{os}		110		250		250		250	µS
Common-Source Input Capacitance	C_{iss}	V_{GS} = -10 V, V_{DS} = 10 V, f = 1 MHz	4		5		5		5	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.9		2.5		2.5		2.5	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, I_D = 10 mA, f = 100 Hz	6							$nV/\sqrt{Hz}$
HIGH FREQUENCY										
Common-Gate Foward Transconductance	g_{fg}	V_{DS} = 10 V, I_D = 10 mA, f = 105 MHz	15							mS
		f = 450 MHz	13							
Common-Gate Output Conductance	g_{og}	f = 105 MHz	0.16							
		f = 450 MHz	0.55							
Common-Gate Power Gain[4]	G_{pg}	f = 105 MHz	16							dB
		f = 450 MHz	11.5							
Noise Figure	NF	f = 105 MHz	1.5							
		f = 450 MHz	2.7							

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.
4. Gain (G_{pg}) measured at optimum input noise match.

SST404 SERIES

Siliconix incorporated

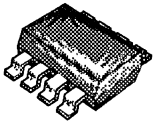
N-Channel JFET Pairs

The SST404 Series is the surface mount equivalent of our U401 Series. It is available in a SO-8 package with three ranges of offset and drift specifications. It features extremely low noise and gate leakage and is intended for use in a wide range of precision instrumentation. For ease of manufacturing, the symmetrical pinout prevents improper orientation. Finally, tape and reel options are available to make this product compatible with automatic assembly methods. (See Section 8.)

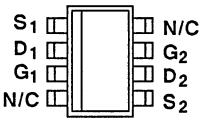
For additional design information please see performance curves NNR, which are located in Section 7.

PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G MAX (pA)	$\lvert V_{GS_1} - V_{GS_2} \rvert$ MAX (mV)
SST404	-50	2	-15	15
SST405	-50	2	-15	20
SST406	-50	2	-15	40

SO-8



TOP VIEW



SIMILAR PRODUCTS

- TO-71, See U401 Series
- Chips, Order U40XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMIT	UNITS
Gate-Drain Voltage		V_{GD}	-50	V
Gate-Source Voltage		V_{GS}	-50	
Forward Gate Current		I_G	10	mA
Power Dissipation	Per Side	P_D	300	mW
	Total		500	
Power Derating	Per Side		2.4	mW/°C
	Total		4	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature		T_{stg}	-55 to 200	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

ELECTRICAL CHARACTERISTICS[1]			LIMITS							
				SST404		SST405		SST406		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-58	-50		-50		-50		V
Gate-Gate Breakdown Voltage	$V_{(BR)G1-G2}$	I_G = ±1 µA, V_{DS} = 0 V, V_{GS} = 0 V	-58	±50		±50		±50		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 1 nA	-1.5	-0.5	-2.5	-0.5	-2.5	-0.5	-2.5	V
Saturation Drain[3] Current	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V	3.5	0.5	10	0.5	10	0.5	10	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -30 V, V_{DS} = 0 V	-2		-25		-25		-25	pA
		T_A = 125°C	-1							nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 200 µA	-2		-15		-15		-15	pA
		T_A = 125°C	-0.8		-10		-10		-10	nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 0.1 mA	250							Ω
Gate-Source Voltage	V_{GS}	V_{DG} = 15 V, I_D = 200 µA	-1		-2.3		-2.3		-2.3	V
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 15 V, I_D = 200 µA, f = 1 kHz	1.5	1	2	1	2	1	2	mS
Common-Source Output Conductance	g_{os}		1.3		2		2		2	µS
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	1.5	2	7	2	7	2	7	mS
Common-Source Output Conductance	g_{os}		10		20		20		20	µS
Common-Source Input Capacitance	C_{iss}	V_{DG} = 15 V, I_D = 200 µA, f = 1 MHz			8		8		8	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.5		3		3		3	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 15 V, I_D = 200 µA, f = 10 Hz	10		20		20		20	$nV/\sqrt{Hz}$
MATCHING										
Differential Gate-Source Voltage	$\lvert V_{GS1}-V_{GS2}\rvert$	V_{DG} = 10 V, I_D = 200 µA			15		20		40	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	V_{DG} = 10 V, I_D = 200 µA, T = -55 to 25°C			25		40		80	µV/°C
		V_{DG} = 10 V, I_D = 200 µA, T = 25 to 125°C			25		40		80	µV/°C
Common Mode Rejection Ratio	CMRR	V_{DG} = 10 to 20 V, I_D = 200 µA	102	95		90				dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

4

SST440 SERIES

Siliconix incorporated

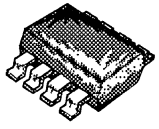
N-Channel JFET Pairs

The SST440 Series are monolithic pairs of JFETs mounted in a single SO-8 package. The SST440 Series features high speed amplification (slew rate), high gain (typically > 6 mS), and low gate leakage (typically < 1 pA). This performance makes these devices perfect for use as wideband differential amplifiers in demanding test and measurement applications. Finally, its SO-8 package is available in tape and reel to support automated assembly. (See Section 8.)

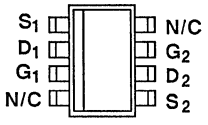
For additional design information please see performance curves NNZ, which are located in Section 7.

PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G MAX (pA)	$\lvert V_{GS_1} - V_{GS_2} \rvert$ MAX (mV)
SST440	-25	4.5	-500	10
SST441	-25	4.5	-500	20

SO-8



TOP VIEW



SIMILAR PRODUCTS

- TO-71, See U440 Series
- TO-78, See U443 Series
- Low Noise, See SST404 Series
- Chips, Order U44XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMIT	UNITS
Gate-Drain Voltage		V_{GD}	-25	V
Gate-Source Voltage		V_{GS}	-25	
Forward Gate Current		I_G	50	mA
Power Dissipation	Per Side	P_D	300	mW
	Total		500	
Power Derating	Per Side		2.4	mW/°C
	Total		4	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature		T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

ELECTRICAL CHARACTERISTICS[1]				LIMITS				
				SST440		SST441		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-35	-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA	-3.5	-1	-6	-1	-6	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	15	6	30	6	30	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-1		-500		-500	pA
		V_{GS} = -15 V, V_{DS} = 0 V, T_A = 125°C	-0.2					nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 5 mA	-1		-500		-500	pA
		V_{DG} = 10 V, I_D = 5 mA, T_A = 125°C	-0.2					nA
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 5 mA, f = 1 kHz	6	4.5	9	4.5	9	mS
Common-Source Output Conductance	g_{os}		20		200		200	µS
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 5 mA, f = 100 MHz	5.5					mS
Common-Source Output Conductance	g_{os}		30					µS
Common-Source Input Capacitance	C_{iss}	V_{DG} = 10 V, I_D = 5 mA, f = 1 MHz	3.5					pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1					pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 5 mA, f = 10 kHz	4					$nV/\sqrt{Hz}$
MATCHING								
Differential Gate-Source Voltage	$\lvert V_{GS1}-V_{GS2}\rvert$	V_{DG} = 10 V, I_D = 5 mA	7		10		20	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	V_{DG} = 10 V, I_D = 5 mA, T = -55 to 25°C	10					µV/°C
		V_{DG} = 10 V, I_D = 5 mA, T = 25 to 125°C	10					µV/°C
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 10 V, V_{GS} = 0 V	0.98					
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V_{DG} = 10 V, I_D = 5 mA, f = 1 kHz	0.98					
Common Mode Rejection Ratio	CMRR	V_{DD} = 5 to 10 V, I_D = 5 mA	90					dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

4

SST4091 SERIES

Siliconix incorporated

N-Channel JFET

The SST4091 Series is the surface mount equivalent of our popular 2N4091 device types. Its low cost and $r_{DS(on)}$ make it a good choice for an all-purpose analog switch, while its high g_{fs} and good high-frequency response also make this product useful in a high-gain amplifier mode. Like all SOT-23 products available from Siliconix, tape and reel capabilities exist for automated assembly. (See Section 8.)

For further design information please consult the typical performance curves NCB which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	$I_{D(OFF)}$ TYP (pA)	t_{ON} TYP (ns)
SST4091	–10	30	5	4
SST4092	–7	50	5	4
SST4093	–5	80	5	4

SOT-23 **TOP VIEW**

1 GATE
2 DRAIN
3 SOURCE

SIMILAR PRODUCTS

- TO-18, See 2N4091 Series
- TO-92, See PN4091 Series
- Duals, See 2N5564 Series
- Chips, Order 2N409XCHP

PRODUCT MARKING	
SST4091	C41
SST4092	C42
SST4093	C43

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	–35	V
Gate-Source Voltage	V_{GS}	–35	
Gate Current	I_G	10	mA
Power Dissipation	P_D	350	mW
Power Derating		2.8	mW/°C
Operating Junction Temperature	T_J	–55 to 150	°C
Storage Temperature	T_{stg}	–55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				SST4091		SST4092		SST4093		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-55	-35		-35		-35		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 20 V, I_D = 10 nA		-5	-10	-2	-7	-1	-5	V
Saturation Drain Current [3]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V		30		15		8		mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-0.005		-1		-1		-1	nA
		V_{GS} = -15 V, V_{DS} = 0 V, T_A = 125°C	-3							nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 10 mA	-5							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 10 V, V_{GS} = -10 V	0.005		1		1		1	nA
		V_{DS} = 10 V, V_{GS} = -10 V, T_A = 125°C	3							nA
Drain-Source On-Voltage	$V_{DS(ON)}$	V_{GS} = 0 V, I_D = 6.6 mA	0.15		0.2					V
		V_{GS} = 0 V, I_D = 4 mA	0.15				0.2			V
		V_{GS} = 0 V, I_D = 2.5 mA	0.15						0.2	V
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA			30		50		80	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 1 mA, f = 1 kHz	6							mS
Common-Source Output Conductance	g_{os}	V_{DG} = 10 V, I_D = 1 mA, f = 1 kHz	25							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V, f = 1 kHz			30		50		80	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	12		16		16		16	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} = -20 V, f = 1 MHz	3.5		5		5		5	pF
Equivalent Input Noise Voltage	$\overline{e}_n$	V_{DG} = 10 V, I_D = 10 mA, f = 1 kHz	3.0							$nV/\sqrt{Hz}$
SWITCHING										
Turn-on Time	$t_{d(ON)}$	V_{DD} = 5 V, $V_{GS(ON)}$ = 0 V	2							ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	2							ns
Turn-off Time	$t_{d(OFF)}$	SST4091 6.6 mA -12 V 425 Ω	6							ns
	t_f	SST4092 4 mA -8 V 700 Ω SST4093 2.5 mA -6 V 1120 Ω	13							ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

4

SST4391 SERIES

Siliconix incorporated

N-Channel JFET

The SST4391 Series is the surface mount equivalent of our popular 2N4391 device types. Its low cost and $r_{DS(on)}$ make it a good choice for an all-purpose analog switch, while its high g_{fs} and good high-frequency response also make this product useful in a high-gain amplifier mode. Like all SOT-23 products available from Siliconix, tape and reel capabilities exist for automated assembly. (See Section 8.)

For further design information please consult the typical performance curves NCB which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	$I_{D(OFF)}$ TYP (pA)	t_{ON} TYP (ns)
SST4391	–10	30	5	4
SST4392	–5	60	5	4
SST4393	–3	100	5	4

SOT-23 TOP VIEW

1 GATE
2 DRAIN
3 SOURCE

SIMILAR PRODUCTS

- TO-18, See 2N4391 Series
- TO-92, See PN4391 Series
- Duals, See 2N5564 Series
- Chips, Order 2N439XCHP

PRODUCT MARKING	
SST4391	C91
SST4392	C92
SST4393	C93

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	–35	V
Gate-Source Voltage	V_{GS}	–35	
Gate Current	I_G	50	mA
Power Dissipation	P_D	350	mW
Power Derating		2.8	mW/°C
Operating Junction Temperature	T_J	–55 to 150	°C
Storage Temperature	T_{stg}	–55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				SST4391		SST4392		SST4393		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-55	-35		-35		-35		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 10 nA		-4	-10	-2	-5	-0.5	-3	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V		50		25		5		mA
Gate Reverse Current	I_{GSS}	V_{GS} = -5 V, V_{DS} = 0 V	-5		-100		-100		-100	pA
		V_{DS} = 0 V, T_A = 125°C	-3		-200		-200		-200	nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 10 mA	-5							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 10 V, V_{GS} = -10 V	5		100		100		100	pA
		V_{DS} = 10 V, V_{GS} = -10 V, T_A = 125°C	3		200		200		200	nA
Drain-Source On-Voltage	$V_{DS(ON)}$	V_{GS} = 0 V, I_D = 12 mA	0.3		0.4					V
		V_{GS} = 0 V, I_D = 6 mA	0.3				0.4			V
		V_{GS} = 0 V, I_D = 3 mA	0.25						0.4	V
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA			30		60		100	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 1 mA, f = 1 kHz	6							mS
Common-Source Output Conductance	g_{os}		25							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 mA, f = 1 kHz			30		60		100	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	13		16		16		16	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, f = 1 MHz, V_{GS} = -12 V	3.5		5					pF
		V_{DS} = 0 V, f = 1 MHz, V_{GS} = -7 V	3.8				5			pF
		V_{DS} = 0 V, f = 1 MHz, V_{GS} = -5 V	4						5	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 10 mA, f = 1 kHz	3.0							nV/√Hz
SWITCHING										
Turn-on Time	$t_{d(ON)}$	V_{DD} = 10 V, $V_{GS(ON)}$ = 0 V	2							ns
	t_r	P/N: SST4391 12 mA -12 V 800 Ω; SST4392 6 mA -7 V 1600 Ω; SST4393 3 mA -5 V 3200 Ω	2							ns
Turn-off Time	$t_{d(OFF)}$		6							ns
	t_f		13							ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

4

SST4416

Siliconix incorporated

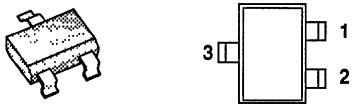
N-Channel JFET

The SST4416 is the SOT-23 equivalent of our popular PN4416 Series, designed to provide high-performance amplification, especially at high-frequency. These parts feature low noise, high gain, and provide a wide bandwidth. To support the needs of automated assembly techniques these low cost devices are available with tape and reel options. (See Section 8.)

For additional design information please see performance curves NH, which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
SST4416	-6	-30	4.5	15

SOT-23 TOP VIEW



1 SOURCE
2 DRAIN
3 GATE

PRODUCT MARKING	
SST4416	H16

SIMILAR PRODUCTS

- TO-72, See 2N4416
- TO-92, See PN4416
- Chips, Order PN4416CHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-30	V
Gate-Source Voltage	V_{GS}	-30	
Gate Current	I_G	10	mA
Power Dissipation	P_D	350	mW
Power Derating		3.18	mW/°C
Operating Junction Temperature	T_J	-55 to 135	°C
Storage Temperature	T_{stg}	-65 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				SST4416		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-36	-30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 1 nA	-3		-6	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V	10	5	15	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-0.002		-1	nA
		T_A = 125°C	-0.6			
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 1 mA	-20			pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 10 V, V_{GS} = -6 V	2			pA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA	150			Ω
Gate-Source Forward Voltage	$V_{GS(f)}$	I_G = 1 mA, V_{DS} = 0 V	0.7			V
DYNAMIC						
Common-Source Forward Transconductance[3]	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 kHz	6	4.5	7.5	mS
Common-Source Output Conductance[3]	g_{os}		15		50	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	2.2		4	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		0.7		0.8	pF
Common-Source Output Capacitance	C_{oss}		1		2	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 100 Hz	9			$nV/\sqrt{Hz}$

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

4

SST4859 SERIES

Siliconix incorporated

N-Channel JFET

The SST4859 Series is the surface mount equivalent of our 2N4859 device types. Its low cost and $r_{DS(on)}$ make it a good choice for an all-purpose analog switch, while its high g_{fs} and good frequency response also make this product useful in a high-gain amplifier mode. Like all SOT-23 products available from Siliconix, tape and reel capabilities exist for automated assembly. (See Section 8.)

For further design information please consult the typical performance curves NCB which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	$I_{D(OFF)}$ TYP (pA)	t_{ON} TYP (ns)
SST4859	-10	25	5	2
SST4860	-6	40	5	3
SST4861	-4	60	5	4

SOT-23 TOP VIEW

1 GATE
2 DRAIN
3 SOURCE

SIMILAR PRODUCTS

- TO-18, See 2N4859 Series
- TO-92, See PN4091 Series
- Duals, See 2N5564 Series
- Chips, Order 2N485XCHP Series

PRODUCT MARKING	
SST4859	C59
SST4860	C60
SST4861	C61

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-30	V
Gate-Source Voltage	V_{GS}	-30	
Gate Current	I_G	50	mA
Power Dissipation	P_D	350	mW
Power Derating		2.8	mW/°C
Operating Junction Temperature	T_J	-55 to 150	°C
Storage Temperature	T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				SST4859		SST4860		SST4861		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-55	-30		-30		-30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 10 nA		-4	-10	-2	-6	-0.8	-4	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		50		20	100	8	80	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-0.005		-1		-1		-1	nA
		T_A = 125°C	-3							
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 10 mA	-5							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 15 V, V_{GS} = -10 V	0.005		1		1		1	nA
		V_{DS} = 15 V, V_{GS} = -10 V, T_A = 125°C	3							
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA			25		40		60	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 20 V, I_D = 1 mA, f = 1 kHz	6							mS
Common-Source Output Conductance	g_{os}		25							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V, f = 1 kHz			25		40		60	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = -10 V, f = 1 MHz	7							pF
Common-Source Reverse Transfer Capacitance	C_{rss}		3							pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 10 mA, f = 1 kHz	3							$nV/\sqrt{Hz}$
SWITCHING										
Turn-on Time	$t_{d(ON)}$	V_{DD} = 10 V, $V_{GS(ON)}$ = 0 V	2							ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	2							ns
Turn-off Time	$t_{d(OFF)}$	SST4859 20 mA -10 V 464 Ω SST4860 10 mA -6 V 953 Ω	8							ns
	t_f	SST4861 5 mA -4 V 1910 Ω	5							ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

4

SST5114 SERIES

Siliconix incorporated

P-Channel JFETs

The SST5114 Series is a p-channel JFET analog switch designed to complement our n-channel SST4391 Series. They feature low on-resistance and good off-isolation as well as the fast switching associated with JFETs. They are housed in SOT-23 packages and are available tape and reeled to support automated assembly. (See Section 8.)

For additional design information please see performance curves PSCIA, which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	$I_{D(OFF)}$ MAX (pA)	t_{ON} MAX (ns)
SST5114	10	75	-500	16
SST5115	6	100	-500	30
SST5116	4	150	-500	60

SOT-23 **TOP VIEW**

1 GATE
2 DRAIN
3 SOURCE

SIMILAR PRODUCTS

- TO-18, See 2N5114 Series
- TO-92, See J174 Series
- Chips, Order 2N511XCHP

PRODUCT MARKING	
SST5114	S14
SST5115	S15
SST5116	S16

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	30	V
Gate-Source Voltage	V_{GS}	30	
Gate Current	I_G	50	mA
Power Dissipation	P_D	350	mW
Power Derating		2.8	mW/°C
Operating Junction Temperature	T_J	-55 to 150	°C
Storage Temperature	T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS [1]				LIMITS							
					SST5114		SST5115		SST5116		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC											
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA, V_{DS} = 0 V		45	30		30		30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = -15 V, I_D = -1 nA			5	10	3	6	1	4	V
Saturation Drain Current[3]	I_{DSS}	V_{GS} = 0 V	V_{DS} = -18 V		-30	-90					mA
			V_{DS} = -15 V				-15	-60	-5	-25	mA
Gate Reverse Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V		5		500		500		500	pA
			T_A = 150°C	0.01							µA
Gate Operating Current	I_G	V_{DG} = -15 V, I_D = -1 mA		5							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = -15 V	V_{GS} = 12 V	-10		-500					pA
			V_{GS} = 7 V	-10				-500			pA
			V_{GS} = 5 V	-10						-500	pA
		V_{DS} = -15 V, T_A = 150°C	V_{GS} = 12 V	-0.02							nA
			V_{GS} = 7 V	-0.02							nA
			V_{GS} = 5 V	-0.02							nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = -1 mA				75		100		150	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = -1 mA, V_{DS} = 0 V		-0.7		-1		-1		-1	V
DYNAMIC											
Common-Source Forward Transconductance	g_{fs}	V_{DG} = -15 V, I_D = -1 mA, f = 1 kHz		4.5							mS
Common-Source Output Conductance	g_{os}	V_{DG} = -15 V, I_D = -1 mA, f = 1 kHz		20							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0, f = 1 kHz				75		100		150	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = -15 V, V_{GS} = 0 V, f = 1 MHz		20							pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, f = 1 MHz	V_{GS} = 12 V	5							pF
			V_{GS} = 7 V	6							pF
			V_{GS} = 5 V	6							pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = -10 V, I_D = -1 mA, f = 1 kHz		20							$nV/\sqrt{Hz}$
SWITCHING											
Turn-on Time	$t_{d(ON)}$	$V_{GS(ON)}$ = 0 V				6		10		25	ns
	t_r	P/N: SST5114	V_{DD} -10 V, $I_{D(ON)}$ -15 mA, $V_{GS(OFF)}$ 20 V, R_L 130 Ω			10		20		35	ns
Turn-off Time	$t_{d(OFF)}$	SST5115	-6 V, -7 mA, 12 V, 900 Ω			6		8		20	ns
	t_f	SST5116	-6 V, -3 mA, 8 V, 2000 Ω			15		30		60	ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

4

SST5912

Siliconix incorporated

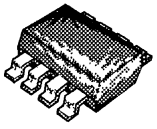
N-Channel JFET Pair

The SST5912 is a monolithic pair of JFETs mounted in a single SO-8 package. The SST5912 features high speed amplification (slew rate), high gain (typically > 6 mS), and low gate leakage (typically < 1 pA). This performance makes these devices perfect for use as wideband differential amplifiers in demanding test and measurement applications. Finally, its SO-8 package is available in tape and reel to support automated assembly. (See Section 8.)

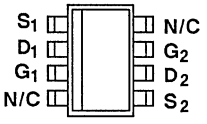
For additional design information please see performance curves NNZ, which are located in Section 7.

PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G MAX (pA)	$\lvert V_{GS_1} - V_{GS_2} \rvert$ MAX (mV)
SST5912	-25	5	-100	15

SO-8



TOP VIEW



SIMILAR PRODUCTS

- TO-78, See M5911 Series
- Low Noise, See SST404 Series
- Chips, Order M5912CHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMIT	UNITS
Gate-Drain Voltage		V_{GD}	-25	V
Gate-Source Voltage		V_{GS}	-25	
Forward Gate Current		I_G	50	mA
Power Dissipation	Per Side	P_D	300	mW
	Total		500	
Power Derating	Per Side		2.4	mW/°C
	Total		4	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature		T_{stg}	-65 to 150	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

ELECTRICAL CHARACTERISTICS[1]				LIMITS		
				SST5912		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-35	-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA	-3.5	-1	-5	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	15	7	40	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-1		-100	pA
		T_A = 125°C	-0.2			nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 5 mA	-1		-100	pA
		T_A = 125°C	-0.2			nA
Gate-Source Voltage	V_{GS}	V_{DG} = 10 V, I_D = 5 mA	-1.5	-0.3	-4	V
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7			V
DYNAMIC						
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 5 mA, f = 1 kHz	6	5	10	mS
Common-Source Output Conductance	g_{os}		20		100	µS
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 5 mA, f = 100 MHz	6	5	10	mS
Common-Source Output Conductance	g_{os}		30		150	µS
Common-Source Input Capacitance	C_{iss}	V_{DG} = 10 V, I_D = 5 mA, f = 1 MHz	3.5		5	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1		1.2	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 5 mA, f = 10 kHz	4		20	$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DG} = 10 V, I_D = 5 mA, f = 10 kHz, R_G = 100 kΩ	0.1		1	dB
MATCHING						
Differential Gate-Source Voltage	$\lvert V_{GS1}-V_{GS2}\rvert$	V_{DG} = 10 V, I_D = 5 mA	7		15	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	V_{DG} = 10 V, I_D = 5 mA, T = -55 to 25°C	10		40	µV/°C
		T = 25 to 125°C	10		40	
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 10 V, V_{GS} = 0 V	0.98	0.95	1	
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V_{DG} = 10 V, I_D = 5 mA, f = 1 kHz	0.98	0.95	1	
Differential Gate Current	$\lvert I_{G1}-I_{G2}\rvert$	V_{DG} = 10 V, I_D = 5 mA, T_A = 125°C	0.01		20	nA
Common Mode Rejection Ratio	CMRR	V_{DD} = 5 to 10 V, I_D = 5 mA	90			dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

4

SST6908 SERIES

Siliconix incorporated

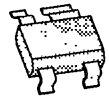
N-Channel JFET Circuits

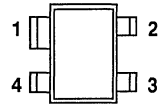
The SST6908 Series is much more than a JFET. The addition of back-to-back diodes effectively clamps input "over-voltage" while a high-performance JFET provides an effective amplification stage. With the addition of a source resistor, a complete common-source amplifier is created which provides both low leakage and very low noise. This performance is especially effective as a small signal pre-amplifier as well as impedance matching between low and high impedance sources. Finally, its SOT-143 package provides a cost effective design solution and is available tape and reeled to support automated assembly. (See Section 8.)

For additional design information please see performance curves NBB, which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (μS)	I_{DSS} MAX (mA)
SST6908	-1.8	-30	100	2
SST6909	-2.3	-30	400	3.5
SST6910	-3.5	-30	1200	5

SOT-143 **TOP VIEW**

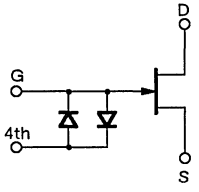




1 GATE
2 DRAIN
3 SOURCE
4 DIODES (4TH)

SIMILAR PRODUCTS

- TO-72, See 2N6908 Series
- Chips, Order 2N69XXCHP



PRODUCT MARKING	
SST6908	B08
SST6909	B09
SST6910	B10

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-30	V
Gate-Source Voltage	V_{GS}	-30	
Forward Gate Current	I_G	10	mA
Power Dissipation	P_D	350	mW
Power Derating		2.8	mW/°C
Operating Junction Temperature	T_J	-55 to 150	°C
Storage Temperature	T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				SST6908		SST6909		SST6910		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V, V_{G4} = 0 V	-50	-30		-30		-30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA, V_{G4} = 0 V		-0.3	-1.8	-0.6	-2.3	-0.9	-3.5	
Saturation Drain Current [3]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V, V_{G4} = 0 V		0.05	2	0.2	3.5	0.6	5	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V, V_{G4} = 0 V	-2		-25		-25		-25	pA
		T_A = 125°C	-1							nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 50 µA	-2							pA
Forward Gate Diode Current 4	I_{G4}	V_{G4} = ± 100 mV	± 1		± 10		± 10		± 10	
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = ± 0.5 mA, V_{DS} = 0 V, V_{G4} = 0 V	± 0.7		± 1.2		± 1.2		± 1.2	V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V, V_{G4} = 0 V, f = 1 kHz		0.1	3	0.4	3.5	1.2	4	mS
Common-Source Output Conductance	g_{os}				50		75		100	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, V_{G4} = 0 V, f = 1 MHz	3.2		5		5		5	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.5		2		2		2	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 10 Hz	12		25		25		25	$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 kHz, R_G = 1 MΩ	0.1		1		1		1	dB

NOTES:
1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.
4. Forward diode current when a voltage is applied between gate and fourth lead.

SSTDPAD5 SERIES

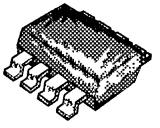
Siliconix incorporated

Dual Low-Leakage Pico-Amp Diodes

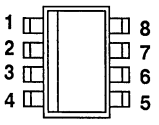
The SSTDPAD5 Series of extremely low-leakage diodes provides a superior alternative to conventional diode technology when reverse current (leakage) must be minimized. These devices feature leakage currents ranging from -5 pA (SSTDPAD5) to -100 pA (SSTDPAD100) to support a wide range of applications. With two diodes per package, the SSTDPAD5 Series is well suited for use in applications such as input protection for operational amplifiers. Its SO-8 package allows designers to maximize circuit performance while maintaining the objectives of low cost and compact packaging. Tape and reel is available for use with automated assembly techniques. (See Section 8.)

PART NO.	I_R (pA)
SSTDPAD5	-5
SSTDPAD10	-10
SSTDPAD20	-20
SSTDPAD50	-50
SSTDPAD100	-100

SO-8



TOP VIEW



1 CATHODE 1
2 CATHODE 1
3 ANODE 1
4 N/C
5 CATHODE 2
6 CATHODE 2
7 ANODE 2
8 N/C

SIMILAR PRODUCTS

- TO-71/TO-78, See DPAD1 Series
- TO-92, See JPAD5 Series
- SOT-23, See SSTPAD5 Series
- TO-18, See PAD1 Series
- Chips, Order DPADXXCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Forward Current	I_F	50	mA
Total Device Dissipation	P_D	400	mW
Storage Temperature	T_{stg}	-55 to 125	°C
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS [1]							
				LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS		TYP [2]	MIN	MAX	UNIT
STATIC							
Reverse Current	I_R	V_R = -20 V	SSTDPAD5	-2		-5	pA
			SSTDPAD10	-2		-10	
			SSTDPAD20	-5		-20	
			SSTDPAD50	-10		-50	
			SSTDPAD100	-10		-100	
Reverse Breakdown Voltage	BV_R	I_R = -1 µA		-50	-30		V
Forward Voltage Drop	V_F	I_F = 1 mA		0.8		1.5	
DYNAMIC							
Reverse Capacitance	C_R	V_R = -5 V, f = 1 MHz		2		4	pF
Differential Capacitance	$\lvert C_{R1} - C_{R2} \rvert$	$V_{R1} = V_{R2}$ = -5 V, f = 1 MHz		0.1		0.5	

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.

SSTPAD5 SERIES

Siliconix incorporated

Low-Leakage Pico-Amp Diodes

The SSTPAD5 Series of low-leakage diodes provides a superior alternative to conventional diode technology when reverse current (leakage) must be minimized. These devices feature leakage currents ranging from –5 pA (SSTPAD5) to –500 pA (SSTPAD500) to support varying system requirements. Its SOT-23 package allows designers to maximize circuit performance while maintaining the objectives of low cost and compact packaging. Tape and reel is available for use with automated assembly techniques. (See Section 8.)

PART NO.	I_R (pA)
SSTPAD5	–5
SSTPAD10	–10
SSTPAD20	–20
SSTPAD50	–50
SSTPAD100	–100
SSTPAD200	–200
SSTPAD500	–500

SIMILAR PRODUCTS

- TO-92, See JPAD5 Series
- TO-18, See PAD1 Series
- Duals, See SSTDPAD5 Series
- Chips, Order PADXXCHP

PRODUCT MARKING	
SSTPAD5	005
SSTPAD10	010
SSTPAD20	020
SSTPAD50	050
SSTPAD100	100
SSTPAD200	200
SSTPAD500	500

SOT-23 TOP VIEW

1 ANODE
2 CATHODE
3 CATHODE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Forward Current	I_F	10	mA
Total Device Dissipation	P_D	350	mW
Storage Temperature	T_{stg}	–55 to 150	°C
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS [1]							
				LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS		TYP [2]	MIN	MAX	UNIT
STATIC							
Reverse Current	I_R	V_R = -20 V	SSTPAD5	-1		-5	pA
			SSTPAD10	-2		-10	
			SSTPAD20	-4		-20	
			SSTPAD50	-5		-50	
			SSTPAD100	-10		-100	
			SSTPAD200	-15		-200	
			SSTPAD500	-25		-500	
Reverse Breakdown Voltage	BV_R	I_R = -1 µA		-60	-35		V
Forward Voltage Drop	V_F	I_F = 5 mA		0.8		1.5	
DYNAMIC							
Reverse Capacitance	C_R	V_R = -5 V, f = 1 MHz		1.5		2	pF

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.

U290 SERIES

Siliconix incorporated

N-Channel JFET

The U290 Series is a high-performance JFET analog switch which offers ultra low on-resistance and fast switching. It features the lowest available on-resistance of any JFET available in the industry today. It is packaged in a hermetically sealed TO-52 can which makes it suitable for military applications. (See Section 1 for details.)

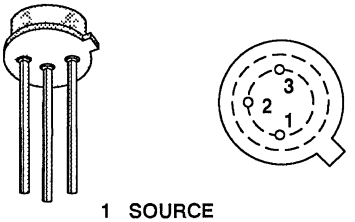
For further design information please consult the typical performance curves NVA which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	$I_{D(OFF)}$ MAX (nA)	t_{ON} MAX (ns)
U290	-10	3	1	35
U291	-4.5	7	1	35

SIMILAR PRODUCTS

- TO-92, See J105 Series
- Chips, Order U29XCHP

TO-206AC (TO-52) BOTTOM VIEW



1 SOURCE
2 DRAIN
3 GATE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-30	V
Gate-Source Voltage	V_{GS}	-30	
Gate Current	I_G	100	mA
Power Dissipation	P_D	500	mW
Power Derating		4.0	mW/°C
Operating Junction Temperature	T_J	-55 to 150	°C
Storage Temperature	T_{stg}	-65 to 200	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS [1]			LIMITS					
				U290		U291		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-35	-30		-30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 3 nA		-4	-10	-1.5	-4.5	V
Saturation Drain Current [3]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V		500		200		mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-0.02		-1		-1	nA
		T_A = 150°C	-0.04		-1		-1	µA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 25 mA	-0.01					nA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 5 V, V_{GS} = -10 V	0.01		1		1	nA
		V_{DS} = 5 V, V_{GS} = -10 V, T_A = 150°C	0.02		1		1	µA
Drain-Source On-Voltage	$V_{DS(ON)}$	V_{GS} = 0 V, I_D = 10 mA			30		70	mV
Drain-Source On-Resistance	$r_{DS(ON)}$				3		7	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 25 mA, f = 1 kHz	55					mS
Common-Source Output Conductance	g_{os}		5					µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 mA, f = 1 kHz			3		7	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = 0 V, f = 1 MHz	120		160		160	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} = -15 V, f = 1 MHz	20		30		30	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 25 mA, f = 1 kHz	3					$nV/\sqrt{Hz}$
SWITCHING								
Turn-on Time	$t_{d(ON)}$	V_{DD} = 1.5 V, $V_{GS(ON)}$ = 0 V	6		15		15	ns
	t_r	P/N: U290 — $I_{D(ON)}$ 30 mA, $V_{GS(OFF)}$ -12 V, R_L 50 Ω; U291 — 30 mA, -7 V, 50 Ω	8		20		20	ns
Turn-off Time	$t_{d(OFF)}$		5		15		15	ns
	t_f		9		20		20	ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

4

U308 SERIES

Siliconix incorporated

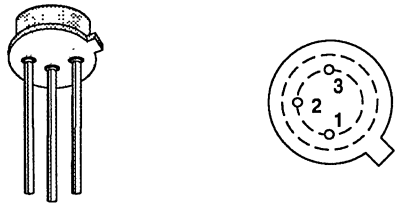
N-Channel JFETs

The U308 Series offers superb amplification characteristics. High-gain (> 10,000 µS), low noise (typically < 6 $nV\sqrt{Hz}$) and low gate leakage (typically < 2 pA) are features of this series. Of special interest, however, is performance at high frequency. Even at 450 MHz, the U308 Series offers high power gain and low noise. Finally, with its TO-52 hermetically sealed package, full military processing is available. (See Section 1.)

For additional design information and a closer look at high-frequency characteristics, please consult performance curves NZB which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
U308	-6	-25	10	60
U309	-4	-25	10	30
U310	-6	-25	10	60

TO-206AC (TO-52) **BOTTOM VIEW**



1 SOURCE
2 DRAIN
3 GATE

SIMILAR PRODUCTS

- TO-92, See J308 Series
- SOT-23, See SST308 Series
- Dual, See U430 Series
- Chips, Order U30XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	
Gate Current	I_G	20	mA
Power Dissipation	P_D	500	mW
Power Derating		4	mW/°C
Operating Junction Temperature	T_J	-55 to 150	°C
Storage Temperature	T_{stg}	-65 to 175	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS[1]				LIMITS							
					U308		U309		U310		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = −1 µA, V_{DS} = 0 V	−35	−25		−25		−25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA		−1	−6	−1	−4	−2.5	−6	
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V		12	60	12	30	24	60	mA
Gate Reverse Current	I_{GSS}	V_{GS} = −15 V, V_{DS} = 0 V	−2		−150		−150		−150	pA
		T_A = 125°C	−0.8		−150		−150		−150	nA
Gate Operating Current	I_G	V_{DG} = 9 V, I_D = 10 mA	−15							pA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA	35							Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 10 mA, V_{DS} = 0 V	0.7		1		1		1	V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 10 mA, f = 1 kHz	14	10		10		10		mS
Common-Source Output Conductance	g_{os}		110		250		250		250	µS
Common-Source Input Capacitance	C_{iss}	V_{GS} = −10 V, V_{DS} = 10 V, f = 1 MHz	4		5		5		5	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.9		2.5		2.5		2.5	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, I_D = 10 mA, f = 100 Hz	6							$nV/\sqrt{Hz}$
HIGH FREQUENCY										
Common-Gate Foward Transconductance	g_{fg}	V_{DS} = 10 V, I_D = 10 mA, f = 105 MHz	15							mS
		f = 450 MHz	13							
Common-Gate Output Conductance	g_{og}	f = 105 MHz	0.16							
		f = 450 MHz	0.55							
Common-Gate Power Gain[4]	G_{pg}	f = 105 MHz	16	14		14		14		dB
		f = 450 MHz	11.5	10		10		10		
Noise Figure	NF	f = 105 MHz	1.5		2		2		2	
		f = 450 MHz	2.7		3.5		3.5		3.5	

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.
4. Gain (G_{pg}) measured at optimum input noise match.

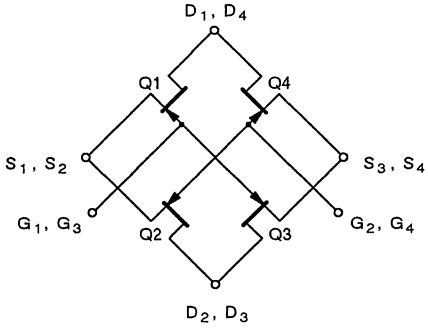
U350

Siliconix incorporated

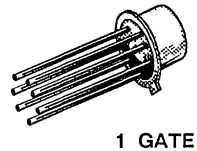
N-Channel JFET Ring Demodulator

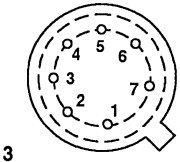
The U350 is a set of four matched n-channel JFETs connected as a ring demodulator. The matched set of JFETs has low $r_{DS(ON)}$, high g_{fs}, and square law operation which gives high conversion gain and a very high intermodulation intercept point. Best device performance is in the HF-VHF frequency range. The hermetic TO-99 package shields the die set as well as lending itself to military processing.

PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{GSS} MAX (nA)	NF TYP (dB)
U350	-25	10	-1	7



TO-99 (TO-78) BOTTOM VIEW





1 GATE 1, GATE 3
2 DRAIN 1, DRAIN 4
3 SOURCE 1, SOURCE 2
4 GND & CASE
5 SOURCE 3, SOURCE 4
6 DRAIN 2, DRAIN 3
7 GATE 2, GATE 4

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-25	V
Gate-Source Voltage	V_{GS}	-25	
Forward Gate Current	I_G	25	mA
Power Dissipation	P_D	1	W
Power Derating		8	mW/°C
Operating Junction Temperature	T_J	-55 to 150	°C
Storage Temperature	T_{stg}	-65 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				U350		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-35	-25		V
Gate-Source Cutoff Voltage[4]	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA	-3	-2	-6	V
Saturation Drain Current[3, 4]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V	45	24	60	mA
Gate Reverse Current[4]	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-0.002		-1	nA
		T_A = 125°C	-0.001		-1	µA
Gate-Source Forward Voltage[4]	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7		1	V
DYNAMIC						
Common-Source Forward Transconductance[4]	g_{fs}	V_{DS} = 10 V, I_D = 10 mA, f = 1 kHz	15	10	18	mS
Common-Source Output Conductance[4]	g_{os}		100		150	µS
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 0 mA, f = 1kHz	33		90	Ω
Common-Source Input Capacitance	C_{gs}	V_{GS} = -10 V, I_D = 0 mA, f = 1 MHz	4		5	pF
Common-Source Reverse Transfer Capacitance	C_{gd}	V_{GD} = -10 V, I_S = 0 mA, f = 1 MHz	2		2.5	pF
Conversion Gain	G_c	V_{DS} = 20 V, V_{GS} = ½$V_{GS(OFF)}$, f = 100 MHz, R_L = 1700 Ω, See Figure 1	4			dB
Noise Figure	NF		7			dB
Intercept Point			33			dBm
MATCHING						
Saturation Drain Current Ratio[3]	$\frac{I_{DSS}}{I_{DSS}}$	V_{DS} = 15 V, V_{GS} = 0 V	0.95	0.9	1	
Transconductance Ratio	$\frac{g_{fs}}{g_{fs}}$	V_{DS} = 15 V, I_D = 10 mA, f = 1 kHz	0.95	0.9	1	
Output Conductance Ratio	$\frac{g_{os}}{g_{os}}$		0.95	0.9	1	
Gate-Source Cutoff Voltage Ratio	$\frac{V_{GS(OFF)}}{V_{GS(OFF)}}$	V_{DS} = 15 V, I_D = 1 nA	0.95	0.9	1	

NOTES:
1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.
4. Other gate terminal clamped to -8 V.

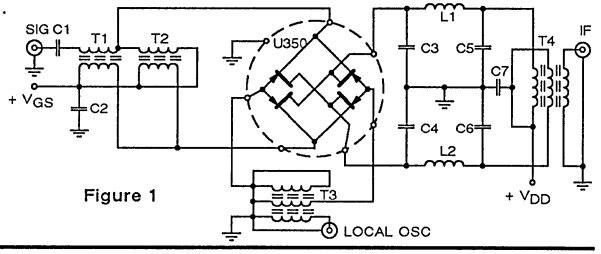


Figure 1

4

U401 SERIES

Siliconix incorporated

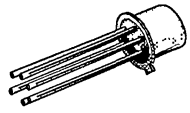
N-Channel JFETs

The U401 Series of high-performance monolithic dual JFETs features extremely low noise, tight offset voltage and drift over temperature specifications. It is targeted for use in a wide range of precision instrumentation applications. The U401 Series has a wide selection of both offset and drift specifications with the prime device, the U401, featuring 5 mV offset and 10 μV/°C drift. The six devices allow designers to make important cost/benefit decisions. This series is available in a TO-71 hermetically sealed package and is available with military screening. (See Section 1.)

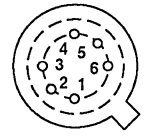
For additional design information please see performance curves NNR, which are located in Section 7.

PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G MAX (pA)	$\lvert V_{GS_1} - V_{GS_2} \rvert$ MAX (mV)
U401	-50	2	-15	5
U402	-50	2	-15	10
U403	-50	2	-15	10
U404	-50	2	-15	15
U405	-50	2	-15	20
U406	-50	2	-15	40

TO-71



BOTTOM VIEW



1 SOURCE 1
2 DRAIN 1
3 GATE 1
4 SOURCE 2
5 DRAIN 2
6 GATE 2

SIMILAR PRODUCTS

- High-Gain, See 2N5911 Series
- SO-8, See SST404 Series
- Chips, Order U40XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMIT	UNITS
Gate-Drain Voltage		V_{GD}	-50	V
Gate-Source Voltage		V_{GS}	-50	
Forward Gate Current		I_G	10	mA
Power Dissipation	Per Side	P_D	300	mW
	Total		500	
Power Derating	Per Side		2.4	mW/°C
	Total		4	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature		T_{stg}	-65 to 200	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

ELECTRICAL CHARACTERISTICS[1]			LIMITS							
				U401		U402		U403		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-58	-50		-50		-50		V
Gate-Gate Breakdown Voltage	$V_{(BR)G1-G2}$	I_G = ±1 µA, V_{DS} = 0 V, V_{GS} = 0 V	-58	±50		±50		±50		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 1 nA	-1.5	-0.5	-2.5	-0.5	-2.5	-0.5	-2.5	V
Saturation Drain[3] Current	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	3.5	0.5	10	0.5	10	0.5	10	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -30 V, V_{DS} = 0 V	-2		-25		-25		-25	pA
		T_A = 125°C	-1							nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 200 µA	-2		-15		-15		-15	pA
		T_A = 125°C	-0.8		-10		-10		-10	nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 0.1 mA	250							Ω
Gate-Source Voltage	V_{GS}	V_{DG} = 15 V, I_D = 200 µA	-1		-2.3		-2.3		-2.3	V
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 15 V, I_D = 200 µA, f = 1 kHz	1.5	1	2	1	2	1	2	mS
Common-Source Output Conductance	g_{os}		1.3		2		2		2	µS
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	4	2	7	2	7	2	7	mS
Common-Source Output Conductance	g_{os}		5		20		20		20	µS
Common-Source Input Capacitance	C_{iss}	V_{DG} = 15 V, I_D = 200 µA, f = 1 MHz	4		8		8		8	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.5		3		3		3	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 15 V, I_D = 200 µA, f = 10 Hz	10		20		20		20	$nV/\sqrt{Hz}$
MATCHING										
Differential Gate-Source Voltage	$\lvert V_{GS1}-V_{GS2}\rvert$	V_{DG} = 10 V, I_D = 200 µA			5		10		10	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	V_{DG} = 10 V, I_D = 200 µA, T = -55 to 25°C			10		10		25	µV/°C
		T = 25 to 125°C			10		10		25	µV/°C
Common Mode Rejection Ratio	CMRR	V_{DG} = 10 to 20 V, I_D = 200 µA	102	95		95		95		dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

4

Siliconix incorporated

ELECTRICAL CHARACTERISTICS[1]			LIMITS							
				U404		U405		U406		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = −1 µA, V_{DS} = 0 V	−58	−50		−50		−50		V
Gate-Gate Breakdown Voltage	$V_{(BR)G1-G2}$	I_G = ±1 µA, V_{DS} = 0 V, V_{GS} = 0 V	−58	±50		±50		±50		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 1 nA	−1.5	−0.5	−2.5	−0.5	−2.5	−0.5	−2.5	V
Saturation Drain[3] Current	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	3.5	0.5	10	0.5	10	0.5	10	mA
Gate Reverse Current	I_{GSS}	V_{GS} = −30 V, V_{DS} = 0 V	−2		−25		−25		−25	pA
		T_A = 125°C	−1							nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 200 µA	−2		−15		−15		−15	pA
		T_A = 125°C	−0.8		−10		−10		−10	nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 0.1 mA	250							Ω
Gate-Source Voltage	V_{GS}	V_{DG} = 15 V, I_D = 200 µA	−1		−2.3		−2.3		−2.3	V
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 15 V, I_D = 200 µA, f = 1 kHz	1.5	1	2	1	2	1	2	mS
Common-Source Output Conductance	g_{os}		1.3		2		2		2	µS
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	4	2	7	2	7	2	7	mS
Common-Source Output Conductance	g_{os}		5		20		20		20	µS
Common-Source Input Capacitance	C_{iss}	V_{DG} = 15 V, I_D = 200 µA, f = 1 MHz	4		8		8		8	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.5		3		3		3	pF
Equivalent Input Noise Voltage	$\overline{e}_n$	V_{DG} = 15 V, I_D = 200 µA, f = 10 Hz	10		20		20		20	$nV/\sqrt{Hz}$
MATCHING										
Differential Gate-Source Voltage	$\lvert V_{GS1}-V_{GS2}\rvert$	V_{DG} = 10 V, I_D = 200 µA			15		20		40	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	V_{DG} = 10 V, I_D = 200 µA, T = −55 to 25°C			25		40		80	µV/°C
		V_{DG} = 10 V, I_D = 200 µA, T = 25 to 125°C			25		40		80	µV/°C
Common Mode Rejection Ratio	CMRR	V_{DG} = 10 to 20 V, I_D = 200 µA	102	95		90				dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

Siliconix incorporated

U421 SERIES

N-Channel JFET Pairs

The U421 Series are monolithic pairs of n-channel JFETs designed to provide very high input impedance for differential amplification and impedance matching. Among its many unique features, this series offers operating gate current specified at -250 fA (U421-3), high gain at low operating currents , and tight matching (10 mV for U421 and U424). Additionally, its TO-78 package is hermetically sealed and may be screened per MIL-S-19500. (See Section 1.)

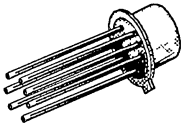
For additional design information please see performance curves NNT, which are located in Section 7.

PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G MAX (pA)	$\lvert V_{GS_1} - V_{GS_2} \rvert$ MAX (mV)
U421	-40	0.3	-0.25	10
U422	-40	0.3	-0.25	15
U423	-40	0.3	-0.25	25
U424	-40	0.3	-0.5	10
U425	-40	0.3	-0.5	15
U426	-40	0.3	-0.5	25

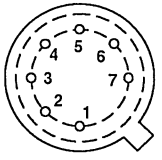
SIMILAR PRODUCTS

- Low-Noise, See U401 Series
- High-Gain, See 2N5911 Series
- Chips, Order U42XCHP

TO-78



BOTTOM VIEW



1 SOURCE 1
2 DRAIN 1
3 GATE 1
4 CASE
5 SOURCE 2
6 DRAIN 2
7 GATE 2

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMIT	UNITS
Gate-Drain Voltage		V_{GD}	-40	V
Gate-Source Voltage		V_{GS}	-40	
Gate-Gate Voltage		V_{GG}	± 40	
Forward Gate Current		I_G	10	mA
Power Dissipation	Per Side	P_D	400	mW
	Total		750	
Power Derating	Per Side		3.2	mW/°C
	Total		6	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature		T_{stg}	-65 to 150	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

4

ELECTRICAL CHARACTERISTICS[1]			LIMITS							
				U421		U422		U423		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-60	-40		-40		-40		V
Gate-Gate Breakdown Voltage	V_{GG}	I_G = -1 µA, I_D = 0, I_S = 0	±55	±40		±40		±40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA	-1.2	-0.4	-2	-0.4	-2	-0.4	-2	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	400	60	1000	60	1000	60	1000	µA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-0.6		-1		-1		-1	pA
		T_A = 125°C	-0.3		-1		-1		-1	nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 30 µA	-0.2		-0.25		-0.25		-0.25	pA
		T_A = 125°C	-150		-250		-250		-250	
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 10 µA	2000							Ω
Gate-Source Voltage	V_{GS}	V_{DG} = 10 V, I_D = 30 µA	-0.8		-1.8		-1.8		-1.8	V
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	0.6	0.3	1.5	0.3	1.5	0.3	1.5	mS
Common-Source Output Conductance	g_{os}		4		10		10		10	µS
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 30 µA, f = 1 kHz	0.2	0.12	0.35	0.12	0.35	0.12	0.35	mS
Common-Source Output Conductance	g_{os}		0.4		3		3		3	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	1.4		3		3		3	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		0.7		1.5		1.5		1.5	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 30 µA, f = 10 Hz	30		70		70		70	$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DG} = 10 V, I_D = 30 µA, f = 10 Hz, R_G = 10 MΩ			1		1		1	dB
MATCHING										
Differential Gate-Source Voltage	$\lvert V_{GS1}-V_{GS2}\rvert$	V_{DG} = 10 V, I_D = 30 µA			10		15		25	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	V_{DG} = 10 V, I_D = 30 µA, T = -55 to 25°C			10		25		40	µV/°C
		T = 25 to 125°C			10		25		40	
Common Mode Rejection Ratio	CMRR	V_{DG} = 10 to 20 V, I_D = 30 µA	102	90		80		80		dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

ELECTRICAL CHARACTERISTICS[1]			LIMITS							
				U424		U425		U426		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-60	-40		-40		-40		V
Gate-Gate Breakdown Voltage	V_{GG}	I_G = -1 µA, I_D = 0, I_S = 0	±55	±40		±40		±40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA	-2	-0.4	-3	-0.4	-3	-0.4	-3	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	800	60	1800	60	1800	60	1800	µA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-0.8		-3		-3		-3	pA
		T_A = 125°C	-0.4		-3		-3		-3	nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 30 µA	-0.3		-0.5		-0.5		-0.5	pA
		T_A = 125°C	-200		-500		-500		-500	
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 10 µA	2000							Ω
Gate-Source Voltage	V_{GS}	V_{DG} = 10 V, I_D = 30 µA	-1.5		-2.9		-2.9		-2.9	V
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	0.6	0.3	1.5	0.3	1.5	0.3	1.5	mS
Common-Source Output Conductance	g_{os}		4		10		10		10	µS
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 30 µA, f = 1 kHz	0.2	0.12	0.35	0.12	0.35	0.12	0.35	mS
Common-Source Output Conductance	g_{os}		0.4		3		3		3	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	1.4		3		3		3	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		0.7		1.5		1.5		1.5	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 30 µA, f = 10 Hz	30		70		70		70	$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DG} = 10 V, I_D = 30 µA, f = 10 Hz, R_G = 10 MΩ			1		1		1	dB
MATCHING										
Differential Gate-Source Voltage	$\lvert V_{GS1}-V_{GS2}\rvert$	V_{DG} = 10 V, I_D = 30 µA			10		15		25	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	V_{DG} = 10 V, I_D = 30 µA, T = -55 to 25°C			10		25		40	µV/°C
		T = 25 to 125°C			10		25		40	
Common Mode Rejection Ratio	CMRR	V_{DG} = 10 to 20 V, I_D = 30 µA	100	90		80		80		dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

U430 SERIES

Siliconix incorporated

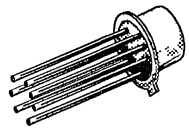
N-Channel JFET Pairs

The U430 Series are pairs of matched JFETs assembled in one TO-78 package. They feature high gain, low noise and low gate leakage and are intended for high performance, high slew rate, mixing and differential amplification. Additionally, these devices offer good power gain even as frequencies are increased beyond 250 MHz. The TO-78 package may be processed for military applications. (See Section 1.)

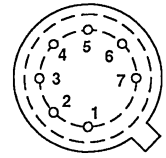
For additional design information please consult performance curves NZB which are located in Section 7.

PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G TYP (pA)	$\lvert V_{GS_1} - V_{GS_2} \rvert$ TYP (mV)
U430	-25	10	-15	25
U431	-25	10	-15	25

TO-78



BOTTOM VIEW



1 SOURCE 1
2 GATE 1
3 DRAIN 1
4 CASE
5 DRAIN 2
6 GATE 2
7 SOURCE 2

SIMILAR PRODUCTS

- Low-Noise, See U401 Series
- High-Gain, See 2N5911 Series
- Low-Leakage, See U421 Series
- Chips, Order U43XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMIT	UNITS
Gate-Drain Voltage		V_{GD}	-25	V
Gate-Source Voltage		V_{GS}	-25	
Forward Current		I_G	10	mA
Power Dissipation	Per Side	P_D	300	mW
	Total		500	
Power Derating	Per Side		2.4	mW/°C
	Total		4	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature		T_{stg}	-65 to 200	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

ELECTRICAL CHARACTERISTICS[1]			LIMITS					
				U430		U431		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-35	-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA		-1	-4	-2	-6	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V		12	30	24	60	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-5		-150		-150	pA
		T_A = 150°C	-10		-150		-150	nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 5 mA	-15					pA
		T_A = 150°C	-10					nA
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 10 mA, V_{DS} = 0 V	0.8		1		1	V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 10 mA, f = 1 kHz	15	10		10		mS
Common-Source Output Conductance	g_{os}		100		250		250	µS
Common-Source Input Capacitance	C_{iss}	V_{GS} = -10 V, V_{DS} = 0 V, f = 1 MHz	4.5		5		5	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		2		2.5		2.5	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, I_D = 10 mA, f = 100 Hz	6					$nV/\sqrt{Hz}$
HIGH FREQUENCY								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 10 mA, f = 100 MHz	14					mS
Common-Source Output Conductance	g_{os}		0.13					mS
Power-Match Source Admittance	g_{ig}		12					mS
MATCHING								
Differential Gate-Source Voltage	$\lvert V_{GS1}-V_{GS2} \rvert$	V_{DG} = 10 V, I_D = 10 mA	25					mV
Saturation Drain[4] Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 10 V, V_{GS} = 0 V	0.95	0.9	1	0.9	1	
Transconductance[4] Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V_{DS} = 10 V, I_D = 10 mA, f = 1 kHz	0.95	0.9	1	0.9	1	
Gate-Source Cutoff Voltage Ratio	$\frac{V_{GS(OFF)1}}{V_{GS(OFF)2}}$	V_{DS} = 10 V, I_D = 1 nA	0.95	0.9	1	0.9	1	
Differential Gate Current	$\lvert I_{G1}-I_{G2} \rvert$	V_{DG} = 10 V, I_D = 5 mA	-2					pA
Common Mode Rejection Ratio	CMRR	V_{DD} = 5 to 10 V, I_D = 10 mA	75					dB

NOTES: 1. T_A = 25°C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.
4. Assumes smaller value in the numerator.

4

U440 SERIES

Siliconix incorporated

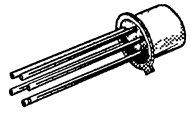
N-Channel JFET Pairs

The U440 Series are matched pairs of JFETs mounted in a single TO-71 package. This two chip design reduces parasitic performance at high frequency while ensuring extremely tight matching. The U440 features high speed amplification (slew rate), high gain (typically > 6 mS), and low gate leakage (typically < 1 pA). This performance makes these devices perfect for use as wideband differential amplifiers in demanding test and measurement applications. Finally, its TO-71 hermetically sealed package is available with military screening per MIL-S-19500. (See Section 1.)

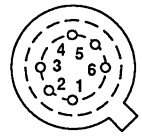
For additional design information please see performance curves NZF, which are located in Section 7.

PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G MAX (pA)	$\lvert V_{GS_1} - V_{GS_2} \rvert$ MAX (mV)
U440	-25	4.5	-500	10
U441	-25	4.5	-500	20

TO-71



BOTTOM VIEW



1 SOURCE 1
2 DRAIN 1
3 GATE 1
4 SOURCE 2
5 DRAIN 2
6 GATE 2

SIMILAR PRODUCTS

- TO-78, See U443 Series
- SO-8, See SST440 Series
- Low Noise, See U401 Series
- Low Leakage, See U421 Series
- Chips, Order U44XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMIT	UNITS
Gate-Drain Voltage		V_{GD}	-25	V
Gate-Source Voltage		V_{GS}	-25	
Gate-Gate Voltage		V_{GG}	± 50	
Gate Current		I_G	50	mA
Power Dissipation	Per Side	P_D	250	mW
	Total		350	
Power Derating	Per Side		2	mW/°C
	Total		2.8	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature		T_{stg}	-65 to 150	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

ELECTRICAL CHARACTERISTICS[1]			LIMITS					
				U440		U441		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = −1 µA, V_{DS} = 0 V	−35	−25		−25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA	−3.5	−1	−6	−1	−6	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	15	6	30	6	30	mA
Gate Reverse Current	I_{GSS}	V_{GS} = −15 V, V_{DS} = 0 V	−1		−500		−500	pA
		T_A = 150°C	−2					nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 5 mA	−1		−500		−500	pA
		T_A = 125°C	−0.3					nA
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 5 mA, f = 1 kHz	6	4.5	9	4.5	9	mS
Common-Source Output Conductance	g_{os}		70		200		200	µS
Common-Source Input Capacitance	C_{iss}	V_{DG} = 10 V, I_D = 5 mA, f = 1 MHz	3					pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1					pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 5 mA, f = 10 kHz	4					$nV/\sqrt{Hz}$
MATCHING								
Differential Gate-Source Voltage	$\lvert V_{GS1}-V_{GS2} \rvert$	V_{DG} = 10 V, I_D = 5 mA	6		10		20	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta \lvert V_{GS1}-V_{GS2} \rvert}{\Delta T}$	V_{DG} = 10 V, I_D = 5 mA, T = −55 to 25°C	20					µV/°C
		T = 25 to 125°C	20					µV/°C
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 10 V, V_{GS} = 0 V	0.97					
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V_{DG} = 10 V, I_D = 5 mA, f = 1 kHz	0.97					
Common Mode Rejection Ratio	CMRR	V_{DD} = 5 to 10 V, I_D = 5 mA	85					dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

U443 SERIES

Siliconix incorporated

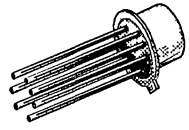
N-Channel JFET Pairs

The U443 Series are matched pairs of JFETs mounted in a single TO-78 package. This two chip design reduces parasitic performance at high frequency while ensuring extremely tight matching. The U443 features high speed amplification (slew rate), high gain (typically > 6 mS), and low gate leakage (typically < 1 pA). This performance makes these devices perfect for use as wideband differential amplifiers in demanding test and measurement applications. Finally, its TO-78 hermetically sealed package is available with military screening per MIL-S-19500. (See Section 1.)

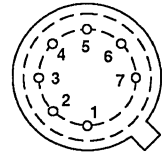
For additional design information please see performance curves NZF, which are located in Section 7.

PART NUMBER	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_G MAX (pA)	$\lvert V_{GS_1} - V_{GS_2} \rvert$ MAX (mV)
U443	-25	4.5	-500	10
U444	-25	4.5	-500	20

TO-78



BOTTOM VIEW



1 SOURCE 1
2 DRAIN 1
3 GATE 1
4 CASE
5 SOURCE 2
6 DRAIN 2
7 GATE 2

SIMILAR PRODUCTS

- TO-71, See U440 Series
- SO-8, See SST440 Series
- Low Noise, See U401 Series
- Low Leakage, See U421 Series
- Chips, Order U44XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMIT	UNITS
Gate-Drain Voltage		V_{GD}	-25	V
Gate-Source Voltage		V_{GS}	-25	
Gate-Gate Voltage		V_{GG}	± 50	
Forward Gate Current		I_G	50	mA
Power Dissipation	Per Side	P_D	367	mW
	Total		500	
Power Derating	Per Side		3	mW/°C
	Total		4	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature		T_{stg}	-65 to 150	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

ELECTRICAL CHARACTERISTICS[1]			LIMITS					
				U443		U444		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-35	-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1 nA	-3.5	-1	-6	-1	-6	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	15	6	30	6	30	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-1		-500		-500	pA
		T_A = 150°C	-2					nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 5 mA	-1		-500		-500	pA
		T_A = 125°C	-0.3					nA
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 10 V, I_D = 5 mA, f = 1 kHz	6	4.5	9	4.5	9	mS
Common-Source Output Conductance	g_{os}		70		200		200	µS
Common-Source Input Capacitance	C_{iss}	V_{DG} = 10 V, I_D = 5 mA, f = 1 MHz	3					pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1					pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 5 mA, f = 10 kHz	4					$nV/\sqrt{Hz}$
MATCHING								
Differential Gate-Source Voltage	$\lvert V_{GS1}-V_{GS2} \rvert$	V_{DG} = 10 V, I_D = 5 mA	6		10		20	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta \lvert V_{GS1}-V_{GS2} \rvert}{\Delta T}$	V_{DG} = 10 V, I_D = 5 mA, T = -55 to 25°C	20					µV/°C
		T = 25 to 125°C	20					µV/°C
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 10 V, V_{GS} = 0 V	0.97					
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	V_{DG} = 10 V, I_D = 5 mA, f = 1 kHz	0.97					
Common Mode Rejection Ratio	CMRR	V_{DD} = 5 to 10 V, I_D = 5 mA	85					dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

4

U1897 SERIES

Siliconix incorporated

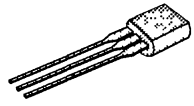
N-Channel JFET

The U1897 Series is a multi-purpose n-channel JFET designed to economically enhance circuit performance. These devices are especially well suited for analog switching applications but function efficiently as high-gain amplifiers, particularly at high-frequency. Our low-cost TO-92 packaging offers affordable performance with flexibility for designers, as these devices can be ordered with a variety of lead forms or tape and reel for automated insertion. (See Section 8.)

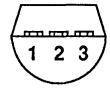
For additional design information please consult the typical performance curves NCB which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	$I_{D(OFF)}$ MAX (pA)	t_{ON} MAX (ns)
U1897	–10	30	200	25
U1898	–7	50	200	35
U1899	–5	80	200	60

TO-92



BOTTOM VIEW



1 DRAIN
2 SOURCE
3 GATE

SIMILAR PRODUCTS

- TO-18, See 2N4091 Series
- SOT-23, See SST4091 Series
- Duals, See 2N5564Series
- Chips, Order U189XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	–40	V
Gate-Source Voltage	V_{GS}	–40	
Gate Current	I_G	10	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature	T_J	–55 to 135	°C
Storage Temperature	T_{stg}	–55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				U1897		U1898		U1899		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-55	-40		-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 20 V, I_D = 1 nA		-5	-10	-2	-7	-1	-5	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V		30		15		8		mA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-5		-400		-400		-400	pA
		T_A = 85°C	-0.2							nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 10 mA	-5							
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 20 V, V_{GS} = -6 V	5						200	pA
		V_{DS} = 20 V, V_{GS} = -8 V	5				200			
		V_{DS} = 20 V, V_{GS} = -12 V	5		200					
		V_{DS} = 20 V, T_A = 85°C, V_{GS} = -6 V	0.2						10	nA
		V_{DS} = 20 V, T_A = 85°C, V_{GS} = -8 V	0.2				10			
		V_{DS} = 20 V, T_A = 85°C, V_{GS} = -12 V	0.2		10					
Drain-Source On-Voltage	$V_{DS(ON)}$	V_{GS} = 0 V, I_D = 2.5 mA	0.15						0.2	V
		V_{GS} = 0 V, I_D = 4 mA	0.15				0.2			
		V_{GS} = 0 V, I_D = 6.6 mA	0.15		0.2					
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA			30		50		80	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 20 V, I_D = 1 mA, f = 1 kHz	6							mS
Common-Source Output Conductance	g_{os}	V_{DG} = 20 V, I_D = 1 mA, f = 1 kHz	25							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 mA, f = 1 kHz			30		50		80	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	14		16		16		16	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	3		3.5		3.5		3.5	pF
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 10 mA, f = 1 kHz	3							$nV/\sqrt{Hz}$
SWITCHING										
Turn-on Time	$t_{d(ON)}$	V_{DD} = 3 V, $V_{GS(ON)}$ = 0 V	2		15		15		20	ns
	t_r	P/N: U1897 6.6 mA -12 V 430 Ω; U1898 4 mA -8 V 700 Ω; U1899 2.5 mA -6 V 1100 Ω	2		10		20		40	ns
Turn-off Time	t_{OFF}		19		40		60		80	ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

4

VCR2N, VCR4N, VCR7N, VCR3P

Siliconix incorporated

JFET Voltage Controlled Resistors

The VCR2N, VCR4N, VCR7N, and VCR3P line of JFET voltage controlled resistors utilize the JFET's linear output characteristics in the resistive region. This area of operation is around V_{DS} = 0 V and extends for a range up to several hundred millivolts – up to the point I_D begins to saturate. Key to device performance is the predictable r_{DS} change versus V_{GS} bias where:

$$r_{DS}\,\text{bias} \approx \frac{r_{DS}\ (@\ V_{GS} = 0)}{1 - \left|\dfrac{V_{GS}}{V_{GS(OFF)}}\right|}$$

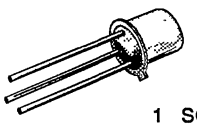
This series features three n-channel devices with $r_{DS(ON)}$ ranging from 20 – 8000 Ω. Also featured is a p-channel device with $r_{DS(ON)}$ specified between 70 and 200 Ω. All packages are hermetically sealed and may be processed per MIL-S-19500. (See Section 1.)

For additional design information please consult typical performance curves (Section 7) as follows:

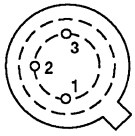
VCR2N ..... NCB
VCR4N ..... NPA
VCR7N ..... NT
VCR3P ..... PSCIA

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (Ω)	$r_{ds(ON)}$ MIN (Ω)	$r_{ds(ON)}$ MAX (Ω)
VCR2N	–3.5	–15	20	60
VCR4N	–7	–15	200	600
VCR7N	–5	–15	4000	8000
VCR3P	5	15	70	200

TO-18

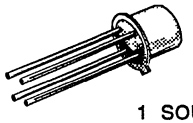


BOTTOM VIEW

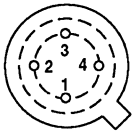


1 SOURCE
2 DRAIN
3 GATE

TO-72



BOTTOM VIEW



1 SOURCE
2 DRAIN
3 GATE
4 SUBSTRATE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT		UNITS
		VCR2N–7N	VCR3P	
Gate-Drain Voltage	V_{GD}	–15	15	V
Gate-Source Voltage	V_{GS}	–15	15	
Gate Current	I_G	10	–10	mA
Power Dissipation (Case 25°C)	P_D	300		mW
Power Derating		2		mW/°C
Operating Junction Temperature	T_J	–55 to 175		°C
Storage Temperature	T_{stg}	–55 to 175		
Lead Temperature (1/16" from case for 10 seconds)	T_L	300		

VCR2N, VCR4N, VCR7N, VCR3P

N-CHANNEL

ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				VCR2N		VCR4N		VCR7N		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-55	-15		-15		-15		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 10 V, I_D = 1µA		-1	-3.5	-3.5	-7	-2.5	-5	
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V			-5		-0.2		-0.1	nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 1 mA		20	60	200	600	4000	8000	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 A f = 1 kHz		20	60	200	600	4000	8000	Ω
Drain-Gate Capacitance	C_{dg}	V_{GD} = -10 V, I_S = 0 A f = 1 MHz			7.5		3		1.5	pF
Source-Gate Capacitance	C_{sg}	V_{GS} = -10 V, I_D = 0 A f = 1 MHz			7.5		3		1.5	

P-CHANNEL

ELECTRICAL CHARACTERISTICS [1]			LIMITS			
				VCR3P		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA, V_{DS} = 0 V	50	15		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = -10 V, I_D = -1 µA	2.5	1	5	
Gate Reverse Current	I_{GSS}	V_{GS} = 15 V, V_{DS} = 0 V	0.005		20	nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = -1 mA	100	70	200	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = -1 mA, V_{DS} = 0 V	-0.7			V
DYNAMIC						
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 A f = 1 kHz	100	70	200	Ω
Drain-Gate Capacitance	C_{dg}	V_{GD} = 10 V, I_S = 0 A f = 1 MHz	6		25	pF
Source-Gate Capacitance	C_{sg}	V_{GS} = 10 V, I_D = 0 A f = 1 MHz	6		15	

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.

DMOS

INTRODUCTION

DMOS products from Siliconix utilize a lateral double-diffused MOS process to offer the ultimate low-cost yet highly reliable switches. It's unique lateral construction affords all the benefits critical to small-signal switching applications. Ultra fast switching speed, exceptionally low capacitance, good off-isolation, and high operating frequency are all available to design engineers today!

Key applications which benefit from this technology include video switching and precision sample and hold applications. In fact, any high performance application which benefits from < 1 ns turn-on time, < 0.5 pF capacitance, and operating frequencies up to 1 GHz, should utilize Siliconix' lateral DMOS as an optimal design solution.

Packaging options are diversified and range from surface mount to hermetically sealed metal cans and both single and quad array switches may be purchased. With our high reliability silicon gate process, full military processing is available per MIL-S-19500 on all hermetically sealed packages.

For additional technical information please see "Switching DMOS Fast" (LPD-11), "An Ultra Broadband Analog Switch" (LPD-20), and "High speed Depletion-mode DMOS FETs" (LPD-12). These application notes are located in section nine and provide useful insight into device operation.

2N7104 SERIES

Siliconix incorporated

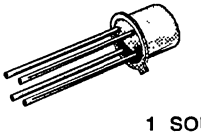
N-Channel Lateral DMOS FETs

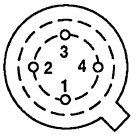
The 2N7104 Series of lateral DMOS FETs is designed for high speed switching in audio, video, and high-frequency applications. These devices are designed on the Siliconix DMOS process and utilize lateral construction to achieve low capacitance and ultra-fast switching speeds. For long term reliablitly this series features a poly-silicon gate, making Siliconix 2N7104 devices the perfect choice for high-performance military applications.

For additional design information please see performance curves DMCB, which are located in Section 7.

PART NUMBER	$V_{(BR)DS}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	C_{rss} MAX (pF)	t_{ON} MAX (ns)
2N7104	20	70	0.5	2
2N7106	10	70	0.5	2
2N7108	15	70	0.5	2

TO-72 BOTTOM VIEW





1 SOURCE
2 DRAIN
3 GATE
4 SUBSTRATE, CASE

SIMILAR PRODUCTS

- Quad Array, See 2N7116 Series
- SO-14 Array, See SD5400 Series
- Zener Protection, See 2N7105 Series
- SOT-143, See SST211 Series
- Chips, Order 2N710XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT			UNITS
		2N7104	2N7106	2N7108	
Gate-Source, Gate-Drain Gate-Substrate Voltage	V_{GS},V_{GD},V_{GB}	±40	±40	±40	V
Drain-Source Voltage	V_{DS}	30	10	20	
Source-Drain Voltage	V_{SD}	10	10	20	
Drain-Substrate Voltage	V_{DB}	30	15	25	
Source-Substrate Voltage	V_{SB}	15	15	25	
Drain Current	I_D	50	50	50	mA
Power Dissipation (T_J = 25°C)	P_D	300	300	300	mW
Power Derating		2.4	2.4	2.4	mW/°C
Operating Junction Temperature	T_J	-55 to 150			°C
Storage Temperature	T_{stg}	-65 to 200			
Lead Temperature (1/16" from case for 10 seconds)	T_L	300			

ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				2N7104		2N7106		2N7108		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Drain-Source Breakdown Voltage[3]	$V_{(BR)DS}$	$V_{GS} = V_{BS} = 0$ V, $I_D = 10\,\mu A$	35	30						V
		$V_{GS} = V_{BS} = -5$ V, $I_S = 10$ nA	30	10		10		20		
Source-Drain Breakdown Voltage[3]	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5$ V, $I_D = 10$ nA	22	10		10		20		
Drain-Substrate Breakdown Voltage[3]	$V_{(BR)DB}$	$V_{GB} = 0$ V, $I_D = 10$ nA, Source OPEN	35	15		15		25		
Source-Substrate Breakdown Voltage[3]	$V_{(BR)SB}$	$V_{GB} = 0$ V, $I_S = 10\,\mu A$, Drain OPEN	35	15		15		25		
Drain-Source Leakage	$I_{DS(OFF)}$	$V_{GS} = V_{BS} = -5$ V, $V_{DS} = 10$ V	0.4		10		10			nA
		$V_{GS} = V_{BS} = -5$ V, $V_{DS} = 20$ V	0.9						10	
		$V_{GS} = V_{BS} = -5$ V, $T_A = 125°C$, $V_{DS} = 10$ V	0.4		5		5			µA
		$V_{GS} = V_{BS} = -5$ V, $T_A = 125°C$, $V_{DS} = 20$ V	0.9						5	
Source-Drain Leakage	$I_{SD(OFF)}$	$V_{GD} = V_{BD} = -5$ V, $V_{SD} = 10$ V	0.5		10		10			nA
		$V_{GD} = V_{BD} = -5$ V, $V_{SD} = 20$ V	1						10	
		$V_{GD} = -5$ V, $T_A = 125°C$, $V_{SD} = 10$ V	0.5		5		5			µA
		$V_{GD} = -5$ V, $T_A = 125°C$, $V_{SD} = 20$ V	1						5	
Gate Leakage	I_{GSS}	$V_{DS} = V_{SB} = 0$ V, $V_{GS} = 12$ V			100		100		100	nA
		$T_A = 125°C$			1		1		1	µA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30$ V, $V_{GS} = V_{BS} = 0$ V			10					
Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS} = V_{GS(th)}$, $I_S = 1\,\mu A$, $V_{SB} = 0$ V	0.7	0.5	2.0	0.1	2.0	0.1	2.0	V
Drain-Source On-Resistance	$r_{DS(ON)}$	$V_{GS} = 5$ V, $I_D = 1$ mA	58		70		70		70	Ω
DYNAMIC										
Forward Transconductance[3]	g_{fs}	$V_{DS} = 10$ V, $V_{SB} = 0$ V, $I_D = 20$ mA, f = 1 kHz	11							mS
Output Conductance[3]	g_{os}		0.9							
Gate Node Capacitance	C_{iss}	$V_{DS} = 10$ V, f = 1 MHz, $V_{GS} = V_{BS} = -15$ V	2.5		3.5		3.5		3.5	pF
Reverse Transfer Capacitance	C_{rss}		0.2		0.5		0.5		0.5	
SWITCHING										
Turn-ON Time	$t_{d(ON)}$	$V_{DD} = 5$ V, $R_L = 680\,\Omega$, $V_{IN} = 5$ V, $R_G = 50\,\Omega$	0.5		1		1		1	ns
	t_r		0.6		1		1		1	
Turn-OFF Time [3]	$t_{d(OFF)}$		2							
	t_f		6							

NOTES: 1. $T_A = 25°C$ unless otherwise noted.
2. For design aid only, not subject to production testing.
3. This parameter not registered with JEDEC.

5

2N7105 SERIES

Siliconix incorporated

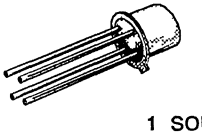
N-Channel Lateral DMOS FETs

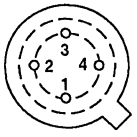
The 2N7105 Series of single-pole, single-throw analog switches is designed for high speed switching in audio, video, and high-frequency applications. These devices are designed on the Siliconix DMOS process and utilize lateral construction to achieve low capacitance and ultra-fast switching speeds. This series also feature an integrated Zener diode designed to protect the gate from electrical "spikes" or overstress.

For additional design information please see performance curves DMCB, which are located in Section 7.

PART NUMBER	$V_{(BR)DS}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	C_{rss} MAX (pF)	t_{ON} MAX (ns)
2N7105	10	70	0.5	2
2N7107	10	70	0.5	2
2N7109	20	70	0.5	2

TO-72 BOTTOM VIEW





1 SOURCE
2 DRAIN
3 GATE
4 SUBSTRATE, CASE

SIMILAR PRODUCTS

- Quad Array, See 2N7116 Series
- SO-14 Array, See SD5400 Series
- SOT-143, See SST211 Series
- Chips, Order 2N710XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT			UNITS
		2N7105	2N7107	2N7109	
Gate-Source, Gate-Drain Voltage	V_{GS},V_{GD}	-30/25	-15/25	-25/30	V
Gate-Substrate Voltage [1]	V_{GB}	-0.3/25	-0.3/25	-0.3/30	
Drain-Source Voltage	V_{DS}	30	10	20	
Source-Drain Voltage	V_{SD}	10	10	20	
Drain-Substrate Voltage	V_{DB}	30	15	25	
Source-Substrate Voltage	V_{SB}	15	15	25	
Drain Current	I_D	50	50	50	mA
Power Dissipation (T_J = 25°C)	P_D	300	300	300	mW
Power Derating		2.4	2.4	2.4	mW/°C
Operating Junction Temperature	T_J	-55 to 150			°C
Storage Temperature	T_{stg}	-65 to 200			
Lead Temperature (1/16" from case for 10 seconds)	T_L	300			

[1]These devices feature an internal Zener protected gate.

ELECTRICAL CHARACTERISTICS [1]				LIMITS							
					2N7105		2N7107		2N7109		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC											
Drain-Source Breakdown Voltage[3]	$V_{(BR)DS}$	$V_{GS} = V_{BS} = 0$ V, $I_D = 10\,\mu A$		35	30						V
		$V_{GS} = V_{BS} = -5$ V, $I_S = 10$ nA		30	10		10		20		
Source-Drain Breakdown Voltage[3]	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5$ V, $I_D = 10$ nA		22	10		10		20		
Drain-Substrate Breakdown Voltage[3]	$V_{(BR)DB}$	$V_{GB} = 0$ V, $I_D = 10$ nA Source OPEN		35	15		15		25		
Source-Substrate Breakdown Voltage[3]	$V_{(BR)SB}$	$V_{GB} = 0$ V, $I_S = 10\,\mu A$ Drain OPEN		35	15		15		25		
Drain-Source Leakage	$I_{DS(OFF)}$	$V_{GS} = V_{BS} = -5$ V	$V_{DS} = 10$ V	0.4		10		10			nA
			$V_{DS} = 20$ V	0.9						10	
		$V_{GS} = V_{BS} = -5$ V, $T_A = 125°C$	$V_{DS} = 10$ V	0.4		5		5			µA
			$V_{DS} = 20$ V	0.9						5	
Source-Drain Leakage	$I_{SD(OFF)}$	$V_{GD} = V_{BD} = -5$ V	$V_{SD} = 10$ V	0.5		10		10			nA
			$V_{SD} = 20$ V	1						10	
		$V_{GD} = -5$ V, $T_A = 125°C$	$V_{SD} = 10$ V	0.5		5		5			µA
			$V_{SD} = 20$ V	1						5	
Gate Leakage	I_{GSS}	$V_{DS} = V_{SB} = 0$ V	$V_{GS} = 25$ V			1		1			
			$V_{GS} = 30$ V							1	
		$V_{DS} = V_{SB} = 0$ V, $T_A = 125°C$	$V_{GS} = 25$ V			100		100			
			$V_{GS} = 30$ V							100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30$ V, $V_{GS} = V_{BS} = 0$ V				10					
Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS} = V_{GS(th)}$, $I_S = 1\,\mu A$, $V_{SB} = 0$ V		0.7	0.5	2	0.1	2	0.1	2	V
Drain-Source On-Resistance	$r_{DS(ON)}$	$V_{GS} = 5$ V, $I_D = 1$ mA		58		70		70		70	Ω
DYNAMIC											
Forward Transconductance[3]	g_{fs}	$V_{DS} = 10$ V, $V_{SB} = 0$ V, $I_D = 20$ mA, $f = 1$ kHz		11							mS
Output Conductance[3]	g_{os}			0.9							
Gate Node Capacitance	C_{iss}	$V_{DS} = 10$ V, $f = 1$ MHz, $V_{GS} = V_{BS} = -15$ V		2.5		3.5		3.5		3.5	pF
Reverse Transfer Capacitance	C_{rss}			0.2		0.5		0.5		0.5	
SWITCHING											
Turn-ON Time	$t_{d(ON)}$	$V_{DD} = 5$ V, $R_L = 680\ \Omega$, $V_{IN} = 5$ V, $R_G = 50\ \Omega$		0.5		1		1		1	ns
	t_r			0.6		1		1		1	
Turn-OFF Time [3]	$t_{d(OFF)}$			2							
	t_f			6							

NOTES: 1. $T_A = 25°C$ unless otherwise noted.
2. For design aid only, not subject to production testing.
3. This parameter not registered with JEDEC.

5

2N7116 SERIES

Siliconix incorporated

N-Channel Lateral DMOS Quad FETs

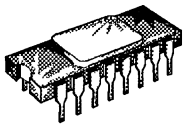
The Siliconix 2N7116 series is a monolithic array of single-pole, single-throw analog switches designed for high speed switching in audio, video and high frequency applications in communications, instrumentation, and process control. Designed on the Siliconix DMOS process, the 2N7116 is rated for analog signals of ±10 V, while the 2N7117 and 2N7118 are rated for ±5 V and ±7.5 V respectively.

These bidirectional switches feature very low interelectrode capacitance and on-resistance to achieve low insertion loss, crosstalk, and feedthrough performance. The threshold voltage for all switches is 2 V maximum, simplifying driver requirements for low level signal applications.

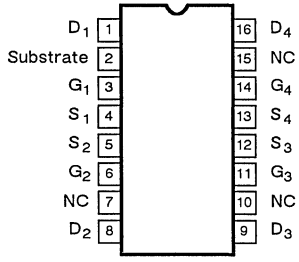
For additional design information please see performance curves DMCA-1B, which are located in Section 7.

PART NUMBER	$V_{(BR)DS}$ MIN (V)	$V_{GS(th)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	t_{ON} MAX (ns)
2N7116	20	2.0	70	2
2N7117	10	2.0	70	2
2N7118	15	2.0	70	2

16-PIN DIP
SIDE BRAZE QUAD



TOP VIEW



SIMILAR PRODUCTS

- SOT-143, See SST211 Series
- TO-18, See SD211DE Series
- SO-14, See SD5400 Series
- Chips, Order 2N711XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMIT 2N7116	LIMIT 2N7117	LIMIT 2N7118	UNITS
Gate-Source, Gate-Drain Voltage		V_{GS}, V_{GD}	25/–25	25/–15	30/–22.5	V
Drain-Substrate, Source-Substrate Voltage		V_{DB}, V_{SB}	25	15	22.5	V
Drain-Source, Source-Drain Voltage		V_{DS}, V_{SD}	20	10	15	V
Gate-Substrate Voltage [1]		V_{GB}	30/–0.3	25/–0.3	30/–0.3	V
Drain Current		I_D	50			mA
Power Dissipation	Package	P_D	640			mW
	Each Device		300			mW
Power Derating (Package)			5			mW/°C
Operating Junction Temperature		T_J	–55 to 125			°C
Storage Temperature		T_{stg}	–55 to 150			°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300			°C

[1]These devices feature an internal Zener procted gate.

ELECTRICAL CHARACTERISTICS [1]				LIMITS							
					2N7116		2N7117		2N7118		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC											
Drain-Source Breakdown Voltage[3]	$V_{(BR)DS}$	$V_{GS} = V_{BS} = 0$ V, $I_D = 10\,\mu A$		35	30						V
		$V_{GS} = V_{BS} = -5$ V, $I_S = 10$ nA		30	10		10		20		
Source-Drain Breakdown Voltage[3]	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5$ V, $I_D = 10$ nA		22	10		10		20		
Drain-Substrate Breakdown Voltage[3]	$V_{(BR)DB}$	$V_{GB} = 0$ V, $I_D = 10$ nA	Source OPEN	35	15		15		25		
Source-Substrate Breakdown Voltage[3]	$V_{(BR)SB}$	$V_{GB} = 0$ V, $I_S = 10\,\mu A$	Drain OPEN	35	15		15		25		
Drain-Source Leakage	$I_{DS(OFF)}$	$V_{GS} = V_{BS} = -5$ V	$V_{DS} = 10$ V	0.4				10			nA
			$V_{DS} = 15$ V	0.7						10	
			$V_{DS} = 20$ V	0.9		10					
		$V_{GS} = V_{BS} = -5$ V, $T_A = 125°C$	$V_{DS} = 10$ V	0.4				5			µA
			$V_{DS} = 15$ V	0.7						5	
			$V_{DS} = 20$ V	0.9		5					
Source-Drain Leakage	$I_{SD(OFF)}$	$V_{GD} = V_{BD} = -5$ V	$V_{SD} = 10$ V	0.5				10			nA
			$V_{SD} = 15$ V	0.7						10	
			$V_{SD} = 20$ V	1		10					
		$V_{GD} = V_{BD} = -5$ V, $T_A = 125°C$	$V_{SD} = 10$ V	0.5				5			µA
			$V_{SD} = 15$ V	0.7						5	
			$V_{SD} = 20$ V	1		5					
Gate Leakage	I_{GSS}	$V_{DS} = V_{SB} = 0$ V	$V_{GS} = 25$ V					1			
			$V_{GS} = 30$ V			1				1	
		$V_{DS} = V_{SB} = 0$ V, $T_A = 125°C$	$V_{GS} = 25$ V					10			
			$V_{GS} = 30$ V			10				10	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30$ V, $V_{GS} = V_{BS} = 0$ V				10					
Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS} = V_{GS(th)}$, $I_D = 1\,\mu A$, $V_{SB} = 0$ V		0.7	0.1	2	0.1	2	0.1	2	V
Drain-Source On-Resistance	$r_{DS(ON)}$	$V_{GS} = 5$ V, $I_D = 1$ mA, $V_{BS} = 0$ V		58		70		70		70	Ω
DYNAMIC											
Forward Transconductance[3]	g_{fs}	$V_{DS} = 10$ V, $V_{SB} = 0$ V, $I_D = 20$ mA, f = 1 kHz		11							mS
Output Conductance[3]	g_{os}			0.9							
Gate Node Capacitance	C_{iss}	$V_{DS} = 10$ V, f = 1 MHz, $V_{GS} = V_{BS} = -15$ V		2.5		3.5		3.5		3.5	pF
Reverse Transfer Capacitance	C_{rss}			0.2		0.5		0.5		0.5	
SWITCHING											
Turn-ON Time	$t_{d(ON)}$	$V_{DD} = 5$ V, $R_L = 680\,\Omega$, $V_{IN} = 5$ V, $R_G = 50\,\Omega$		0.5		1		1		1	ns
	t_r			0.6		1		1		1	
Turn-OFF Time [3]	$t_{d(OFF)}$			2							
	t_f			6							

NOTES: 1. $T_A = 25°C$ unless otherwise noted.
2. For design aid only, not subject to production testing.
3. This parameter not registered with JEDEC.

5

SD210DE SERIES

Siliconix incorporated

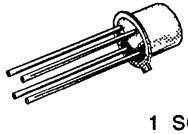
N-Channel Lateral DMOS FETs

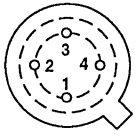
The SD210DE Series of single-pole, single-throw analog switches is designed for high speed switching in audio, video, and high-frequency applications. These devices are designed on the Siliconix DMOS process and utilize lateral construction to achieve low capacitance and ultra-fast switching speeds. For long term reliability, this series also features a poly-silicon gate.

For additional design information please see performance curves DMCB, which are located in Section 7.

PART NUMBER	$V_{(BR)DS}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	C_{rss} MAX (pF)	t_{ON} MAX (ns)
SD210DE	20	45	0.5	2
SD212DE	10	45	0.5	2
SD214DE	15	45	0.5	2

TO-72 BOTTOM VIEW





1 SOURCE
2 DRAIN
3 GATE
4 SUBSTRATE, CASE

SIMILAR PRODUCTS

- Quad Array, See SD5000 Series
- SO-14 Array, See SD5400 Series
- Zener Protection, See SD211DE Series
- SOT-143, See SST211 Series
- Chips, Order SD21XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT			UNITS
		SD210DE	SD212DE	SD214DE	
Gate-Source, Gate-Drain Gate-Substrate Voltage	V_{GS},V_{GD},V_{GB}	±40	±40	±40	V
Drain-Source Voltage	V_{DS}	30	10	20	
Source-Drain Voltage	V_{SD}	10	10	20	
Drain-Substrate Voltage	V_{DB}	30	15	25	
Source-Substrate Voltage	V_{SB}	15	15	25	
Drain Current	I_D	50	50	50	mA
Power Dissipation (25°C Case)	P_D	1200	1200	1200	mW
Power Derating		9.6	9.6	9.6	mW/°C
Operating Junction Temperature	T_J	-55 to 150			°C
Storage Temperature	T_{stg}	-65 to 200			
Lead Temperature (1/16" from case for 10 seconds)	T_L	300			

ELECTRICAL CHARACTERISTICS [1]				LIMITS							
					SD210DE		SD212DE		SD214DE		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC											
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = V_{BS} = 0$ V, $I_D = 10\,\mu$A		35	30						V
		$V_{GS} = V_{BS} = -5$ V, $I_S = 10$ nA		30	10		10		20		
Source-Drain Breakdown Voltage	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5$ V, $I_D = 10$ nA		22	10		10		20		
Drain-Substrate Breakdown Voltage	$V_{(BR)DB}$	$V_{GB} = 0$ V, $I_D = 10$ nA, Source OPEN		35	15		15		25		
Source-Substrate Breakdown Voltage	$V_{(BR)SB}$	$V_{GB} = 0$ V, $I_S = 10\,\mu$A, Drain OPEN		35	15		15		25		
Drain-Source Leakage	$I_{DS(OFF)}$	$V_{GS} = V_{BS} = -5$ V	$V_{DS} = 10$ V	0.4		10		10			nA
			$V_{DS} = 20$ V	0.9						10	
Source-Drain Leakage	$I_{SD(OFF)}$	$V_{GD} = V_{BD} = -5$ V	$V_{SD} = 10$ V	0.5		10		10			
			$V_{SD} = 20$ V	1						10	
Gate Leakage	I_{GBS}	$V_{DB} = V_{SB} = 0$ V, $V_{GB} = \pm 40$ V		0.001		0.1		0.1		0.1	
Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS} = V_{GS(th)}$, $I_S = 1\,\mu$A, $V_{SB} = 0$ V		0.7	0.5	2	0.1	2	0.1	2	V
Drain-Source On-Resistance	$r_{DS(ON)}$	$I_D = 1$ mA, $V_{SB} = 0$ V	$V_{GS} = 5$ V	58		70		70		70	Ω
			$V_{GS} = 10$ V	38		45		45		45	
			$V_{GS} = 15$ V	30							
			$V_{GS} = 20$ V	26							
			$V_{GS} = 25$ V	24							
DYNAMIC											
Forward Transconductance	g_{fs}	$V_{DS} = 10$ V, $V_{SB} = 0$ V, $I_D = 20$ mA, $f = 1$ kHz		11	10		10		10		mS
Output Conductance	g_{os}			0.9							
Gate Node Capacitance	$C_{(GS+GD+GB)}$	$V_{DS} = 10$ V, $f = 1$ MHz, $V_{GS} = V_{BS} = -15$ V		2.5		3.5		3.5		3.5	pF
Drain Node Capacitance	$C_{(GD+DB)}$			1.1		1.5		1.5		1.5	
Source Node Capacitance	$C_{(GS+SB)}$			3.7		5.5		5.5		5.5	
Reverse Transfer Capacitance	C_{rss}			0.2		0.5		0.5		0.5	
SWITCHING											
Turn-ON Time	$t_{d(ON)}$	$V_{DD} = 5$ V, $R_L = 680\ \Omega$, $V_{IN} = 0$ to 5 V		0.5		1		1		1	ns
	t_r			0.6		1		1		1	
Turn-OFF Time	$t_{d(OFF)}$			2							
	t_f			6							

NOTES: 1. $T_A = 25$ °C unless otherwise noted.
2. For design aid only, not subject to production testing.

5

SD211DE SERIES

Siliconix incorporated

N-Channel Lateral DMOS FETs

The SD211DE Series of single-pole, single-throw analog switches is designed for high speed switching in audio, video, and high-frequency applications. These devices are designed on the Siliconix DMOS process and utilize lateral construction to achieve low capacitance and ultra-fast switching speeds. This series also features an integrated zener diode designed to protect the gate from electrical "Spikes" or overstress.

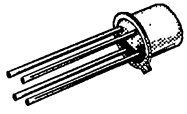
For additional design information please see performance curves DMCB, which are located in Section 7.

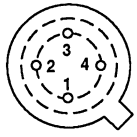
PART NUMBER	$V_{(BR)DS}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	C_{rss} MAX (pF)	t_{ON} MAX (ns)
SD211DE	10	45	0.5	2
SD213DE	10	45	0.5	2
SD215DE	20	45	0.5	2

SIMILAR PRODUCTS

- Quad Array, See SD5000 Series
- SO-14 Array, See SD5400 Series
- SOT-143, See SST211 Series
- Chips Order, SD21XCHP

TO-72 **BOTTOM VIEW**





1 SOURCE
2 DRAIN
3 GATE
4 SUBSTRATE, CASE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT			UNITS
		SD211DE	SD213DE	SD215DE	
Gate-Source, Gate-Drain Voltage	V_{GS},V_{GD}	-30/25	-15/25	-25/30	V
Gate-Substrate Voltage	V_{GB}[1]	-0.3/25	-0.3/25	-0.3/30	
Drain-Source Voltage	V_{DS}	30	10	20	
Source-Drain Voltage	V_{SD}	10	10	20	
Drain-Substrate Voltage	V_{DB}	30	15	25	
Source-Substrate Voltage	V_{SB}	15	15	25	
Drain Current	I_D	50	50	50	mA
Power Dissipation (25°C Case)	P_D	1200	1200	1200	mW
Power Derating		9.6	9.6	9.6	mW/°C
Operating Junction Temperature	T_J	-55 to 150			°C
Storage Temperature	T_{stg}	-65 to 200			
Lead Temperature (1/16" from case for 10 seconds)	T_L	300			

[1] This series features an internal zener diode for gate protection

ELECTRICAL CHARACTERISTICS [1]				LIMITS							
					SD211DE		SD213DE		SD215DE		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC											
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = V_{BS} = 0$ V, $I_D = 10\,\mu$A		35	30						V
		$V_{GS} = V_{BS} = -5$ V, $I_S = 10$ nA		30	10		10		20		
Source-Drain Breakdown Voltage	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5$ V, $I_D = 10$ nA		22	10		10		20		
Drain-Substrate Breakdown Voltage	$V_{(BR)DB}$	$V_{GB} = 0$ V, $I_D = 10$ nA, Source OPEN		35	15		15		25		
Source-Substrate Breakdown Voltage	$V_{(BR)SB}$	$V_{GB} = 0$ V, $I_S = 10\,\mu$A, Drain OPEN		35	15		15		25		
Drain-Source Leakage Current	$I_{DS(OFF)}$	$V_{GS} = V_{BS} = -5$ V	$V_{DS} = 10$ V	0.4		10		10			nA
			$V_{DS} = 20$ V	0.9						10	
Source-Drain Leakage Current	$I_{SD(OFF)}$	$V_{GD} = V_{BD} = -5$ V	$V_{SD} = 10$ V	0.5		10		10			
			$V_{SD} = 20$ V	1						10	
Gate Leakage Current	I_{GBS}	$V_{DB} = V_{SB} = 0$ V, $V_{GB} = 30$ V		10^{-5}		10		10		10	μA
Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS} = V_{GS(th)}$, $I_S = 1\,\mu$A, $V_{SB} = 0$ V		0.7	0.5	2	0.1	2	0.1	2	V
Drain-Source On-Resistance	$r_{DS(ON)}$	$I_D = 1$ mA, $V_{SB} = 0$ V	$V_{GS} = 5$ V	58		70		70		70	Ω
			$V_{GS} = 10$ V	38		45		45		45	
			$V_{GS} = 15$ V	30							
			$V_{GS} = 20$ V	26							
			$V_{GS} = 25$ V	24							
DYNAMIC											
Forward Transconductance	g_{fs}	$V_{DS} = 10$ V, $V_{SB} = 0$ V, $I_D = 20$ mA, f = 1 kHz		11	10		10		10		mS
Output Conductance	g_{os}			0.9							
Gate Node Capacitance	$C_{(GS+GD+GB)}$	$V_{DS} = 10$ V, f = 1 MHz, $V_{GS} = V_{BS} = -15$ V		2.5		3.5		3.5		3.5	pF
Drain Node Capacitance	$C_{(GD+DB)}$			1.1		1.5		1.5		1.5	
Source Node Capacitance	$C_{(GS+SB)}$			3.7		5.5		5.5		5.5	
Reverse Transfer Capacitance	C_{rss}			0.2		0.5		0.5		0.5	
SWITCHING											
Turn-ON Time	$t_{d(ON)}$	$V_{DD} = 5$ V, $R_L = 680\,\Omega$, $V_{IN} = 0$ to 5 V		0.5		1		1		1	ns
	t_r			0.6		1		1		1	
Turn-OFF Time	$t_{d(OFF)}$			2							
	t_f			6							

NOTES: 1. $T_A = 25$ °C unless otherwise noted.
2. For design aid only, not subject to production testing.

5

SD/SST2100 SERIES

Siliconix incorporated

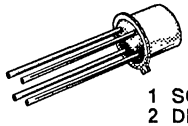
N-Channel Depletion-Mode Lateral DMOS FETs

The SD/SST2100 Series is a depletion-mode MOSFET which utilizes our lateral DMOS process to provide low capacitance, fast switching, and high operating frequency. This DMOS process effectively bridges the operating frequency gap between JFETs and costly gallium-arsenide devices. Additionally, this series is available in both a TO-72 hermetically sealed can as well as the SOT-143 package for commercial applications.

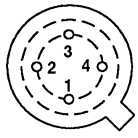
For additional design information please see performance curves DMCD, which are located in Section 7. Application hints can be found in LPD-12 (See Section 9).

PART NUMBER	$V_{(BR)DS}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	C_{rss} MAX (pF)	t_{ON} TYP (ns)
SD2100	15	50	2	1.1
SST2100	15	50	2	1.1

TO-72



BOTTOM VIEW

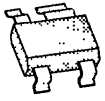


1 SOURCE
2 DRAIN
3 GATE
4 SUBSTRATE

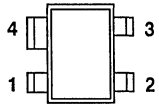
SIMILAR PRODUCTS

- Chips, Order SD2100CHP

SOT-143



TOP VIEW



1 GATE
2 DRAIN
3 SOURCE
4 SUBSTRATE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT		UNITS
		SD2100	SST2100	
Gate-Source Voltage	V_{GS}	± 25	± 25	V
Drain-Source Voltage	V_{DS}	25	25	
Drain Current	I_D	50	50	mA
Power Dissipation (T_A = 25°C)	P_D	350	350	mW
Power Derating		2.8	2.8	mW/°C
Operating Junction Temperature	T_J	-55 to 150		°C
Storage Temperature	T_{stg}	-55 to 150		
Lead Temperature (1/16" from case for 10 seconds)	T_L	300		

ELECTRICAL CHARACTERISTICS [1]				LIMITS			
					SD/SST2100		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP [2]	MIN	MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = V_{BS} = -5$ V, $I_D = 1$ µA		25	15		V
Gate Reverse Current	I_{GSS}	$V_{GS} = \pm 25$ V, $V_{DS} = V_{BS} = 0$ V		± 0.05		± 1	nA
Saturation Drain Current	I_{DSS}	$V_{DS} = 10$ V, $V_{GS} = V_{BS} = 0$ V		7	0.5	10	mA
Gate-Source Cutoff	$V_{GS(OFF)}$	$V_{DS} = 10$ V, $I_D = 1$µA $V_{BS} = 0$ V		-1.5		-2	V
Gate-Source Voltage	V_{GS}	$V_{DG} = 10$ V $V_{BS} = 0$ V	$I_D = 5$ mA	-0.3	-1	1	V
			$I_D = 10$ mA	0.4	0	1.5	
Drain-Source On-Resistance	$r_{DS(ON)}$	$I_D = 100$ µA $V_{BS} = 0$ V	$V_{GS} = 0$ V	120		200	Ω
			$V_{GS} = 5$ V	40		50	
DYNAMIC							
Forward Transconductance	g_{fs}	$V_{DS} = 10$ V, $V_{GS} = V_{BS} = 0$ V $f = 1$ kHz		8000	1000		µS
Output Conductance	g_{os}			250		500	
Forward Transconductance	g_{fs}	$V_{DG} = 10$ V, $V_{BS} = 0$ V $I_D = 10$ mA, $f = 1$ kHz		10000	7000		
Output Conductance	g_{os}			350		500	
Common-Source Input Capacitance	C_{iss}	$V_{DS} = 10$ V, $f = 1$ MHz $V_{GS} = V_{BS} = -5$ V		5		6	pF
Reverse Transfer Capacitance	C_{rss}			1		2	
SWITCHING							
Turn-ON Time	$t_{d(ON)}$	$V_{DD} = 5$ V, $R_L = 680$ Ω $V_{IN} = -4$ V to -2 V		0.7			ns
	t_r			0.4			
Turn-OFF Time	t_{OFF}			5			

NOTES: 1. $T_A = 25$ °C unless otherwise noted.
2. For design aid only, not subject to production testing.

5

SD5000 SERIES

Siliconix incorporated

N-Channel Lateral DMOS Quad FETs

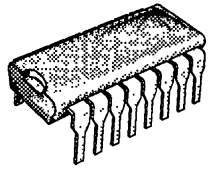
The Siliconix SD5000 Series is a monolithic array of single-pole, single-throw analog switches designed for high speed switching in audio, video and high-frequency applications in communications, instrumentation, and process control. Designed on the Siliconix DMOS process, the SD5000 is rated for analog signals of ±10 V, while the SD5001 and SD5002 are rated for ±5 V and ±7.5 V respectively.

These bidirectional switches feature very low interelectrode capacitance and on-resistance to achieve low insertion loss, crosstalk, and feedthrough performance. The threshold voltage for all switches is 2 V maximum, simplifying driver requirements for low level signal applications.

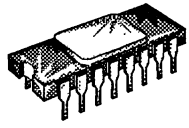
For additional design information please see performance curves DMCA-1B, which are located in Section 7.

PART NUMBER	PACKAGE	$V_{GS(TH)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	t_{ON} MAX (ns)
SD5000N	PLASTIC	2.0	70	2
SD5001N	PLASTIC	2.0	70	2
SD5002N	PLASTIC	2.0	70	2
SD5000I	CERAMIC	2.0	70	2
SD5001I	CERAMIC	2.0	70	2
SD5002I	CERAMIC	2.0	70	2

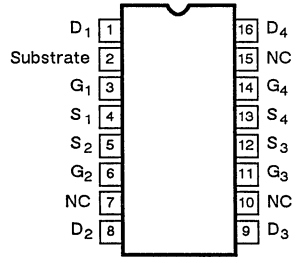
16-PIN DIP QUAD PLASTIC



16-PIN DIP SIDE BRAZE QUAD



TOP VIEW



SIMILAR PRODUCTS

- SO-14, See SD5400 Series
- TO-18, See SD211DE Series
- SOT-143, See SST211 Series
- Chips, Order SD500XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMIT			UNITS
			SD5000	SD5001	SD5002	
Gate-Source, Gate-Drain Voltage		V_{GS}, V_{GD}	30/–25	25/–15	30/–22.5	V
Drain-Substrate, Source-Substrate Voltage		V_{DB}, V_{SB}	25	15	22.5	
Drain-Source, Source-Drain Voltage		V_{DS}, V_{SD}	20	10	15	
Gate-Substrate Voltage [1]		V_{GB}	30/–0.3	25/–0.3	30/–0.3	
Drain Current		I_D	50			mA
Power Dissipation	Package	P_D	640			mW
	Each Device		300			
Power Derating (Package)			5.12			mW/°C
Operating Junction Temperature		T_J	–55 to 125			°C
Storage Temperature		T_{stg}	–65 to 150			
Lead Temperature (1/16" from case for 10 seconds)		T_L	300			

[1] These devices feature an internal zener protected gate.

ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				SD5000		SD5001		SD5002		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = V_{BS} = -5$ V, $I_D = 10$ nA	30	20		10		15		V
Source-Drain Breakdown Voltage	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5$ V, $I_S = 10$ nA	22	20		10		15		V
Drain-Substrate Breakdown Voltage	$V_{(BR)DB}$	$V_{GB} = 0$ V, $I_D = 10$ nA, Source OPEN	35	25		15		22.5		V
Source-Substrate Breakdown Voltage	$V_{(BR)SB}$	$V_{GB} = 0$ V, $I_S = 10\,\mu$A, Drain OPEN	35	25		15		22.5		V
Drain-Source Leakage	$I_{DS(OFF)}$	$V_{GS} = V_{BS} = -5$ V, $V_{DS} = 20$ V	0.9		10					nA
		$V_{DS} = 10$ V	0.4				10			nA
		$V_{DS} = 15$ V	0.7						10	nA
Source-Drain Leakage	$I_{SD(OFF)}$	$V_{GD} = V_{BD} = -5$ V, $V_{SD} = 20$ V	1		10					nA
		$V_{SD} = 10$ V	0.5				10			nA
		$V_{SD} = 15$ V	0.8						10	nA
Gate Leakage	I_{GBS}	$V_{DB} = V_{SB} = 0$ V, $V_{GB} = 30$ V	10^{-5}		1		1		1	μA
Threshold Voltage	$V_{GS}(th)$	$V_{DS} = V_{GS} = V_{GS(th)}$, $I_S = 1\,\mu$A, $V_{SB} = 0$ V	0.7	0.1	2.0	0.1	2.0	0.1	2.0	V
Drain-Source On-Resistance	$r_{DS(ON)}$	$I_D = 1$ mA, $V_{SB} = 0$ V, $V_{GS} = 5$ V	58		70		70		70	Ω
		$V_{GS} = 10$ V	38							Ω
		$V_{GS} = 15$ V	30							Ω
		$V_{GS} = 20$ V	26							Ω
Resistance Match		$I_D = 1$ mA, $V_{SB} = 0$ V, $V_{GS} = 5$ V	1		5		5		5	Ω
DYNAMIC										
Forward Transconductance	g_{fs}	$V_{DS} = 10$ V, $V_{SB} = 0$ V, $I_D = 20$ mA, $f = 1$ kHz	11	10		10		10		mS
Gate Node Capacitance	$C_{(GS+GD+GB)}$	$V_{DS} = 10$ V, $f = 1$ MHz, $V_{GS} = V_{BS} = -15$ V	2.5		3.5		3.5		3.5	pF
Drain Node Capacitance	$C_{(GD+DB)}$		1.1		1.6		1.6		1.6	pF
Source Node Capacitance	$C_{(GS+SB)}$		3.7		5		5		5	pF
Reverse Transfer Capacitance	C_{rss}		0.2		0.5		0.5		0.5	pF
Crosstalk		f = 3 kHz, See Test Circuits in DMCA Performance Curves	-107							dB
SWITCHING										
Turn-ON Time	$t_{d(ON)}$	$V_{DD} = 5$ V, $R_L = 680\ \Omega$, $V_{IN} = 5$ V	0.5		1		1		1	ns
	t_r		0.6		1		1		1	ns
Turn-OFF Time	$t_{d(OFF)}$		2							ns
	t_f		6							ns

NOTES: 1. $T_A = 25$ °C unless otherwise noted.
2. For design aid only, not subject to production testing.

5

SD5400 SERIES

Siliconix incorporated

N-Channel Lateral DMOS Quad FETs

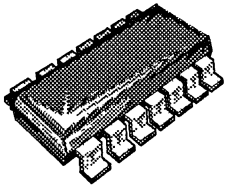
The Siliconix SD5400 series is a monolithic array of single-pole, single-throw analog switches designed for high-speed switching in audio, video and high frequency applications in communications, instrumentation, and process control. Designed with the Siliconix DMOS process, the SD5400 is rated for analog signals of ±10 V, while the SD5401 and SD5402 are rated for ±5 V and ±7.5 V respectively.

These bidirectional switches feature very low interelectrode capacitance and on-resistance to achieve low insertion loss, crosstalk, and feedthrough performance. The threshold voltage for all switches is 2 V maximum, simplifying driver requirements for low level signal applications.

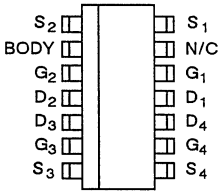
For additional design information please see performance curves DMCA, which are located in Section 7.

PART NUMBER	$V_{(BR)DS}$ MIN (V)	$V_{GS(TH)}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	t_{ON} MAX (ns)
SD5400CY	20	2.0	70	2
SD5401CY	10	2.0	70	2
SD5402CY	15	2.0	70	2

SO-14



TOP VIEW



SIMILAR PRODUCTS

- TO-18, See SD211DE Series
- 16-Pin DIP, See SD5000 Series
- SOT-143, See SST211 Series
- Chips, Order SD540XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMIT			UNITS
			SD5400	SD5401	SD5402	
Gate-Source, Gate-Drain Voltage		V_{GS}, V_{GD}	30/–25	25/–15	30/–22.5	V
Drain-Substrate, Source-Substrate Voltage		V_{DB}, V_{SB}	25	15	22.5	
Drain-Source, Source-Drain Voltage		V_{DS}, V_{SD}	20	10	15	
Gate-Substrate Voltage [1]		V_{GB}	30/–0.3	25/–0.3	30/–0.3	
Drain Current		I_D	50			mA
Power Dissipation	Package	P_D	500			mW
	Each Device		300			
Power Derating (Package)			5			mW/°C
Operating Junction Temperature		T_J	–55 to 125			°C
Storage Temperature		T_{stg}	–55 to 125			
Lead Temperature (1/16" from case for 10 seconds)		T_L	300			

[1] These devices feature an internal Zener protected gate.

ELECTRICAL CHARACTERISTICS [1]			LIMITS							
				SD5400CY		SD5401CY		SD5402CY		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = V_{BS} = -5$ V, $I_D = 10$ nA	30	20		10		15		V
Source-Drain Breakdown Voltage	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5$ V, $I_S = 10$ nA	22	20		10		15		V
Drain-Substrate Breakdown Voltage	$V_{(BR)DB}$	$V_{GB} = 0$ V, $I_D = 10$ nA, Source OPEN	35	25		15		22.5		V
Source-Substrate Breakdown Voltage	$V_{(BR)SB}$	$V_{GB} = 0$ V, $I_S = 10$ µA, Drain OPEN	35	25		15		22.5		V
Drain-Source Leakage	$I_{DS(OFF)}$	$V_{GS} = V_{BS} = -5$ V, $V_{DS} = 20$ V	0.9		10					nA
		$V_{DS} = 10$ V	0.4				10			nA
		$V_{DS} = 15$ V	0.7						10	nA
Source-Drain Leakage	$I_{SD(OFF)}$	$V_{GD} = V_{BD} = -5$ V, $V_{SD} = 20$ V	1		10					nA
		$V_{SD} = 10$ V	0.5				10			nA
		$V_{SD} = 15$ V	0.8						10	nA
Gate Leakage	I_{GBS}	$V_{DB} = V_{SB} = 0$ V, $V_{GB} = 30$ V	10^{-5}		1		1		1	µA
Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS} = V_{GS(th)}$, $I_S = 1$µA, $V_{SB} = 0$ V	0.7	0.1	2	0.1	2	0.1	2	V
Drain-Source On-Resistance	$r_{DS(ON)}$	$I_D = 1$ mA, $V_{SB} = 0$ V, $V_{GS} = 5$ V	58		70		70		70	Ω
		$V_{GS} = 10$ V	38							Ω
		$V_{GS} = 15$ V	30							Ω
		$V_{GS} = 20$ V	26							Ω
Resistance Match		$I_D = 1$ mA, $V_{SB} = 0$ V, $V_{GS} = 5$ V	1		5		5		5	Ω
DYNAMIC										
Forward Transconductance	g_{fs}	$V_{DS} = 10$ V, $V_{SB} = 0$ V, $I_D = 20$ mA, $f = 1$ kHz	11	10		10		10		mS
Gate Node Capacitance	$C_{(GS+GD+GB)}$	$V_{DS} = 10$ V, $f = 1$ MHz, $V_{GS} = V_{BS} = -15$ V	2.5		3.5		3.5		3.5	pF
Drain Node Capacitance	$C_{(GD+DB)}$		1.1		2		2		2	pF
Source Node Capacitance	$C_{(GS+SB)}$		3.7		6		6		6	pF
Reverse Transfer Capacitance	C_{rss}		0.2		0.5		0.5		0.5	pF
Crosstalk		f = 3 kHz, See Test Circuits in DMCA Performance Curves	-107							dB
SWITCHING										
Turn-ON Time	$t_{d(ON)}$	$V_{DD} = 5$ V, $R_L = 680$ Ω, $V_{IN} = 5$ V	0.5		1		1		1	ns
	t_r		0.6		1		1		1	ns
Turn-OFF Time	$t_{d(OFF)}$		2							ns
	t_f		6							ns

NOTES: 1. $T_A = 25$ °C unless otherwise noted.
2. For design aid only, not subject to production testing.

5

Si8901 SERIES

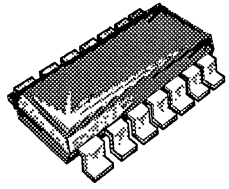
Siliconix incorporated

DMOS Double-Balanced Mixers

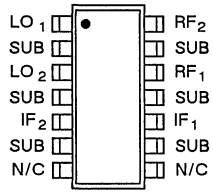
The Si8901 Ring Demodulator/Balanced Mixer offers significant improvements for RF mixer application where low third order harmonic distortion has been a problem. Combining matching with very low junction capacitance, (< 3 pF), low on-resistance (30 Ω) and very high off-resistance (> 10^9 Ω), the Si8901 accepts an RF and a local oscillator (LO) input and provides a high fidelity IF output with typical conversion loss of −8 dB at frequencies up to 200 MHz. Available in an 8-pin TO-78 and SO-14 package, this device is specified over −55 to 125°C temperature range.

PART NUMBER	PACKAGE	$V_{(BR)DS}$ MIN (V)	$V_{GS}(th)$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)
Si8901A	TO-78	15	2.0	70
Si8901CY	SO-14	15	2.0	70

SO-14



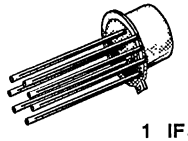
TOP VIEW



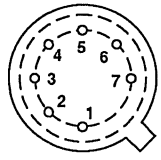
SIMILAR PRODUCTS

- Chips, order Si8901CHP

TO-78



BOTTOM VIEW



1 IF_1
2 RF_1
3 RF_2
4 SUB
5 LO_1
6 LO_2
7 IF_2

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT		UNITS
		Si8901A	Si8901CY	
Gate-Source, Gate-Drain Voltage	V_{GS}, V_{GD}	30/−22.5	30/−22.5	V
Drain-Substrate, Source-Substrate Voltage	V_{DB}, V_{SB}	22.5	22.5	
Drain-Source Voltage	V_{DS}	15	15	
Gate-Substrate Voltage [1]	V_{GB}	30/−0.3	30/−0.3	
Drain Current	I_D	50		mA
Power Dissipation (Package)	P_D	500		mW
Power Derating		5		mW/°C
Operating Junction Temperature	T_J	−55 to 125		°C
Storage Temperature	T_{stg}	−65 to 150		
Lead Temperature (1/16" from case for 10 seconds)	T_L	300		

[1] These devices feature an internal Zener protected gate.

ELECTRICAL CHARACTERISTICS [1]				LIMITS				
				Si8901A		Si8901CY		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = V_{BS} = -5$ V, $I_D = 10$ nA	30	15		15		V
Source-Drain Breakdown Voltage	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5$ V, $I_S = 10$ nA	22	15		15		V
Drain-Substrate Breakdown Voltage	$V_{(BR)DB}$	$V_{GB} = 0$ V, $I_D = 10$ nA, Source OPEN	35	22.5		22.5		V
Source-Substrate Breakdown Voltage	$V_{(BR)SB}$	$V_{GB} = 0$ V, $I_S = 10$ nA, Drain OPEN	35	22.5		22.5		V
Drain-Source Leakage	$I_{DS(OFF)}$	$V_{GS} = V_{BS} = -5$ V, $V_{DS} = 15$ V	0.7					nA
Source-Drain Leakage	$I_{SD(OFF)}$	$V_{GD} = V_{BD} = -5$ V, $V_{SD} = 15$ V	0.8					nA
Gate Leakage	I_{GBS}	$V_{DB} = V_{SB} = 0$ V, $V_{GB} = 30$ V	0.01		2		2	µA
Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS} = V_{GS(th)}$, $I_S = 1$µA, $V_{SB} = 0$ V	0.7	0.1	2	0.1	2	V
Drain-Source On-Resistance	$r_{DS(ON)}$	$I_D = 10$ mA, $V_{SB} = 0$ V, $V_{GS} = 5$ V	60		75		75	Ω
		$I_D = 10$ mA, $V_{SB} = 0$ V, $V_{GS} = 10$ V	40					Ω
		$I_D = 10$ mA, $V_{SB} = 0$ V, $V_{GS} = 15$ V	33					Ω
		$I_D = 10$ mA, $V_{SB} = 0$ V, $V_{GS} = 20$ V	29					Ω
Resistance Match		$I_D = 10$ mA, $V_{SB} = 0$ V, $V_{GS} = 5$ V	1		7		7	Ω
DYNAMIC								
$LO_1 - LO_2$ Capacitance	C_{gg}	$V_{DS} = 0$ V, $V_{BS} = -5.5$ V, $V_{GS} = 4$ V	4.4					pF
Conversion Loss	L_c	See Figure 1, $P_{LO} = +17$ dBm	8					dB
Third Order Intercept	IMD_3	See Figure 1, $P_{LO} = +17$ dBm	35					dB
Maximum Operation Frequency	f_{MAX}		250					MHz

NOTES: 1. $T_A = 25$ °C unless otherwise noted.
2. For design aid only, not subject to production testing.

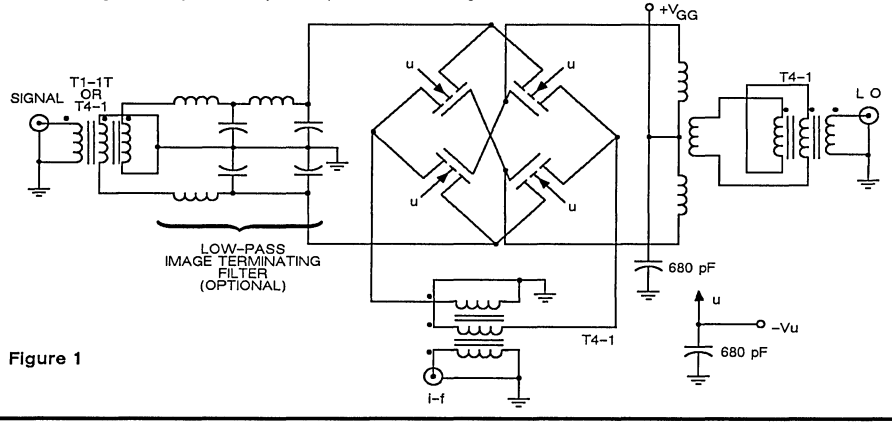


Figure 1

5

SST211 SERIES

Siliconix incorporated

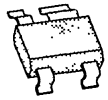
N-Channel Lateral DMOS FETs

The SST211 Series is a single-pole, single-throw analog switch designed for high speed switching in audio, video, and high-frequency applications. These devices are designed on the Siliconix DMOS process and utilize lateral construction to achieve low capacitance and ultra-fast switching speeds. These devices also feature an integrated Zener diode designed to protect the gate from electrical "spikes" or overstress.

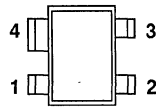
For additional design information please see performance curves DMCB, which are located in Section 7.

PART NUMBER	$V_{(BR)DS}$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)	C_{rss} MAX (pF)	t_{ON} MAX (ns)
SST211	10	50	0.5	2
SST213	10	50	0.5	2
SST215	20	50	0.5	2

SOT-143



TOP VIEW



1 SOURCE
2 DRAIN
3 GATE
4 SUBSTRATE

PRODUCT MARKING	
SST211	D11
SST213	D13
SST215	D15

SIMILAR PRODUCTS

- TO-18, See SD211DE Series
- Quad Array, See SD5000 Series
- SO-14 Array, See SD5400 Series
- Chips, Order SD21XCHP

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT			UNITS
		SST211	SST213	SST215	
Gate-Source, Gate-Drain Voltage	V_{GS},V_{GD}	-30/25	-15/25	-25/30	V
Gate-Substrate Voltage [1]	V_{GB}	-0.3/25	-0.3/25	-0.3/30	
Drain-Source Voltage	V_{DS}	30	10	20	
Source-Drain Voltage	V_{SD}	10	10	20	
Drain-Substrate Voltage	V_{DB}	30	15	25	
Source-Substrate Voltage	V_{SB}	15	15	25	
Drain Current	I_D	50	50	50	mA
Power Dissipation	P_D	350	350	350	mW
Power Derating		2.8	2.8	2.8	mW/°C
Operating Junction Temperature	T_J	-55 to 150			°C
Storage Temperature	T_{stg}	-65 to 150			
Lead Temperature (1/16" from case for 10 seconds)	T_L	300			

[1] These devices feature an internal Zener diode

ELECTRICAL CHARACTERISTICS [1]				LIMITS							
					SST211		SST213		SST215		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC											
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = V_{BS} = 0$ V, $I_D = 10\,\mu A$		35	30						V
		$V_{GS} = V_{BS} = -5$ V, $I_S = 10$ nA		30	10		10		20		
Source-Drain Breakdown Voltage	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5$ V, $I_D = 10$ nA		22	10		10		20		
Drain-Substrate Breakdown Voltage	$V_{(BR)DB}$	$V_{GB} = 0$ V, $I_D = 10$ nA Source OPEN		35	15		15		25		
Source-Substrate Breakdown Voltage	$V_{(BR)SB}$	$V_{GB} = 0$ V, $I_S = 10\,\mu A$ Drain OPEN		35	15		15		25		
Drain-Source Leakage	$I_{DS(OFF)}$	$V_{GS} = V_{BS} = -5$ V	$V_{DS} = 10$ V	0.4		10		10			nA
			$V_{DS} = 20$ V	0.9						10	
Source-Drain Leakage	$I_{SD(OFF)}$	$V_{GD} = V_{BD} = -5$ V	$V_{SD} = 10$ V	0.5		10		10			
			$V_{SD} = 20$ V	1						10	
Gate Leakage	I_{GBS}	$V_{DB} = V_{SB} = 0$ V, $V_{GB} = \pm 25$ V		10^{-5}		10		10		10	μA
Threshold Voltage	$V_{GS}(th)$	$V_{DS} = V_{GS} = V_{GS(th)}$, $I_S = 1\,\mu A$, $V_{SB} = 0$ V		0.7	0.5	2	0.1	2	0.1	2	V
Drain-Source On-Resistance	$r_{DS(ON)}$	$I_D = 1$ mA, $V_{SB} = 0$ V	$V_{GS} = 5$ V	58		75		75		75	Ω
			$V_{GS} = 10$ V	38		50		50		50	
			$V_{GS} = 15$ V	30							
			$V_{GS} = 20$ V	26							
			$V_{GS} = 25$ V	24							
DYNAMIC											
Forward Transconductance	g_{fs}	$V_{DS} = 10$ V, $V_{SB} = 0$ V, $I_D = 20$ mA, f = 1 kHz		11	9		9		9		mS
Output Conductance	g_{os}			0.9							
Gate Node Capacitance	$C_{(GS+GD+GB)}$	$V_{DS} = 10$ V, f = 1 MHz, $V_{GS} = V_{BS} = -15$ V		2.5		3.5		3.5		3.5	pF
Drain Node Capacitance	$C_{(GD+DB)}$			1.1		1.5		1.5		1.5	
Source Node Capacitance	$C_{(GS+SB)}$			3.7		6		6		6	
Reverse Transfer Capacitance	C_{rss}			0.2		0.5		0.5		0.5	
SWITCHING											
Turn-ON Time	$t_{d(ON)}$	$V_{DD} = 5$ V, $R_L = 680\ \Omega$, $V_{IN} = 0$ to 5 V		0.5		1		1		1	ns
	t_r			0.6		1		1		1	
Turn-OFF Time	$t_{d(OFF)}$			2							
	t_f			6							

NOTES: 1. $T_A = 25$ °C unless otherwise noted.
2. For design aid only, not subject to production testing.

5

LOW POWER MOS

INTRODUCTION

Low Power MOS products from Siliconix utilize a vertical DMOS process to offer a wide range of both n- and p-channel Enhancement-mode and n-channel Depletion-mode devices. The vertical structure allows high breakdown voltage, low on-resistance, low capacitance, and fast switching. Inherent in its MOS process, these devices also feature a high-impedance gate and freedom from the thermal runaway typically associated with bipolar devices.

To meet a wide range of applications Siliconix' Low Power MOS product line features n-channel Enhancement-mode devices with breakdown voltages ranging from 30 – 500 volts, on-resistance as low as 1.2 Ω, and many devices with threshold voltages less than 2.5 volts. P-channel devices designed to complement n-channel products are offered with breakdown voltage ranging from 30 – 240 volts, on-resistance as low as 1.8 Ω, and a family of low threshold devices again with threshold voltages less than 2.5 volts.

A recent unique addition to this product line was a family of high voltage n-channel Depletion-mode products. This series features normally "on" operation, breakdown voltage up to 240 volts, and on-resistance as low as 6 Ω. Depletion-mode performance is perfect for use in telecommunications and industrial process control applications.

Packaging options are diverse and include SOT-23, TO-92, TO-237, and 14-pin DIPs for commercial applications and TO-39, TO-52, and 14-pin ceramic packages for demanding industrial or military applications. Full military processing is available per MIL-S-19500 on all hermetically sealed packages.

For additional technical information please see "High-Side Switching" (LPD-17), "Depletion-mode Applications" (LPD-18), "Logic compatable MOS" (LPD-19), and "FETs in Telecom" (LPD-16). These application notes are located in section nine and provide useful design tips and device information.

2N6659

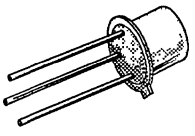
Siliconix incorporated

N-Channel Enhancement-Mode MOS Transistor

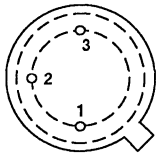
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
35	1.8	1.4	TO-205AD

TO-205AD (TO-39)



BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN & CASE

Performance Curves: **VNDQ06** (See Section 7)

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	2N6659	UNITS
Drain-Source Voltage		V_{DS}	35	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current [1]	T_C = 25°C	I_D	1.4	A
	T_C = 100°C		1	
Pulsed Drain Current [1]		I_{DM}	3	
Power Dissipation	T_C = 25°C	P_D	6.25	W
	T_C = 100°C		2.5	
Operating Junction Temperature		T_j	-55 to 150	°C
Storage Temperature [2]		T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	2N6659	UNITS
Junction-to-Ambient [2]	R_{thJA}	170	°C/W
Junction-to-Case	R_{thJC}	20	

[1] Pulse width limited by maximum junction temperature
[2] This parameter not registered with JEDEC

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				2N6659		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	70	35		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.5	0.8	2	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±15 V	±1		±100	nA
		V_{DS} = 0 V, V_{GS} = ±15 V, T_C = 125°C	±5		±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 35 V	0.05		10	µA
		V_{GS} = 0 V, V_{DS} = 28 V, T_C = 125°C	0.3		500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.8	1.5		A
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	[4] V_{GS} = 5 V, I_D = 0.3 A	1.8		5	Ω
		V_{GS} = 10 V, I_D = 1 A	1.3		1.8	Ω
		V_{GS} = 10 V, I_D = 1 A, [4] T_C = 125°C	2.6		3.6	Ω
Drain-Source On-Voltage[3]	$V_{DS(ON)}$	[4] V_{GS} = 5 V, I_D = 0.3 A	0.54		1.5	V
		V_{GS} = 10 V, I_D = 1 A	1.3		1.8	V
		V_{GS} = 10 V, I_D = 1 A, [4] T_C = 125°C	2.6		3.6	V
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	350	170		mS
Common Source Output Conductance[3,4]	g_{OS}	V_{DS} = 10 V, I_D = 0.1 A	1100			µS
DYNAMIC						
Small Signal Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 10 V, I_D = 1 A, f = 1 kHz	1.3		1.8	Ω
Drain-Source Capacitance	C_{ds}	V_{DS} = 24 V, V_{GS} = 0 V, f = 1 MHz	30		40	pF
Input Capacitance	C_{iss}	V_{DS} = 24 V, V_{GS} = 0 V, f = 1 MHz	38		50	pF
Output Capacitance[4]	C_{oss}		28		40	pF
Reverse Transfer Capacitance	C_{rss}		8		10	pF
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	8		10	ns
Turn-Off Time	t_{OFF}		9		10	ns

NOTES: 1. T_C = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 80 µs, duty cycle ≤ 1%.
4. This parameter not registered with JEDEC.

6

2N6660

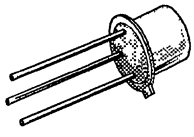
Siliconix incorporated

N-Channel Enhancement-Mode MOS Transistor

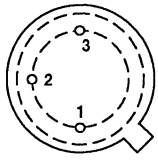
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
60	3	1.1	TO-205AD

TO-205AD (TO-39)



BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN & CASE

Performance Curves: **VNDQ06** (See Section 7)

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	2N6660	UNITS
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	1.1	A
	T_C = 100°C		0.8	
Pulsed Drain Current[1]		I_{DM}	3	
Power Dissipation	T_C = 25°C	P_D	6.25	W
	T_C = 100°C		2.5	
Operating Junction Temperature[2]		T_j	-55 to 150	°C
Storage Temperature		T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	2N6660	UNITS
Junction-to-Ambient[2]	R_{thJA}	170	°C/W
Junction-to-Case	R_{thJC}	20	

[1]Pulse width limited by maximum junction temperature
[2]This parameter not registered with JEDEC

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				2N6660		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	70	60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.5	0.8	2	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±15 V	±1		±100	nA
		V_{DS} = 0 V, V_{GS} = ±15 V, T_C = 125°C	±5		±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 60 V	0.05		10	µA
		V_{GS} = 0 V, V_{DS} = 48 V, T_C = 125°C	0.3		500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.8	1.5		A
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	[4] V_{GS} = 5 V, I_D = 0.3 A	1.8		5	Ω
		V_{GS} = 10 V, I_D = 1 A	1.3		3	Ω
		V_{GS} = 10 V, I_D = 1 A, [4] T_C = 125°C	2.6		4.2	Ω
Drain-Source On-Voltage[3]	$V_{DS(ON)}$	[4] V_{GS} = 5 V, I_D = 0.3 A	0.54		1.5	V
		V_{GS} = 10 V, I_D = 1 A	1.3		3	V
		V_{GS} = 10 V, I_D = 1 A, [4] T_C = 125°C	2.6		4.2	V
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	350	170		mS
Common Source Output Conductance[3,4]	g_{OS}	V_{DS} = 10 V, I_D = 0.1 A	1100			µS
DYNAMIC						
Small Signal Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 10 V, I_D = 1 A, f = 1 kHz	1.3		3	Ω
Drain-Source Capacitance	C_{ds}	V_{DS} = 24 V, V_{GS} = 0 V, f = 1 MHz	30		40	pF
Input Capacitance	C_{iss}	V_{DS} = 24 V, V_{GS} = 0 V, f = 1 MHz	38		50	pF
Output Capacitance[4]	C_{oss}		28		40	pF
Reverse Transfer Capacitance	C_{rss}		8		10	pF
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	8		10	ns
Turn-Off Time	t_{OFF}		9		10	ns

NOTES: 1. T_C = 25°C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 80 µs, duty cycle ≤ 1%.
4. This parameter not registered with JEDEC.

6

2N6660 JANTX, JANTXV

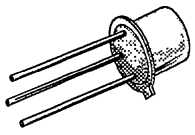
Siliconix incorporated

N-Channel Enhancement-Mode MOS Transistor

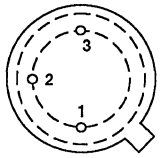
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
60	3	0.99	TO-205AD

TO-205AD (TO-39)



BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN & CASE

Performance Curves: **VNMA06** (See Section 7)

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	2N6660	UNITS
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	0.99	A
	T_C = 100°C		0.62	
Pulsed Drain Current[1]		I_{DM}	3	
Power Dissipation	T_C = 25°C	P_D	6.25	W
	T_A = 25°C		0.725	
Operating Junction Temperature		T_j	-65 to 150	°C
Storage Temperature		T_{stg}	-65 to 175	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	2N6660	UNITS
Junction-to-Ambient	R_{thJA}	170	°C/W
Junction-to-Case	R_{thJC}	20	

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				2N6660		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	90	60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.5	0.8	2	V
		T_C = -55°C	1.9		2.5	
		T_C = 125°C	1	0.3		
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	±1		±100	nA
		T_C = 125°C	±5		±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 48 V	0.0004		1	µA
		V_{DS} = 48 V, T_C = 125°C	2		100	
On-State Drain Current[3, 4]	$I_{D(ON)}$	V_{DS} = 7.5 V, V_{GS} = 10 V	2			A
Drain-Source On-Resistance[3, 5]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.3 A	3.5		5	Ω
		V_{GS} = 10 V, I_D = 1 A	2.25		3	
		T_C = 125°C	4		5.6	
Drain-Source On-Voltage[3]	$V_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.3 A	1.05		1.5	V
		V_{GS} = 10 V, I_D = 1 A	2.25		3	
		T_C = 125°C	4		5.6	
Forward Transconductance[3]	g_{FS}	V_{DS} = 7.5 V, I_D = 0.525 A	275	170		mS
Common Source Output Conductance[3,4]	g_{OS}	V_{DS} = 7.5 V, I_D = 0.1 A	900			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	30		50	pF
Output Capacitance	C_{oss}		30		40	
Reverse Transfer Capacitance	C_{rss}		5		10	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A, V_{GEN} = 10 V, R_G = 50 Ω (Switching time is essentially independent of operating temperature)	7		10	ns
Turn-Off Time	t_{OFF}		6		10	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS [1]			LIMITS			
				2N6660		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
Forward Voltage	V_{SD}	I_S = 0.99 A	0.8	0.7	1.6	V

NOTES: 1. T_C = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 80 µs, duty cycle ≤ 1%.
4. This parameter not registered with MIL-S-19500/547A.
5. Not a measured value $r_{DS(ON)} = V_{DS(ON)}/I_D$.

2N6661

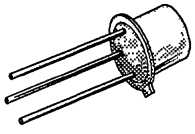
Siliconix incorporated

N-Channel Enhancement-Mode MOS Transistor

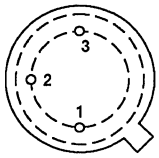
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
90	4	0.9	TO-205AD

TO-205AD (TO-39)



BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN & CASE

Performance Curves: **VNDQ09** (See Section 7)

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	2N6661	UNITS
Drain-Source Voltage		V_{DS}	90	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	0.9	A
	T_C = 100°C		0.7	
Pulsed Drain Current[1]		I_{DM}	3	
Power Dissipation	T_C = 25°C	P_D	6.25	W
	T_C = 100°C		2.5	
Operating Junction Temperature[2]		T_J	-55 to 150	°C
Storage Temperature		T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	2N6661	UNITS
Junction-to-Ambient[2]	R_{thJA}	170	°C/W
Junction-to-Case	R_{thJC}	20	

[1]Pulse width limited by maximum junction temperature
[2]This parameter not registered with JEDEC

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				2N6661		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	120	90		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.6	0.8	2	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±15 V	±1		±100	nA
		T_C = 125°C	±5		±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 90 V	0.03		10	µA
		V_{DS} = 72 V, T_C = 125°C	0.3		500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 15 V, V_{GS} = 10 V	1.8	1.5		A
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	[4] V_{GS} = 5 V, I_D = 0.3 A	4.2		5.3	Ω
		V_{GS} = 10 V, I_D = 1 A	3.6		4	Ω
		[4] T_C = 125°C	6.8		9	Ω
Drain-Source On-Voltage[3]	$V_{DS(ON)}$	[4] V_{GS} = 5 V, I_D = 0.3 A	1.26		1.6	V
		V_{GS} = 10 V, I_D = 1 A	3.6		4	V
		[4] T_C = 125°C	6.8		9	V
Forward Transconductance[3,4]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	350	170		mS
Common Source Output Conductance[3,4]	g_{OS}	V_{DS} = 10 V, I_D = 0.1 A	225			µS
DYNAMIC						
Small Signal Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 10 V, I_D = 1 A, f = 1 kHz	3.6		4	Ω
Drain-Source Capacitance	C_{ds}	V_{DS} = 24 V, V_{GS} = 0 V, f = 1 MHz	30		40	pF
Input Capacitance	C_{iss}	V_{DS} = 24 V, V_{GS} = 0 V, f = 1 MHz	35		50	pF
Output Capacitance[4]	C_{oss}		15		40	pF
Reverse Transfer Capacitance	C_{rss}		2		10	pF
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	6		10	ns
Turn-Off Time	t_{OFF}		8		10	ns

NOTES:
1. T_C = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 80 µs, duty cycle ≤ 1%.
4. This parameter not registered with JEDEC.

2N6661 JANTX, JANTXV

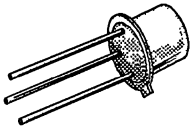
Siliconix incorporated

N-Channel Enhancement-Mode MOS Transistor

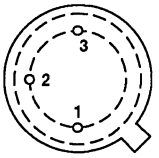
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
90	4	0.86	TO-205AD

TO-205AD (TO-39)



BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN & CASE

Performance Curves: **VNMA09** (See Section 7)

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	2N6661	UNITS
Drain-Source Voltage		V_{DS}	90	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	0.86	A
	T_C = 100°C		0.54	
Pulsed Drain Current[1]		I_{DM}	3	
Power Dissipation	T_C = 25°C	P_D	6.25	W
	T_A = 25°C		0.725	
Operating Junction Temperature		T_j	-65 to 150	°C
Storage Temperature		T_{stg}	-65 to 175	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	2N6661	UNITS
Junction-to-Ambient	R_{thJA}	170	°C/W
Junction-to-Case	R_{thJC}	20	

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				2N6661		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	130	90		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.3	0.8	2	
		T_C = -55°C	1.7		2.5	
		T_C = 125°C	0.8	0.3		
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	±1		±100	nA
		T_C = 125°C	±5		±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 72 V	0.01		1	µA
		V_{DS} = 72 V, T_C = 125°C	30		100	
On-State Drain Current[3, 4]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.7			A
Drain-Source On-Resistance[3, 5]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.3 A	4.3		5.3	Ω
		V_{GS} = 10 V, I_D = 1 A	2.75		4	
		T_C = 125°C	5		7.5	
Drain-Source On-Voltage[3]	$V_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.3 A	1.3		1.6	V
		V_{GS} = 10 V, I_D = 1 A	2.75		4	
		T_C = 125°C	5		7.5	
Forward Transconductance[3]	g_{FS}	V_{DS} = 7.5 V, I_D = 0.475 A	250	170		mS
Common Source Output Conductance[3,4]	g_{OS}	V_{DS} = 7.5 V, I_D = 0.1 A	425			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	30		50	pF
Output Capacitance	C_{oss}		30		40	
Reverse Transfer Capacitance	C_{rss}		5		10	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A, V_{GEN} = 10 V, R_G = 50 Ω (Switching time is essentially independent of operating temperature)	8.5		10	ns
Turn-Off Time	t_{OFF}		9.6		10	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS [1]			LIMITS			
				2N6661		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
Forward Voltage	V_{SD}	I_S = 0.86 A	0.9	0.7	1.4	V

NOTES:
1. T_C = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 80 µs, duty cycle ≤ 1%.
4. This parameter not registered with MIL-S-19500/547A.
5. Not a measured value $r_{DS(ON)} = V_{DS(ON)}/I_D$.

2N7000

Siliconix incorporated

N-Channel Enhancement-Mode MOS Transistor

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
60	5	0.2	TO-92

TO-92 BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN

Performance Curves: **VNDS06** (See Section 7)

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	2N7000	UNITS
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±40	
Continuous Drain Current	T_C = 25°C	I_D	±0.2	A
	T_C = 100°C		0.13	
Pulsed Drain Current[1]		I_{DM}	0.5	
Pulsed Power Dissipation[2]			3.1	W
Power Dissipation	T_C = 25°C	P_D	0.4	
	T_C = 100°C		0.16	
Operating Junction Temperature		T_j	-55 to 150	°C
Storage Temperature		T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	2N7000	UNITS
Junction-to-Ambient	R_{thJA}	312.5	°C/W
Junction-to-Case	R_{thJC}	40	

[1]Pulse width limited by maximum junction temperature
[2]One second single, power pulse

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				2N7000		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	70	60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2.3	0.8	3	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±15 V	± 1		± 10	nA
		V_{DS} = 0 V, V_{GS} = ±15 V, [4]T_C = 125°C	± 5			nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 48 V	0.001		1	µA
		V_{GS} = 0 V, V_{DS} = 48 V, T_C = 125°C	0.02		1000	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 4.5 V	210	75		mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	[4]V_{GS} = 4.5 V, I_D = 75 mA	4.8		5.3	Ω
		V_{GS} = 10 V, I_D = 0.5 A	2.5		5	Ω
		V_{GS} = 10 V, I_D = 0.5 A, T_C = 125°C	4.4		9	Ω
Drain-Source On-Voltage[3]	$V_{DS(ON)}$	[4]V_{GS} = 4.5 V, I_D = 75 mA	0.36		0.4	V
		V_{GS} = 10 V, I_D = 0.5 A	1.25		2.5	V
		V_{GS} = 10 V, I_D = 0.5 A, [4]T_C = 125°C	2.2		4.5	V
Forward Transconductance[3]	g_{fs}	V_{DS} = 10 V, I_D = 0.2 A, f = 1 kHz	170	100		mS
Common Source Output Conductance[3,4]	g_{os}	V_{DS} = 5 V, I_D = 50 mA	500			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	16		60	pF
Output Capacitance	C_{oss}		11		25	pF
Reverse Transfer Capacitance	C_{rss}		2		5	pF
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 15 V, R_L = 25 Ω, I_D = 0.5 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	7		10	ns
Turn-Off Time	t_{OFF}		7		10	ns

NOTES: 1. T_A = 25°C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.
4. This parameter not registered with JEDEC.

2N7001

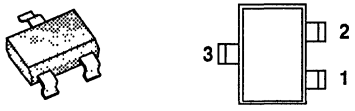
Siliconix incorporated

N-Channel Enhancement-Mode MOS Transistor

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
240	45	0.045	SOT-23

SOT-23 TOP VIEW



1 GATE
2 SOURCE
3 DRAIN

Performance Curves: **VNDN24** (See Section 7)

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	2N7001	UNITS
Drain-Source Voltage		V_{DS}	240	V
Gate-Source Voltage		V_{GS}	±40	
Continuous Drain Current	T_C = 25°C	I_D	0.045	A
	T_C = 100°C		0.029	
Pulsed Drain Current[1]		I_{DM}	0.21	
Power Dissipation	T_C = 25°C	P_D	200	mW
	T_C = 100°C		80	
Operating Junction Temperature		T_j	-55 to 150	°C
Storage Temperature		T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	2N7001	UNITS
Junction-to-Ambient	R_{thJA}	625	°C/W

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				2N7001		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 100 µA	270	240		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 0.25 mA	1.85	1	2.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	±1		±10	nA
		[4] T_C = 125°C	±5			nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 120 V	0.001		0.1	µA
		V_{GS} = 0 V, V_{DS} = 120 V, T_C = 125°C	0.5		1	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	750	100		mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 50 mA	35		85	Ω
		[4] V_{GS} = 4.5 V, I_D = 20 mA	40		45	Ω
		T_C = 125°C	80		85	Ω
Drain-Source On-Voltage[3]	$V_{DS(ON)}$	V_{GS} = 10 V, I_D = 50 mA	1.75		2.25	V
		[4] V_{GS} = 4.5 V, I_D = 20 mA	0.8		0.9	V
		T_C = 125°C	1.6		1.7	V
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 50 mA	80	30		mS
Common Source Output Conductance[3,4]	g_{OS}		10			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	15		30	pF
Output Capacitance	C_{oss}		4		15	pF
Reverse Transfer Capacitance	C_{rss}		1		10	pF
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 60 V, R_L = 1.2 kΩ, I_D = 50 mA, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	7		30	ns
Turn-Off Time	t_{OFF}		18		20	ns

NOTES: 1. T_C = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 80 µs, duty cycle ≤ 1%.
4. This parameter not registered with JEDEC.

6

2N7002

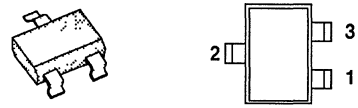
Siliconix incorporated

N-Channel Enhancement-Mode MOS Transistor

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
60	7.5	0.115	SOT-23

SOT-23 TOP VIEW



1 GATE
2 DRAIN
3 SOURCE

Performance Curves: **VNDS06** (See Section 7)

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	2N7002	UNITS
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±40	
Continuous Drain Current	T_C = 25°C	I_D	± 0.115	A
	T_C = 100°C		± 0.073	
Pulsed Drain Current[1]		I_{DM}	0.8	
Power Dissipation	T_C = 25°C	P_D	200	mW
	T_C = 100°C		80	
Operating Junction Temperature		T_j	-55 to 150	°C
Storage Temperature		T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	2N7002	UNITS
Junction-to-Ambient	R_{thJA}	625	°C/W

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				2N7002		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	70	60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 0.25 mA	2.15	1	2.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	± 1		±100	nA
		T_C = 125°C	± 5			nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 60 V	0.02		1	µA
		T_C = 125°C	1		500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} ≥ 2 $V_{DS(ON)}$, V_{GS} = 10 V	1000	500		mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 50 mA	5		7.5	Ω
		T_C = 125°C	9		13.5	Ω
		V_{GS} = 10 V, I_D = 0.5 A	2.5		7.5	Ω
		T_C = 125°C	4.4		13.5	Ω
Drain-Source On-Voltage[3]	$V_{DS(ON)}$	V_{GS} = 5 V, I_D = 50 mA	0.25		0.375	V
		V_{GS} = 10 V, I_D = 0.5 A	1.25		3.75	V
		[4]T_C = 125°C	2.2		6.75	V
Forward Transconductance[3]	g_{fs}	V_{DS} = 10 V, I_D = 0.2 A, f = 1 kHz	170	80		mS
Common Source Output Conductance[3,4]	g_{OS}	V_{DS} = 5 V, I_D = 50 mA	500			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	16		50	pF
Output Capacitance	C_{oss}		11		25	pF
Reverse Transfer Capacitance	C_{rss}		2		5	pF
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 30 V, R_L = 150 Ω, I_D = 0.2 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	7		20	ns
Turn-Off Time	t_{OFF}		7		20	ns

NOTES: 1. T_C = 25°C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 80 µs, duty cycle ≤ 1%.
4. This parameter not registered with JEDEC.

2N7007

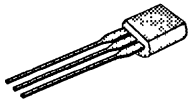
Siliconix incorporated

N-Channel Enhancement-Mode MOS Transistor

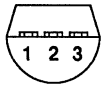
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
240	45	0.065	TO-92

TO-92



BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN

Performance Curves: **VNDN24** (See Section 7)

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	2N7007	UNITS
Drain-Source Voltage		V_{DS}	240	V
Gate-Source Voltage		V_{GS}	±40	
Continuous Drain Current	T_C = 25°C	I_D	0.065	A
	T_C = 100°C		0.041	
Pulsed Drain Current[1]		I_{DM}	0.260	
Power Dissipation	T_C = 25°C	P_D	0.4	W
	T_C = 100°C		0.16	
Operating Junction Temperature		T_j	-55 to 150	°C
Storage Temperature		T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	2N7007	UNITS
Junction-to-Ambient	R_{thJA}	312.5	°C/W

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				2N7007		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 100 µA	270	240		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 0.25 mA	1.85	1	2.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	±1		±10	nA
		V_{DS} = 0 V, V_{GS} = ±20 V, T_C = 125°C	±5			nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 120 V	0.001		0.1	µA
		V_{GS} = 0 V, V_{DS} = 120 V, T_C = 125°C	0.6		1	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 20 V, V_{GS} = 4.5 V	100	50		mA
		V_{DS} = 20 V, V_{GS} = 10 V	170	150		mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 4.5 V, I_D = 20 mA	40		45	Ω
		V_{GS} = 4.5 V, I_D = 20 mA, T_C = 125°C	80		85	Ω
		V_{GS} = 10 V, I_D = 50 mA	35		45	Ω
		V_{GS} = 10 V, I_D = 50 mA, T_C = 125°C	75		85	Ω
Drain-Source On-Voltage[3]	$V_{DS(ON)}$	V_{GS} = 4.5 V, I_D = 20 mA	0.8		0.9	V
		V_{GS} = 10 V, I_D = 50 mA	1.75		2.25	V
		V_{GS} = 10 V, I_D = 50 mA, [4]T_C = 125°C	3.75		4.25	V
Forward Transconductance[3]	g_{fs}	V_{DS} = 10 V, I_D = 50 mA, f = 1 kHz	50	30		mS
Common Source Output Conductance[3,4]	g_{OS}	V_{DS} = 10 V, I_D = 50 mA	10			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	15		30	pF
Output Capacitance	C_{oss}		4		15	pF
Reverse Transfer Capacitance	C_{rss}		1		10	pF
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 60 V, R_L = 1.2 kΩ, I_D = 50 mA, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	7		30	ns
Turn-Off Time	t_{OFF}		18		20	ns

NOTES: 1. T_C = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 80 µs, duty cycle ≤ 1%.
4. This parameter not registered with JEDEC.

2N7008

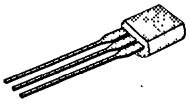
Siliconix incorporated

N-Channel Enhancement-Mode MOS Transistor

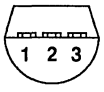
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
60	7.5	0.15	TO-92

TO-92



BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN

Performance Curves: **VNDS06** (See Section 7)

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	2N7008	UNITS
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±40	
Continuous Drain Current	T_C = 25°C	I_D	0.15	A
	T_C = 100°C		0.1	
Pulsed Drain Current[1]		I_{DM}	1	
Power Dissipation	T_C = 25°C	P_D	400	mW
	T_C = 100°C		160	
Operating Junction Temperature		T_j	-55 to 150	°C
Storage Temperature		T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	2N7008	UNITS
Junction-to-Ambient	R_{thJA}	312.5	°C/W

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				2N7008		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	70	60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 0.25 mA	2.15	1	2.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±30 V	± 1		±100	nA
		V_{DS} = 0 V, V_{GS} = ±30 V, [4]T_C = 125°C	± 5			nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 50 V	0.02		1	µA
		V_{GS} = 0 V, V_{DS} = 50 V, T_C = 125°C	1		500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} ≥ 2 $V_{DS(ON)}$, V_{GS} = 10 V	1000	500		mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 50 mA	5		7.5	Ω
		V_{GS} = 5 V, I_D = 50 mA, T_C = 125°C	9		13.5	Ω
		V_{GS} = 10 V, I_D = 0.5 A	2.5		7.5	Ω
		V_{GS} = 10 V, I_D = 0.5 A, T_C = 125°C	4.4		13.5	Ω
Drain-Source On-Voltage[3]	$V_{DS(ON)}$	V_{GS} = 5 V, I_D = 50 mA	0.25		0.375	V
		V_{GS} = 10 V, I_D = 0.5 A	1.25		3.75	V
		V_{GS} = 10 V, I_D = 0.5 A, [4]T_C = 125°C	2.2		6.75	V
Forward Transconductance[3]	g_{fs}	V_{DS} = 10 V, I_D = 0.2 A, f = 1 kHz	170	80		mS
Common Source Output Conductance[3,4]	g_{OS}	V_{DS} = 5 V, I_D = 50 mA	500			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	16		50	pF
Output Capacitance	C_{oss}		11		25	pF
Reverse Transfer Capacitance	C_{rss}		2		5	pF
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 30 V, R_L = 150 Ω, I_D = 0.2 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	7		20	ns
Turn-Off Time	t_{OFF}		7		20	ns

NOTES: 1. T_C = 25°C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 80 µs, duty cycle ≤ 1%.
4. This parameter not registered with JEDEC.

6

3N163 SERIES

Siliconix incorporated

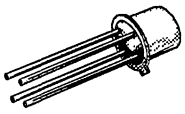
P-Channel Enhancement-Mode MOS Transistors

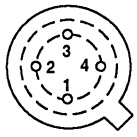
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (mA)	PACKAGE
3N163	–40	250	–50	TO-72
3N164	–30	300	–50	TO-72

Performance Curves: **MRA** (See Section 7)

TO-72 **BOTTOM VIEW**





1 DRAIN
2 GATE
3 SUBSTRATE, CASE
4 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	3N163	3N164	UNITS
Drain-Source Voltage	V_{DS}	–40	–30	V
Gate-Source Voltage	V_{GS}	±40	±30	
Transient Gate-Source Voltage		±125	±125	
Continuous Drain Current	I_D	–50	–50	mA
Power Dissipation	P_D	375	375	mW
Power Derating		3	3	
Operating Junction	T_J	–55 to 150		°C
Storage Temperature	T_{stg}	–65 to 200		
Lead Temperature (1/16" from case for 10 seconds)	T_L	300		

ELECTRICAL CHARACTERISTICS[1]			LIMITS					
				3N163		3N164		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = -10 µA	-70	-40		-30		V
Source-Drain Breakdown Voltage	$V_{(BR)SDS}$	$V_{GD} = V_{BD}$ = 0 V, I_S = -10 µA	-70	-40		-30		V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$, I_D = -10 µA	-2.5	-2	-5	-2	-5	V
Gate-Source Voltage	V_{GS}	V_{DS} = -15 V, I_D = -0.5 mA	-3.5	-3	-6.5	-2.5	-6.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = -40 V	<-1		-10			pA
		T_A = 125°C	-1		-25			pA
		V_{DS} = 0 V, V_{GS} = -30 V	<-1				-10	pA
		T_A = 125°C	-1				-25	pA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -15 V, V_{GS} = 0 V	-8		-200		-400	pA
		T_A = 125°C	-20					nA
Zero-Gate Voltage Source Current	I_{SDS}	V_{SD} = -20 V, $V_{GD} = V_{DB}$ = 0 V	-10		-400		-800	pA
		T_A = 125°C	-25					nA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = -15 V, V_{GS} = -10 V	-10	-5	-30	-3	-30	mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = -20 V, I_D = -100 µA	180		250		300	Ω
		T_A = 125°C	270					Ω
DYNAMIC								
Forward Transconductance[3]	g_{fs}	V_{DS} = -15 V, I_D = -10 mA, f = 1 kHz	2.7	2	4	1	4	mS
Common Source Output Conductance[3]	g_{os}	V_{DS} = -15 V, I_D = -10 mA, f = 1 kHz	150		250		250	µS
Input Capacitance	C_{iss}	V_{DS} = -15 V, I_D = -10 mA, f = 1 MHz	2.4		2.5		2.5	pF
Output Capacitance	C_{oss}	V_{DS} = -15 V, I_D = -10 mA, f = 1 MHz	2.5		3		3	pF
Reverse Transfer Capacitance	C_{rss}	V_{DS} = -15 V, I_D = -10 mA, f = 1 MHz	0.5		0.7		0.7	pF
SWITCHING								
Turn-On Time	$t_{d(ON)}$	V_{DD} = -15 V, R_L = 1500 Ω, I_D = -10 mA, V_{GEN} = 12 V, R_G = 50 Ω (Switching time is essentially independent of operating temperature)	5		12		12	ns
	t_r		13		24		24	ns
Turn-Off Time	t_{OFF}		25		50		50	ns

NOTES: 1. T_A = 25°C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

6

BS107

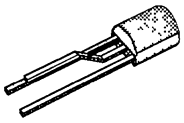
Siliconix incorporated

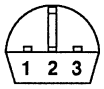
N-Channel Enhancement-Mode MOS Transistor

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
200	28	0.12	TO-92

TO-92-18 BOTTOM VIEW





1 SOURCE
2 GATE
3 DRAIN

Performance Curves: **VNDQ20** (See Section 7)

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	BS107	UNITS
Drain-Source Voltage	V_{DS}	200	V
Gate-Source Voltage	V_{GS}	±25	
Continuous Drain Current (T_A = 25°C)	I_D	0.12	A
Power Dissipation (T_A = 25°C)	P_D	0.5	W
Operating Junction and Storage Temperature	T_j, T_{stg}	−55 to 150	°C
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	BS107	UNITS
Junction-to-Ambient	R_{thJA}	250	°C/W

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				BS107		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 100 µA	225	200		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.45	0.8	3	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±15 V	±1		±10	nA
Drain Leakage Current	I_{DSX}	V_{DS} = 70 V, V_{GS} = 0.2 V			1	µA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 130 V, V_{GS} = 0 V	0.001		30	nA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 2.8 V, I_D = 20 mA	6		28	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.1 A	180			mS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V f = 1 MHz	35			pF
Output Capacitance	C_{oss}		9			pF
Reverse Transfer Capacitance	C_{rss}		1			pF
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 125 Ω I_D = 0.2 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	5			ns
Turn-Off Time	t_{OFF}		14			ns

NOTES: 1. T_C = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 80 µs, duty cycle ≤ 1%.

BS170

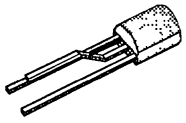
Siliconix incorporated

N-Channel Enhancement-Mode MOS Transistor

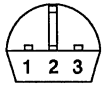
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
60	5	0.5	TO-92

TO-92-18



BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

Performance Curves: **VNDS06** (See Section 7)

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	BS170	UNITS
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±25	
Continuous Drain Current	T_A = 25°C	I_D	0.5	A
	T_A = 100°C		0.175	
Power Dissipation (T_A = 25°C)		P_D	0.83	W
Operating Junction and Storage Temperature		T_j, T_{stg}	−55 to 150	°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	BS170	UNITS
Junction-to-Ambient	R_{thJA}	156	°C/W

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				BS170		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 100 µA	70	60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2.3	0.8	3	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±15 V			±10	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 25 V, V_{GS} = 0 V	0.02		0.5	µA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 10 V , I_D = 0.2 A	2.5		5	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.2 A	230	100		mS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V f = 1 MHz	16		60	pF
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 125 Ω I_D = 0.2 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	7		10	ns
Turn-Off Time	t_{OFF}		7		10	ns

NOTES: 1. T_C = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 80 µs , duty cycle ≤ 1%.

BS208

Siliconix incorporated

P-Channel Enhancement-Mode MOS Transistor

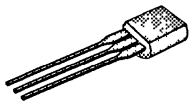
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
-200	14	-0.2	TO-92 RM

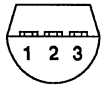
RM = Reverse Mold

Performance Curves: **VPDV24** (See Section 7)

TO-92



BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	BS208	UNITS
Drain-Source Voltage	V_{DS}	-200	V
Gate-Source Voltage	V_{GS}	±20	
Continuous Drain Current	I_D	-0.2	A
Pulsed Drain Current[1]	I_{DM}	-0.8	
Power Dissipation	P_D	0.83	W
Operating Junction and Storage Temperature	T_j, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	BS208	UNITS
Junction-to-Ambient	R_{thJA}	156	°C/W

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				BS208		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −100 µA	−230	−200		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −1 mA	−1.9			
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±15 V	±1		±10	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −130 V, V_{GS} = 0 V	−0.002		−1	µA
	I_{DSX}	V_{DS} = −70 V, V_{GS} = −0.2 V	−8		−25	
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = −10 V, V_{GS} = −4.5 V	−300			mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = −10 V, I_D = −100 mA	10		14	Ω
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = −20 V V_{GS} = 0 V f = 1 MHz	70			pF
Output Capacitance	C_{oss}		25			
Reverse Transfer Capacitance	C_{rss}		11			
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = −25 V, R_L = 125 Ω I_D = −200 mA, V_{GEN} = −10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	6			ns
	t_r		8			
Turn-Off TIme	$t_{d(OFF)}$		18			
	t_f		17			

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

6

BS250

Siliconix incorporated

P-Channel Enhancement-Mode MOS Transistor

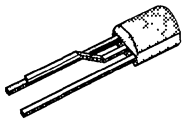
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
-45	14	-0.18	TO-92RM

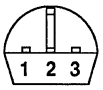
RM = Reverse Mold

Performance Curves: **VPDS06** (See Section 7)

TO-92-18



BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	BS250	UNITS
Drain-Source Voltage	V_{DS}	-45	V
Gate-Source Voltage	V_{GS}	±25	
Continuous Drain Current (T_A = 25°C)	I_D	-0.18	A
Power Dissipation	P_D	0.83	W
Operating Junction and Storage Temperature	T_j, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	BS250	UNITS
Junction-to-Ambient	R_{thJA}	150	°C/W

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				BS250		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = -100 µA	-70	-45		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA	-2	-1	-3.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±15 V	±1		±20	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -25 V, V_{GS} = 0 V	-0.20		-500	nA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = -10 V, I_D = -0.2 A	6		14	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = -10 V, I_D = -0.2 A	125			mS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = -10 V, V_{GS} = 0 V f = 1 MHz	15			pF
SWITCHING						
Turn-On Time	t_{ON}	I_D = -0.2 A	8		10	ns
Turn-Off Time	t_{OFF}	I_D = -0.2 A	8		10	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS[1]			LIMITS			
				BS250		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
Continuous Current	I_S				-0.18	A
Forward Voltage[3]	V_{SD}	I_F = I_S = -0.18 V, V_{GS} = 0 V	0.85			V

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

BSS89

Siliconix incorporated

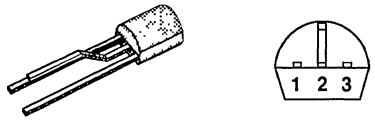
N-Channel Enhancement-Mode MOS Transistor

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
200	6	0.3	TO-92 CD

CD = Center Drain

TO-92-18 BOTTOM VIEW



1 GATE
2 DRAIN
3 SOURCE

Performance Curves: **VNDB24** (See Section 7)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	BSS89	UNITS
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_A = 25°C	I_D	0.3	A
Pulsed Drain Current[1]		I_{DM}	1.2	
Power Dissipation	T_A = 25°C	P_D	1	W
Operating Junction and Storage Temperature		T_j, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	BSS89	UNITS
Junction-to-Ambient	R_{thJA}	125	°C/W

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				BSS89		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	270	200		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.4	0.8	2.8	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V	1		100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 200 V, V_{GS} = 0 V	0.01		60	µA
		V_{DS} = 200 V, V_{GS} = 0 V, T_J = 125°C	1		200	µA
		V_{DS} = 60 V, V_{GS} = 0 V	5		200	nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 0.4 A	5		6	Ω
Forward Transconductance	g_{FS}	V_{DS} = 25 V, I_D = 0.4 A	0.4	0.14		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	105			pF
Output Capacitance	C_{oss}		25			pF
Reverse Transfer Capacitance	C_{rss}		5			pF
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = 30 V, R_L = 100 Ω, I_D = 0.28 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	3		20	ns
	t_r		2		60	ns
Turn-Off Time	$t_{d(OFF)}$		15		90	ns
	t_f		34		55	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS[1]			LIMITS			
				BSS89		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
Forward Voltage[3]	V_{SD}	I_F = I_S = -0.6 A, V_{GS} = 0 V	0.9		1.4	V

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

BSS92

Siliconix incorporated

P-Channel Enhancement-Mode MOS Transistor

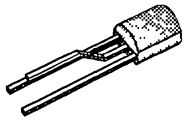
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
-200	20	-0.15	TO-92 CDRM

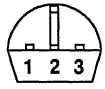
CD = Center Drain, RM = Reverse Mold, TO-18 Lead Form

Performance Curves: **VPDQ20** (See Section 7)

TO-92-18



BOTTOM VIEW



1 SOURCE
2 DRAIN
3 GATE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	BSS92	UNITS
Drain-Source Voltage		V_{DS}	-200	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_A = 25°C	I_D	-0.15	A
	T_A = 100°C		-0.09	
Pulsed Drain Current[1]		I_{DM}	-0.60	
Power Dissipation	T_A = 25°C	P_D	1.0	W
	T_A = 100°C		0.40	
Operating Junction and Storage Temperature		T_j, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	BSS92	UNITS
Junction-to-Ambient	R_{thJA}	125	°C/W

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				BSS92		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = -250 µA	-220	-200		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA	-1.9	-0.8	-2.8	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = -20 V	±1		±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -60 V, V_{GS} = 0 V	-0.01		-0.2	µA
		V_{DS} = -200 V, V_{GS} = 0 V	-0.02		-60	
		V_{DS} = -200 V, V_{GS} = 0 V, T_J = 125°C	-3		-200	
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = -10 V, I_D = -100 mA	11.4		20	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = -25 V, I_D = -100 mA	150	60		mS
DYNAMIC						
Input Capacitance	C_{lss}	V_{DS} = -25 V, V_{GS} = 0 V, f = 1 MHz	30			pF
Output Capacitance	C_{oss}		10			
Reverse Transfer Capacitance	C_{rss}		2			
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = -30 V, R_L = 120 Ω, I_D = -0.25 A, V_{GEN} = -10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	6			ns
	t_r		8			
Turn-Off Time	$t_{d(OFF)}$		18			
	t_f		17			

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS[1]			LIMITS			
				BSS92		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
Forward Voltage[3]	V_{SD}	I_F = I_S = -0.3 A, V_{GS} = 0 V	-0.9		-1.2	V

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

BSS129

Siliconix incorporated

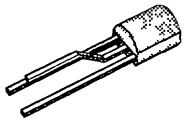
N-Channel Depletion-Mode MOS Transistor

PRODUCT SUMMARY

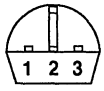
$V_{(BR)DSV}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
230	20	0.15	TO-92 CDRM

CD = Center Drain, RM = Reverse Mold

TO-92-18



BOTTOM VIEW



1 GATE
2 DRAIN
3 SOURCE

Performance Curves: **VDDV24** (See Section 7)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	BSS129	UNITS
Drain-Source Voltage		V_{DS}	230	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_A = 35°C	I_D	0.15	A
Pulsed Drain Current[1]		I_{DM}	0.60	
Power Dissipation		P_D	1	W
Operating Junction and Storage Temperature		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	BSS129	UNITS
Junction-to-Ambient	R_{thJA}	125	°C/W

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				BSS129		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSV}$	V_{GS} = -3 V, I_D = 250 mA	260	230		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 3 V, I_D = 1 mA	-2.3	-0.7		V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V	± 1		± 100	nA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 230 V, V_{GS} = -3 V	0.04		0.1	µA
		T_J = 125°C	7.5		200	µA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = 14 mA	4		20	Ω
Forward Transconductance	g_{FS}	V_{DS} = 25 V, I_D = 250 mA	175	140		mS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = -5 V, f = 1 MHz	70			pF
Output Capacitance	C_{oss}		20			pF
Reverse Transfer Capacitance	C_{rss}		10			pF
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = 25 V, R_L = 830 Ω, I_D = 30 mA, V_{GEN} = -5 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	15			ns
	t_r		75			ns
Turn-Off Time	$t_{d(OFF)}$		40			ns
	t_f		100			ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

MFE823

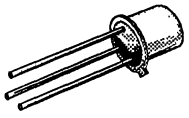
Siliconix incorporated

P-Channel Enhancement-Mode MOS Transistor

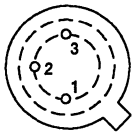
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	g_{fs} (mS)	I_D (mA)	PACKAGE
MFE823	–25	1	–30	TO-18

TO-18



BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE, SUBSTRATE
CASE

Performance Curves: MRA (See Section 7)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	MFE823	UNITS
Drain-Source Voltage		V_{DS}	–25	V
Gate-Source Voltage		V_{GS}	±10	
Continuous Drain Current	T_A = 25°C	I_D	–30	mA
Power Dissipation	T_A = 25°C	P_D	375	mW
Power Derating			3	mW/°C
Operating Junction		T_J	–55 to 150	°C
Storage Temperature		T_{stg}	–65 to 200	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				MFE823		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = -10 µA	-70	-25		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = -10 V, I_D = -10 µA	-2.5	-2	-6	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = -10 V	<-1		-1	pA
		T_A = 125°C	-1			pA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -10 V, V_{GS} = 0 V	-0.01		-20	nA
		T_A = 125°C	-20			nA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -10 V	-10	-3		mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = -20 V, I_D = -100 µA	180			Ω
DYNAMIC						
Forward Transconductance[3]	g_{fs}	V_{DS} = -10 V, I_D = -2 mA, f = 1 kHz	1.5	1		mS
Common Source Output Conductance[3]	g_{os}	V_{DS} = -10 V, I_D = -2 mA, f = 1 kHz	35			µS
Input Capacitance	C_{iss}	V_{DS} = -10 V, V_{GS} = -10 V, f = 1 MHz	2.4		6	pF
Reverse Transfer Capacitance	C_{rss}	V_{DS} = -10 V, V_{GS} = -10 V, f = 1 MHz	0.5		1.5	pF

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

ND2012 SERIES

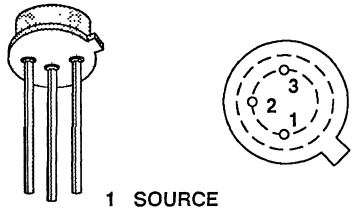
Siliconix incorporated

N-Channel Depletion-Mode MOS Transistors

TO-92 BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN

TO-206AC (TO-52) BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN & CASE

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSV}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
ND2012L	200	12	0.16	TO-92
ND2012E	200	12	0.22	TO-206AC

Performance Curves: **VDDQ20** (See Section 7)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	ND2012L	ND2012E[2]	UNITS
Drain-Source Voltage		V_{DS}	200	200	V
Gate-Source Voltage		V_{GS}	±30	±20	V
Continuous Drain Current	T_A = 25°C	I_D	0.16	0.22	A
	T_A = 100°C		0.10	0.14	A
Pulsed Drain Current[1]		I_{DM}	0.8	0.8	A
Power Dissipation	T_A = 25°C	P_D	0.80	1.5	W
	T_A = 100°C		0.32	0.60	W
Operating Junction and Storage Temperature		T_j, T_{stg}	−55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		°C

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	ND2012L	ND2012E	UNITS
Junction-to-Ambient	R_{thJA}	156	400	°C/W

[1]Pulse width limited by maximum junction temperature
[2]Reference case for all temperature testing

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				ND2012		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSV}$	V_{GS} = -8 V, I_D = 10 µA	220	200		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 5 V, I_D = 10 µA	-3	-1.5	-4	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	±0.1		±10	nA
		T_J = 125°C	±5		±50	nA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 160 V, V_{GS} = -8 V	0.2		1	µA
		T_J = 125°C	5		200	µA
Drain Saturation Current[3]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	400	30		mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 2 V, I_D = 20 mA	7			Ω
		V_{GS} = 0 V, I_D = 20 mA	8		12	Ω
		T_J = 125°C	15		30	Ω
Forward Transconductance	g_{FS}	V_{DS} = 7.5 V, I_D = 20 mA	55			mS
Common Source Output Conductance[3]	g_{OS}		75			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = -5 V, f = 1 MHz	35		100	pF
Output Capacitance	C_{oss}		10		20	pF
Reverse Transfer Capacitance	C_{rss}		2		5	pF
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = 25 V, R_L = 1250 Ω, I_D = 20 mA, V_{GEN} = -5 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	20			ns
	t_r		20			ns
Turn-Off Time	$t_{d(OFF)}$		10			ns
	t_f		10			ns

NOTES: 1. T_A = 25 °C unless otherwise noted, T_C = 25 °C for ND2012E.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

6

ND2020 SERIES

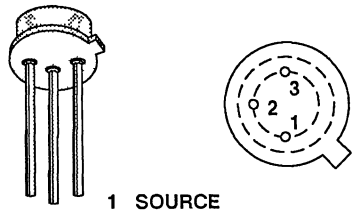
Siliconix incorporated

N-Channel Depletion-Mode MOS Transistors

TO-92 BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN

TO-206AC (TO-52) BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN & CASE

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSV}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
ND2020L	200	20	0.132	TO-92
ND2020E	200	20	0.18	TO-206AC

Performance Curves: **VDDQ20** (See Section 7)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	ND2020L	ND2020E[2]	UNITS
Drain-Source Voltage		V_{DS}	200	200	V
Gate-Source Voltage		V_{GS}	±30	±20	
Continuous Drain Current	T_A = 25°C	I_D	0.132	0.18	A
	T_A = 100°C		0.083	0.11	
Pulsed Drain Current[1]		I_{DM}	0.8	0.8	
Power Dissipation	T_A = 25°C	P_D	0.80	1.5	W
	T_A = 100°C		0.32	0.60	
Operating Junction and Storage Temperature		T_j, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	ND2020L	ND2020E	UNITS
Junction-to-Ambient	R_{thJA}	156	400	°C/W

[1]Pulse width limited by maximum junction temperature
[2]Reference case for all temperature testing

ELECTRICAL CHARACTERISTICS[1]			LIMITS					
				ND2020L		ND2020E		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Drain-Source Breakdown Voltage	$V_{(BR)DSV}$	V_{GS} = -5 V, I_D = 1 µA	220	200		200		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 5 V, I_D = 10 µA	-1.8	-0.5	-2.5	-0.5	-2.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	±0.1		±10		±10	nA
		V_{DS} = 0 V, V_{GS} = ±20 V, T_J = 125°C	±5		±50		±50	nA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 160 V, V_{GS} = -5 V	0.2		1		1	µA
		V_{DS} = 160 V, V_{GS} = -5 V, T_J = 125°C	5		200		200	µA
Drain Saturation Current[3]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	110	30		30		mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 2 V, I_D = 20 mA	10					Ω
		V_{GS} = 0 V, I_D = 20 mA	11		20		20	Ω
		V_{GS} = 0 V, I_D = 20 mA, T_J = 125°C	20		50		30	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 7.5 V, I_D = 20 mA	55					mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = 7.5 V, I_D = 20 mA	75					µS
DYNAMIC								
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = -5 V, f = 1 MHz	35		100		100	pF
Output Capacitance	C_{oss}	V_{DS} = 25 V, V_{GS} = -5 V, f = 1 MHz	10		20		20	pF
Reverse Transfer Capacitance	C_{rss}	V_{DS} = 25 V, V_{GS} = -5 V, f = 1 MHz	2		5		5	pF
SWITCHING								
Turn-On Time	$t_{d(ON)}$	V_{DD} = 25 V, R_L = 1250 Ω, I_D = 20 mA, V_{GEN} = -5 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	20					ns
	t_r		20					ns
Turn-Off Time	$t_{d(OFF)}$		10					ns
	t_f		10					ns

NOTES: 1. T_A = 25 °C unless otherwise noted, T_C = 25 °C for ND2020E.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

ND2406 SERIES

Siliconix incorporated

N-Channel Depletion-Mode MOS Transistors

TO-92 BOTTOM VIEW

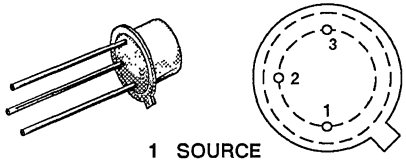
1 SOURCE
2 GATE
3 DRAIN

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSV}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
ND2406L	240	6	0.23	TO-92
ND2406B	240	6	0.57	TO-205AF

Performance Curves: **VDDV24** (See Section 7)

TO-205AF BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN & CASE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	ND2406L	ND2406B[2]	UNITS
Drain-Source Voltage		V_{DS}	240	240	V
Gate-Source Voltage		V_{GS}	±30	±20	
Continuous Drain Current	T_A = 25°C	I_D	0.23	0.57	A
	T_A = 100°C		0.14	0.36	
Pulsed Drain Current[1]		I_{DM}	0.90	1	
Power Dissipation	T_A = 25°C	P_D	0.80	5	W
	T_A = 100°C		0.32	2	
Operating Junction and Storage Temperature		T_j, T_{stg}	−55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	ND2406L	ND2406B	UNITS
Junction-to-Ambient	R_{thJA}	156	125	°C/W

[1]Pulse width limited by maximum junction temperature
[2]Reference case for all temperature testing

ELECTRICAL CHARACTERISTICS[1]			LIMITS					
				ND2406L		ND2406B		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Drain-Source Breakdown Voltage	$V_{(BR)DSV}$	V_{GS} = -9 V, I_D = 10 µA	260	240		240		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 5 V, I_D = 10 µA	-2.8	-1.5	-4.5	-1.5	-4.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	±1		±10		±10	nA
		V_{DS} = 0 V, V_{GS} = ±20 V, T_J = 125°C	±5		±50		±50	nA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 180 V, V_{GS} = -9 V	0.04		1		1	µA
		V_{DS} = 180 V, V_{GS} = -9 V, T_J = 125°C	15		200		200	µA
Drain Saturation Current[3]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	640	40		40		mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 2 V, I_D = 30 mA	3					Ω
		V_{GS} = 0 V, I_D = 30 mA	3.5		6		6	Ω
		V_{GS} = 0 V, I_D = 30 mA, T_J = 125°C	7		15		15	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 30 mA	110					mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = 10 V, I_D = 30 mA	70					µS
DYNAMIC								
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = -5 V, f = 1 MHz	70		120		120	pF
Output Capacitance	C_{oss}	V_{DS} = 25 V, V_{GS} = -5 V, f = 1 MHz	20		30		30	pF
Reverse Transfer Capacitance	C_{rss}	V_{DS} = 25 V, V_{GS} = -5 V, f = 1 MHz	10		15		15	pF
SWITCHING								
Turn-On Time	$t_{d(ON)}$	V_{DD} = 25 V, R_L = 830 Ω, I_D = 30 mA, V_{GEN} = -5 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	15					ns
	t_r		75					ns
Turn-Off Time	$t_{d(OFF)}$		40					ns
	t_f		100					ns

NOTES: 1. T_A = 25 °C unless otherwise noted, T_C = 25 °C for ND2406B.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

ND2410 SERIES

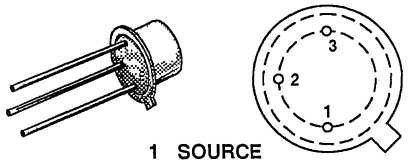
Siliconix incorporated

N-Channel Depletion-Mode MOS Transistors

TO-92 BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN

TO-205AF BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN & CASE

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSV}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
ND2410L	240	10	0.18	TO-92
ND2410B	240	10	0.46	TO-205AF

Performance Curves: **VDDV24** (See Section 7)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	ND2410L	ND2410B[2]	UNITS
Drain-Source Voltage		V_{DS}	240	240	V
Gate-Source Voltage		V_{GS}	±30	±20	V
Continuous Drain Current	T_A = 25°C	I_D	0.18	0.46	A
	T_A = 100°C		0.12	0.29	A
Pulsed Drain Current[1]		I_{DM}	0.90	1	A
Power Dissipation	T_A = 25°C	P_D	0.80	5	W
	T_A = 100°C		0.32	2	W
Operating Junction and Storage Temperature		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		°C

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	ND2410L	ND2410B	UNITS
Junction-to-Ambient	R_{thJA}	156	125	°C/W

[1]Pulse width limited by maximum junction temperature
[2]Reference case for all temperature testing

ELECTRICAL CHARACTERISTICS[1]			LIMITS					
				ND2410L		ND2410B		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Drain-Source Breakdown Voltage	$V_{(BR)DSV}$	V_{GS} = -5 V, I_D = 1 µA	260	240		240		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 5 V, I_D = 10 µA	-1.7	-0.5	-2.5	-0.5	-2.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	±0.1		±10		±10	nA
		V_{DS} = 0 V, V_{GS} = ±20 V, T_J = 125°C	±5		±50		±50	nA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 180 V, V_{GS} = -5 V	0.04		1		1	µA
		V_{DS} = 180 V, V_{GS} = -5 V, T_J = 125°C	7.5		200		200	µA
Drain Saturation Current[3]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V	120	40		40		mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 2 V, I_D = 30 mA	4.5					Ω
		V_{GS} = 0 V, I_D = 30 mA	5		10		20	Ω
		V_{GS} = 0 V, I_D = 30 mA, T_J = 125°C	10		25		25	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 30 mA	110					mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = 10 V, I_D = 30 mA	70					µS
DYNAMIC								
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = -5 V, f = 1 MHz	70		120		120	pF
Output Capacitance	C_{oss}	V_{DS} = 25 V, V_{GS} = -5 V, f = 1 MHz	20		30		30	pF
Reverse Transfer Capacitance	C_{rss}	V_{DS} = 25 V, V_{GS} = -5 V, f = 1 MHz	10		15		15	pF
SWITCHING								
Turn-On Time	$t_{d(ON)}$	V_{DD} = 25 V, R_L = 830 Ω, I_D = 30 mA, V_{GEN} = -5 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	15					ns
	t_r		75					ns
Turn-Off Time	$t_{d(OFF)}$		40					ns
	t_f		100					ns

NOTES: 1. T_A = 25 °C unless otherwise noted, T_C = 25 °C for ND2410B.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

TP0610 SERIES

Siliconix incorporated

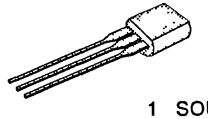
P-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

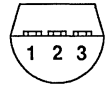
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
TP0610E	-60	10	-0.25	TO-206AC
TP0610L	-60	10	-0.18	TO-92
TP0610T	-60	10	-0.12	SOT-23

Performance Curves: **VPDS06** (See Section 7)

TO-92

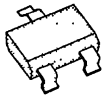


BOTTOM VIEW

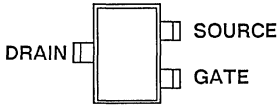


1 SOURCE
2 GATE
3 DRAIN

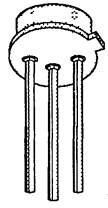
SOT-23



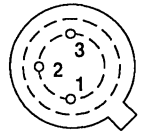
TOP VIEW



TO-206AC (TO-52)



BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN & CASE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	TP0610E[2]	TP0610L	TP0610T	UNITS
Drain-Source Voltage		V_{DS}	-60	-60	-60	V
Gate-Source Voltage		V_{GS}	±20	±30	±30	V
Continuous Drain Current	T_A = 25°C	I_D	-0.25	-0.18	-0.12	A
	T_A = 100°C		-0.15	-0.11	-0.07	A
Pulsed Drain Current[1]		I_{DM}	-1	-0.8	-0.4	A
Power Dissipation	T_A = 25°C	P_D	1.5	0.80	0.36	W
	T_A = 100°C		0.60	0.32	0.14	W
Operating Junction and Storage Temperature		T_j, T_{stg}	-55 to 150			°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300			°C

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	TP0610E	TP0610L	TP0610T	UNITS
Junction-to-Ambient	R_{thJA}	400	156	350	°C/W

[1]Pulse width limited by maximum junction temperature
[2]Reference T_C for all temperature testing

ELECTRICAL CHARACTERISTICS[1]			LIMITS					
				TP0610E		TP0610L		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = -10 µA	-70	-60		-60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA	-1.7	-1	-2.4	-1	-2.4	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	±1		±10		±10	nA
		V_{DS} = 0 V, V_{GS} = ±20 V, T_J = 125°C	±5		±50		±50	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -48 V, V_{GS} = 0 V	-0.02		-1		-1	µA
		V_{DS} = -48 V, V_{GS} = 0 V, T_J = 125°C	-0.2		-200		-200	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -4.5 V	-80	-50		-50		mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = -4.5 V, I_D = -25 mA	11		25		25	Ω
		V_{GS} = -10 V, I_D = -0.5 A	8		10		10	Ω
		V_{GS} = -10 V, I_D = -0.5 A, T_J = 125°C	15		20		20	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = -10 V, I_D = -0.5 A	135	80		80		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = -10 V, I_D = -0.1 A	400					µS
DYNAMIC								
Input Capacitance	C_{iss}	V_{DS} = -25 V, V_{GS} = 0 V, f = 1 MHz	15		60		60	pF
Output Capacitance	C_{oss}		10		25		25	pF
Reverse Transfer Capacitance	C_{rss}		3		5		5	pF
SWITCHING								
Turn-On Time	$t_{d(ON)}$	V_{DD} = -25 V, R_L = 133 Ω, I_D = -0.18 A, V_{GEN} = -10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	6		10		10	ns
	t_r		10		15		15	ns
Turn-Off Time	$t_{d(OFF)}$		7		15		15	ns
	t_f		8		20		20	ns

NOTES: 1. T_A = 25 °C unless otherwise noted, T_C = 25 °C for TP0610E.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

Siliconix incorporated

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				TP0610T		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −10 µA	−70	−60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −1 mA	−1.7	−1	−2.4	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	±1		±10	nA
		T_J = 125°C	±5		±50	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −48 V, V_{GS} = 0 V	−0.02		−1	µA
		T_J = 125°C	−0.2		−200	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = −10 V, V_{GS} = −4.5 V	−80	−50		mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = −4.5 V, I_D = −25 mA	11		25	Ω
		V_{GS} = −10 V, I_D = −0.2 A	6		10	Ω
		T_J = 125°C	12		20	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = −10 V, I_D = −0.1 A	90	60		mS
Common Source Output Conductance[3]	g_{OS}		400			µS
DYNAMIC						
Input Capacitance	C_{lss}	V_{DS} = −25 V, V_{GS} = 0 V, f = 1 MHz	15		60	pF
Output Capacitance	C_{oss}		10		25	pF
Reverse Transfer Capacitance	C_{rss}		3		5	pF
SWITCHING						
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = −25 V, R_L = 133 Ω, I_D = −0.18 A, V_{GEN} = −10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	6		10	ns
	t_r		10		15	ns
Turn-Off Delay Time	$t_{d(OFF)}$		7		15	ns
	t_f		8		20	ns

NOTES: 1. T_A = 25°C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

Siliconix incorporated

VN40AFD

N-Channel Enhancement-Mode MOS Transistor

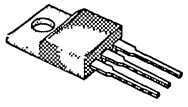
PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
40	5	1.14	TO-220SD

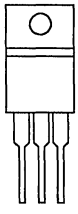
SD = Side Drain

Performance Curves: **VNDQ06** (See Section 7)

TO-220SD



TOP VIEW



1 2 3

1 SOURCE
2 GATE
3 & TAB – DRAIN

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VN40AFD	UNITS
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±30	
Continuous Drain Current	T_C = 25°C	I_D	1.14	A
	T_C = 100°C		0.72	
Pulsed Drain Current[1]		I_{DM}	3	
Power Dissipation	T_C = 25°C	P_D	15	W
	T_C = 100°C		6	
Operating Junction and Storage Temperature		T_j, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VN40AFD	UNITS
Junction-to-Case	R_{thJC}	8.3	°C/W

[1]Pulse width limited by maximum junction temperature.

VN40AFD

Siliconix incorporated

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VN40AFD		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	70	40		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.5	0.8	2.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±15 V	±1		±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V	0.05		10	µA
		V_{DS} = 32 V, V_{GS} = 0 V, T_C = 125°C	0.3		500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 15 V, V_{GS} = 10 V	1.8	1		A
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.3 A	1.8		5	Ω
		V_{GS} = 10 V, I_D = 1 A	1.3		5	Ω
		V_{GS} = 10 V, I_D = 1 A, T_C = 125°C	2.6		10	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	350	170		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = 10 V, I_D = 0.1 A	1100			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	35		50	pF
Output Capacitance	C_{oss}		25		65	pF
Reverse Transfer Capacitance	C_{rss}		5		10	pF
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	8		15	ns
Turn-Off Time	t_{OFF}		9.5		15	ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

Siliconix incorporated

VN46AFD

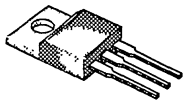
N-Channel Enhancement-Mode MOS Transistor

PRODUCT SUMMARY

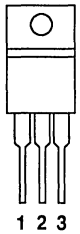
$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
40	3	1.46	TO-220SD

Performance Curves: **VNDQ06** (See Section 7)

TO-220SD



TOP VIEW



1 2 3

1 SOURCE
2 GATE
3 & TAB – DRAIN

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VN46AFD	UNITS
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±30	
Continuous Drain Current	T_C = 25°C	I_D	1.46	A
	T_C = 100°C		0.92	
Pulsed Drain Current[1]		I_{DM}	3	
Power Dissipation	T_C = 25°C	P_D	15	W
	T_C = 100°C		6	
Operating Junction and Storage Temperature		T_j, T_{stg}	–55 to 150	°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VN46AFD	UNITS
Junction-to-Case	R_{thJC}	8.3	°C/W

[1]Pulse width limited by maximum junction temperature

6

VN46AFD

Siliconix incorporated

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VN46AFD		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	70	40		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.5	0.8	2.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±15 V	± 1		±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V	0.05		10	µA
		V_{DS} = 32 V, V_{GS} = 0 V, T_C = 125°C	0.3		500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.8	1		A
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.3 A	1.8		5	Ω
		V_{GS} = 10 V, I_D = 1 A	1.3		3	Ω
		V_{GS} = 10 V, I_D = 1 A, T_C = 125°C	2.6		6	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	350	170		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = 10 V, I_D = 0.1 A	1100			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	35		50	pF
Output Capacitance	C_{oss}		25		65	pF
Reverse Transfer Capacitance	C_{rss}		5		10	pF
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	8		15	ns
Turn-Off Time	t_{OFF}		9.5		15	ns

NOTES: 1. T_C = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

VN66 SERIES

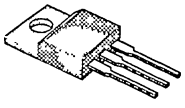
N-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

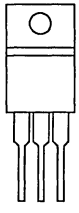
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN66AD	60	3	1.7	TO-220
VN66AFD	60	3	1.46	TO-220SD

Performance Curves: **VNDQ06** (See Section 7)

TO-220/TO-220SD



TOP VIEW



1 2 3

TO-220

1 GATE
2 & TAB – DRAIN
3 SOURCE

TO-220SD

1 SOURCE
2 GATE
3 & TAB – DRAIN

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)[2]

PARAMETERS/TEST CONDITIONS		SYMBOL	VN66AD	VN66AFD	UNITS
Drain-Source Voltage		V_{DS}	60	60	V
Gate-Source Voltage		V_{GS}	±30	±30	
Continuous Drain Current	T_C = 25°C	I_D	1.7	1.46	A
	T_C = 100°C		1	0.92	
Pulsed Drain Current[1]		I_{DM}	3	3	
Power Dissipation	T_C = 25°C	P_D	20	15	W
	T_C = 100°C		8	6	
Operating Junction and Storage Temperature		T_j, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VN66AD	VN66AFD	UNITS
Junction-to-Case	R_{thJC}	6.25	8.3	°C/W

[1]Pulse width limited by maximum junction temperature.
[2]Absolute maximum ratings have been revised.

Siliconix incorporated

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VN66[4]		
PARAMETER	SYMBOL	TEST CONDITIONS[4]	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	70	60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.5	0.8	2.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±30 V	± 1		±100	nA
		T_C = 125°C	± 5		± 500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 48 V	0.05		1	µA
		T_C = 125°C	0.3		10	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.8	1.5		A
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.3 A	1.8		5	Ω
		V_{GS} = 10 V, I_D = 1 A	1.3		3	Ω
		T_C = 125°C	2.6		6	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	350	170		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = 7.5 V, I_D = 0.1 A	1100			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	35		50	pF
Output Capacitance	C_{oss}		25		40	pF
Reverse Transfer Capacitance	C_{rss}		5		10	pF
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	8		15	ns
Turn-Off Time	t_{OFF}		9.5		15	ns

NOTES: 1. T_C = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.
4. Data sheet limits and/or test conditions have been revised.

VN67 SERIES

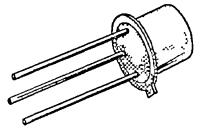
N-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

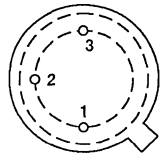
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN67AB	60	3.5	0.79	TO-205AD
VN67AD	60	3.5	1.58	TO-220
VN67AFD	60	3.5	1.37	TO-220SD

Performance Curves: **VNDQ06** (See Section 7)

TO-205AD (TO-39)



BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN & CASE

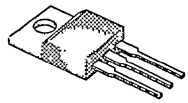
TO-220

1 GATE
2 & TAB – DRAIN
3 SOURCE

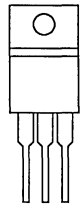
TO-220SD

1 SOURCE
2 GATE
3 & TAB – DRAIN

TO-220/TO-220SD



TOP VIEW



1 2 3

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)[2]

PARAMETERS/TEST CONDITIONS		SYMBOL	VN67AB	VN67AD	VN67AFD	UNITS
Drain-Source Voltage		V_{DS}	60	60	60	V
Gate-Source Voltage		V_{GS}	±20	±30	±30	V
Continuous Drain Current	T_C = 25°C	I_D	0.79	1.58	1.37	A
	T_C = 100°C		0.5	1	0.87	A
Pulsed Drain Current[1]		I_{DM}	3	3	3	A
Power Dissipation	T_C = 25°C	P_D	5	20	15	W
	T_C = 100°C		2	8	6	W
Operating Junction and Storage Temperature		T_j, T_{stg}	-55 to 150			°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300			°C

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VN67AB	VN67AD	VN67AFD	UNITS
Junction-to-Case	R_{thJC}	25	6.25	8.3	°C/W

[1] Pulse width limited by maximum junction temperature
[2] Absolute maximum ratings have been revised from previous data sheet

Siliconix incorporated

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VN67[4]		
PARAMETER	SYMBOL	TEST CONDITIONS[4]	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	70	60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.5	0.8	2.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±15 V	± 1		±100	nA
		V_{DS} = 0 V, V_{GS} = ±15 V, T_C = 125°C	± 5		±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 60 V	0.05		10	µA
		V_{GS} = 0 V, V_{DS} = 48 V, T_C = 125°C	0.3		500	µA
On-State Drain Current[3]	I_D	V_{DS} = 10 V, V_{GS} = 10 V	1.8	1.5		A
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.3 A	1.8		5	Ω
		V_{GS} = 10 V, I_D = 1 A	1.3		3.5	Ω
		V_{GS} = 10 V, I_D = 1 A, T_C = 125°C	2.6		7	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	350	170		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = 7.5 V, I_D = 0.1 A	1100			µS
DYNAMIC						
Input Capacitance	C_{lss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	35		50	pF
Output Capacitance	C_{oss}		25		40	pF
Reverse Transfer Capacitance	C_{rss}		5		10	pF
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	8		15	ns
Turn-Off Time	t_{OFF}		9.5		15	ns

NOTES: 1. T_C = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤2%.
4. Data sheet limits and/or test conditions have been revised.

Siliconix incorporated

VN88 SERIES

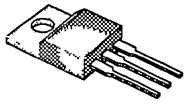
N-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

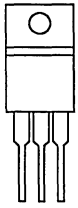
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN88AD	80	4	1.49	TO-220
VN88AFD	80	4	1.29	TO-220SD

Performance Curves: **VNDQ09** (See Section 7)

TO-220/TO-220SD



TOP VIEW



1 2 3

TO-220

1 GATE
2 & TAB – DRAIN
3 SOURCE

TO-220SD

1 SOURCE
2 GATE
3 & TAB – DRAIN

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted) [2]

PARAMETERS/TEST CONDITIONS		SYMBOL	VN88AD	VN88AFD	UNITS
Drain-Source Voltage		V_{DS}	80	80	V
Gate-Source Voltage		V_{GS}	±30	±30	
Continuous Drain Current	T_C = 25°C	I_D	1.49	1.29	A
	T_C = 100°C		0.94	0.81	
Pulsed Drain Current [1]		I_{DM}	3	3	
Power Dissipation	T_C = 25°C	P_D	20	15	W
	T_C = 100°C		8	6	
Operating Junction and Storage Temperature		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VN88AD	VN88AFD	UNITS
Junction-to-Case	R_{thJC}	6.25	8.3	°C/W

[1] Pulse width limited by maximum junction temperature
[2] Absolute maximum ratings have been revised from previous data sheet

6

Siliconix incorporated

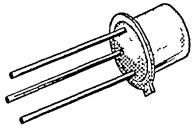
ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VN88[4]		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	120	80		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.6	0.8	2.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±15 V	± 1		± 100	nA
		V_{DS} = 0 V, V_{GS} = ±15 V, T_C = 125°C	± 5		± 500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 80 V	0.03		10	µA
		V_{GS} = 0 V, V_{DS} = 64 V, T_C = 125°C	0.3		500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.8	1.5		A
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.3 A	4.2		5.6	Ω
		V_{GS} = 10 V, I_D = 1 A	3.6		4	Ω
		V_{GS} = 10 V, I_D = 1 A, T_C = 125°C	6.8		8	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	350	170		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = 7.5 V, I_D = 0.1 A	225			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	35		50	pF
Output Capacitance	C_{oss}		15		40	pF
Reverse Transfer Capacitance	C_{rss}		2		10	pF
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	6		15	ns
Turn-Off Time	t_{OFF}		8		15	ns

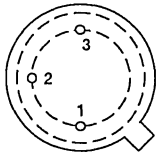
NOTES: 1. T_C = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.
4. Data sheet limits have been revised.

VN90AB

N-Channel Enhancement-Mode MOS Transistor

TO-205AD (TO-39) BOTTOM VIEW





1 SOURCE
2 GATE
3 DRAIN

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
90	5	0.67	TO-205AD

Performance Curves: **VNDQ09** (See Section 7)

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)[2]

PARAMETERS/TEST CONDITIONS		SYMBOL	VN90AB	UNITS
Drain-Source Voltage		V_{DS}	90	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	0.67	A
	T_C = 100°C		0.42	
Pulsed Drain Current[1]		I_{DM}	2	
Power Dissipation	T_C = 25°C	P_D	5	W
	T_C = 100°C		2	
Operating Junction Temperature		T_j	-55 to 150	°C
Storage Temperature		T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

THERMAL RESISTANCE[2]

THERMAL RESISTANCE	SYMBOL	VN90AB	UNITS
Junction-to-Ambient	R_{thJC}	25	°C/W

[1] Pulse width limited by maximum junction temperature
[2] Absolute maximum ratings have been revised from previous datasheet

Siliconix incorporated

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VN90AB		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	120	90		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.6	0.8	2	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±15	±1		±100	nA
		V_{DS} = 0 V, V_{GS} = ±15, T_C = 125°C	±5		±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 90 V	0.03		10	µA
		V_{GS} = 0 V, V_{DS} = 72 V, T_C = 125°C	0.30		500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.8	1.5		A
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.3A	4.2		5.3	Ω
		V_{GS} = 10 V, I_D = 1 A	3.6		5	Ω
		V_{GS} = 10 V, I_D = 1 A, [4]T_C = 125°C	6.8		10	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	350	170		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = 10 V, I_D = 0.5 A	300			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	35		50	pF
Output Capacitance	C_{oss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	15		40	pF
Reverse Transfer Capacitance	C_{rss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	2		10	pF
SWITCHING						
Turn-On Delay Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A, V_{GEN} = 0 to 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	6		10	ns
Turn-Off Delay Time	t_{OFF}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A, V_{GEN} = 0 to 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	8		10	ns

NOTES:
1. T_C = 25°C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.
4. This parameter has been revised from previous datasheet.

VN0300 SERIES

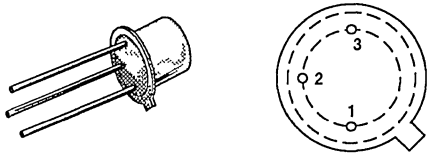
N-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN0300B	30	1.2	1.51	TO-205AD
VN0300L	30	1.2	0.64	TO-92
VN0300M	30	1.2	0.67	TO-237

Performance Curves: VNDQ03 (See Section 7)

TO-205AD (TO-39) BOTTOM VIEW

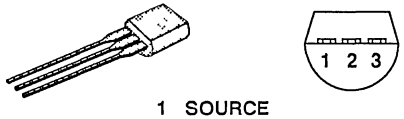


1 SOURCE
2 GATE
3 DRAIN & CASE

TO-237 BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN

TO-92 BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)[3]

PARAMETERS/TEST CONDITIONS		SYMBOL	VN0300B[2]	VN0300L	VN0300M	UNITS
Drain-Source Voltage		V_{DS}	30	30	30	V
Gate-Source Voltage		V_{GS}	±20	±30	±30	V
Continuous Drain Current	T_A = 25°C	I_D	1.51	0.64	0.67	A
	T_A = 100°C		0.95	0.38	0.43	A
Pulsed Drain Current[1]		I_{DM}	3	3	3	A
Power Dissipation	T_A = 25°C	P_D	5	0.8	1	W
	T_A = 100°C		2	0.32	0.4	W
Operating Junction and Storage Temperature		T_j, T_{stg}	-55 to 150			°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300			°C

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VN0300B	VN0300L	VN0300M	UNITS
Junction-to-Ambient	R_{thJA}	170	156	125	°C/W

[1]Pulse width limited by maximum junction temperature
[2]Reference case temperature for all testing
[3]Absolute maximum ratings have been revised from previous datasheet

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VN0300[4]		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	65	30		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.5	0.8	2.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±30 V	± 1		±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V	0.0001		10	µA
		T_C = 125°C	0.2		500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	3	1		A
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.3 A	1.4		3.3	Ω
		V_{GS} = 10 V, I_D = 1 A	0.85		1.2	Ω
		T_C = 125°C	1.8		1.65	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	500	200		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = 10 V, I_D = 0.1 A	1500			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	38		100	pF
Output Capacitance	C_{oss}		28		95	pF
Reverse Transfer Capacitance	C_{rss}		8		25	pF
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 24 Ω, I_D = 1 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	9		30	ns
Turn-Off Time	t_{OFF}		13		30	ns

NOTES: 1. T_A = 25°C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%
4. Reference case temperature for VN0300B.

VN0603 SERIES

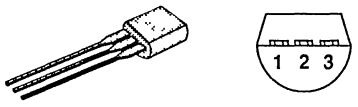
N-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN0603L	60	3.5	0.30	TO-92
VN0603T	60	3.5	0.22	SOT-23

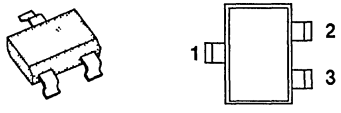
Performance Curves: **VNDS06** (See Section 7)

TO-92 BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN

SOT-23 TOP VIEW



1 DRAIN
2 SOURCE
3 GATE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VN0603L	VN0603T	UNITS
Drain-Source Voltage		V_{DS}	60	60	V
Gate-Source Voltage		V_{GS}	±30	±30	
Continuous Drain Current	T_A = 25°C	I_D	0.30	0.22	A
	T_A = 100°C		0.21	0.14	
Pulsed Drain Current[1]		I_{DM}	1	0.8	
Power Dissipation	T_A = 25°C	P_D	0.8	0.36	W
	T_A = 100°C		0.32	0.14	
Operating Junction and Storage Temperature		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VN0603L	VN0603T	UNITS
Junction-to-Ambient	R_{thJA}	156	350	°C/W

[1]Pulse width limited by maximum junction temperature

Siliconix incorporated

ELECTRICAL CHARACTERISTICS[1]			LIMITS					
				VN0603L		VN0603T		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	70	60		60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2.3	0.8	3	0.8	3	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	± 1		±100		±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V	0.02		1		1	µA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 125°C	1		500		500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1000	750		500		mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 4.5 V, I_D = 50 mA	4.5		7.5		7.5	Ω
		V_{GS} = 10 V, I_D = 0.2 A	2.5		3.5		3.5	Ω
		V_{GS} = 10 V, I_D = 0.2 A, T_J = 125°C	4.5		7		7	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A, VN0603L	230	100		100		mS
		V_{DS} = 10 V, I_D = 0.5 A, VN0603T	230	100		100		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = 10 V, I_D = 50 mA	500					µS
DYNAMIC								
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	16		60		60	pF
Output Capacitance	C_{oss}		11		40		40	pF
Reverse Transfer Capacitance	C_{rss}		2		10		10	pF
SWITCHING								
Turn-On Time	t_{ON}	V_{DD} = 15 V, R_L = 23 Ω, I_D = 0.2 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	10		15		15	ns
Turn-Off Time	t_{OFF}		10		15		15	ns

NOTES: 1. T_A = 25°C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

Siliconix incorporated

VN0605T

N-Channel Enhancement-Mode MOS Transistor

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
60	5	0.18	SOT-23

SOT-23 TOP VIEW

1 DRAIN
2 SOURCE
3 GATE

Performance Curves: **VNDS06** (See Section 7)

PRODUCT MARKING	
VN0605T	V02

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VN0605T	UNITS
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±30	
Continuous Drain Current	T_A = 25°C	I_D	0.18	A
	T_A = 100°C		0.11	
Pulsed Drain Current[1]		I_{DM}	0.72	
Power Dissipation	T_A = 25°C	P_D	0.36	W
	T_A = 100°C		0.14	
Operating Junction Temperature		T_j	−55 to 150	°C
Storage Temperature		T_{stg}	−55 to 150	
Lead Temperature (1/16" from case for 10 seconds)		T_L	300	

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VN0605T	UNITS
Junction-to-Ambient	R_{thJA}	350	°C/W

[1]Pulse width limited by maximum junction temperature

Siliconix incorporated

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VN0605T		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	70	60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2.3	0.8	3.0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	± 1		±100	nA
		T_J = 125°C	± 5		±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 50 V, V_{GS} = 0 V	0.02		1	µA
		T_J = 125°C	1		500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	700	500		mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 4.5 V, I_D = 50 mA	4.5		7.5	Ω
		V_{GS} = 10 V, I_D = 0.5 A	3		5	Ω
		T_J = 125°C	5.5		10	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.2 A	180	80		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = 10 V, I_D = 50 mA	500			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	16		60	pF
Output Capacitance	C_{oss}		11		25	pF
Reverse Transfer Capacitance	C_{rss}		2		5	pF
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 30 V, R_L = 150 Ω, I_D = 0.2 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	7		20	ns
Turn-Off Time	t_{OFF}		11		20	ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 80 µs, duty cycle ≤ 1%.

VN0610L, VN10KE, VN10KM

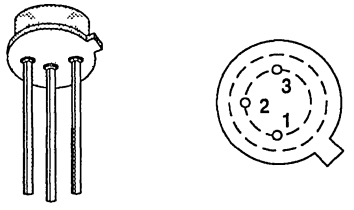
N-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN0610L	60	5	0.27	TO-92
VN10KE	60	5	0.17	TO-206AC
VN10KM	60	5	0.31	TO-237

Performance Curves: **VNDP06** (See Section 7)

TO-206AC (TO-52) BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN

TO-237 BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN & TAB

TO-92 BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VN0610L	VN10KE	VN10KM	UNITS
Drain-Source Voltage		V_{DS}	60	60	60	V
Gate-Source Voltage[2]		V_{GS}	15/–0.3	15/–0.3	15/–0.3	V
Continuous Drain Current	T_A = 25°C	I_D	0.27	0.17	0.31	A
	T_A = 100°C		0.17	0.11	0.20	A
Pulsed Drain Current[1]		I_{DM}	1	1	1	A
Power Dissipation	T_A = 25°C	P_D	0.8	0.3	1	W
	T_A = 100°C		0.32	0.12	0.4	W
Operating Junction and Storage Temperature		T_j, T_{stg}	–55 to 150			°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300			°C

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VN0610L	VN10KE	VN10KM	UNITS
Junction-to-Ambient	R_{thJA}	156	400	125	°C/W

[1] Pulse width limited by maximum junction temperature
[2] Features internal gate-source Zener diode

6

ELECTRICAL CHARACTERISTICS[1]				LIMITS		
				All		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 100 µA	120	60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.4	0.8	2.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = 15 V	1		100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V	0.7		10	µA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 125°C	3		500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1000	750		mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.2 A	4		7.5	Ω
		V_{GS} = 10 V, I_D = 0.5 A	3		5	Ω
		V_{GS} = 10 V, I_D = 0.5 A, T_J = 125°C	5.6		9	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	300	100		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = 7.5 V, I_D = 50 mA	200			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	38		60	pF
Output Capacitance	C_{oss}		16		25	pF
Reverse Transfer Capacitance	C_{rss}		2		5	pF
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 15 V, R_L = 23 Ω, I_D = 0.6 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	7		10	ns
Turn-Off Time	t_{OFF}		9		10	ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

VN0610LL, VN10LE, VN10LM

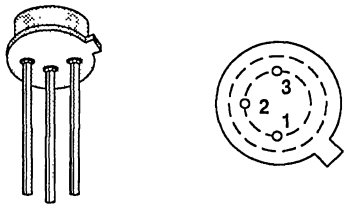
N-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN0610LL	60	5	0.28	TO-92
VN10LE	60	5	0.38	TO-206AC
VN10LM	60	5	0.32	TO-237

Performance Curves: **VNDS06** (See Section 7)

TO-206AC (TO-52) BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN & CASE

TO-237 BOTTOM VIEW

1 SOURCE
2 GATE
3 & TAB – DRAIN

TO-92 BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VN0610LL	VN10LE[2]	VN10LM	UNITS
Drain-Source Voltage		V_{DS}	60	60	60	V
Gate-Source Voltage		V_{GS}	±30	±20	±30	V
Continuous Drain Current	T_A = 25°C	I_D	0.28	0.38	0.32	A
	T_A = 100°C		0.17	0.24	0.2	A
Pulsed Drain Current[1]		I_{DM}	1.3	1	1.4	A
Power Dissipation	T_A = 25°C	P_D	0.8	1.5	1.0	W
	T_A = 100°C		0.32	0.6	0.4	W
Operating Junction and Storage Temperature		T_j, T_{stg}	–55 to 150			°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300			°C

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VN0610LL	VN10LE	VN10LM	UNITS
Junction-to-Ambient	R_{thJA}	156	400	125	°C/W

[1] Pulse width limited by maximum junction temperature
[2] Reference case for all temperature testing

Siliconix incorporated

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				ALL		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 100 µA	70	60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2.3	0.8	2.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±30 V[5]	±1		±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 50 V, V_{GS} = 0 V	0.02		10	µA
		V_{DS} = 50 V, V_{GS} = 0 V, T_J = 125°C	1		500	
On-State Drain Current[4]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1000	750		mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.2 A	5		7.5	Ω
		V_{GS} = 10 V, I_D = 0.5 A	2.5		5	Ω
		V_{GS} = 10 V, I_D = 0.5 A, T_J = 125°C	4.4		9	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	230	100		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = 5 V, I_D = 50 mA	500			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	16		60	pF
Output Capacitance	C_{oss}		11		25	pF
Reverse Transfer Capacitance	C_{rss}		2		5	pF
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 15 V, R_L = 23 Ω, I_D = 0.6 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	7		10	ns
Turn-Off Time	t_{OFF}		7		10	ns

NOTES:
1. T_A = 25 °C unless otherwise noted, T_C = 25 °C for VN10LE.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.
4. Pulse width limited by maximum junction temperature.
5. V_{GS} = ±20 V for VN10LE.

VN0808 SERIES

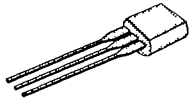
N-Channel Enhancement-Mode MOS Transistors

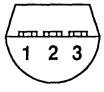
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN0808L	80	4	0.30	TO-92
VN0808M	80	4	0.33	TO-237

Performance Curves: **VNDQ09** (See Section 7)

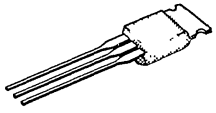
TO-92 BOTTOM VIEW

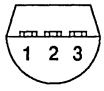




1 SOURCE
2 GATE
3 DRAIN

TO-237 BOTTOM VIEW





1 SOURCE
2 GATE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VN0808L	VN0808M	UNITS
Drain-Source Voltage		V_{DS}	80	80	V
Gate-Source Voltage		V_{GS}	±30	±30	
Continuous Drain Current [2]	T_A = 25°C	I_D	0.30	0.33	A
	T_A = 100°C		0.19	0.21	
Pulsed Drain Current [1, 2]		I_{DM}	1.9	1.9	
Power Dissipation	T_A = 25°C	P_D	0.8	1	W
	T_A = 100°C		0.32	0.4	
Operating Junction and Storage Temperature		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VN0808L	VN0808M	UNITS
Junction-to-Ambient	R_{thJA}	156	125	°C/W

[1] Pulse width limited by maximum junction temperature
[2] This parameter has been revised from previous datasheet

Siliconix incorporated

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VN0808		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	120	80		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.6	0.8	2	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±15 V	±1		±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V	0.03		10	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 125°C	0.3		500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.8	1.5		A
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.3 A	4.2			Ω
		V_{GS} = 10 V, I_D = 1 A	3.6		4	Ω
		V_{GS} = 10 V, I_D = 1 A, [4]T_J = 125°C	6.8		8	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	350	170		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = 10 V, I_D = 0.1 A	225			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	35		50	pF
Output Capacitance	C_{oss}		15		40	pF
Reverse Transfer Capacitance	C_{rss}		2		10	pF
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	6		10	ns
Turn-Off Time	t_{OFF}		8		10	ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.
4. This parameter has been revised from previous datasheet.

VN1206B, VN1206D

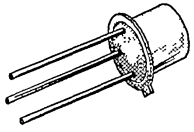
N-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

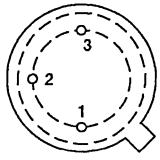
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN1206B	120	6	0.59	TO-205AD
VN1206D	120	6	1.19	TO-220

Performance Curves: **VNDQ12** (See Section 7)

TO-205AD (TO-39)

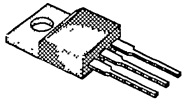


BOTTOM VIEW

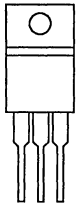


1 SOURCE
2 GATE
3 DRAIN & CASE

TO-220



TOP VIEW



1 2 3

1 GATE
2 & TAB – DRAIN
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)[2]

PARAMETERS/TEST CONDITIONS		SYMBOL	VN1206B	VN1206D	UNITS
Drain-Source Voltage		V_{DS}	120	120	V
Gate-Source Voltage		V_{GS}	±20	±30	
Continuous Drain Current	T_C = 25°C	I_D	0.59	1.19	A
	T_C = 100°C		0.37	0.75	
Pulsed Drain Current[1]		I_{DM}	2.5	2.5	
Power Dissipation	T_C = 25°C	P_D	5	20	W
	T_C = 100°C		2	8	
Operating Junction and Storage Temperature		T_j, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VN1206B	VN1206D	UNITS
Junction-to-Case	R_{thJC}	25	6.25	°C/W

[1]Pulse width limited by maximum junction temperature
[2]Absolute maximum ratings have been revised from previous data sheet

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VN1206		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 100 µA	145	120		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.4	0.8	2	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±15 V	±1		±100	nA
		T_C = 125°C	±5		±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 120 V, V_{GS} = 0 V	0.001		10	µA
		T_C = 125°C	0.5		500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.6	1		A
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 2.5 V, I_D = 0.1 A	6		10	Ω
		V_{GS} = 10 V, I_D = 0.5 V	3.4		6	Ω
		T_C = 125°C	7		14.8	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	425	300		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = 7.5 V, I_D = 0.1 A	400			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	35		125	pF
Output Capacitance	C_{oss}		15		50	pF
Reverse Transfer Capacitance	C_{rss}		2		20	pF
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = 60 V, R_L = 150 Ω, I_D = 0.4 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	3		8	ns
	t_r		2.5		8	ns
Turn-Off Time	$t_{d(OFF)}$		7		18	ns
	t_f		2.5		12	ns

NOTES: 1. T_C = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

VN1206L, VN1206M

N-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN1206L	120	6	0.23	TO-92
VN1206M	120	6	0.26	TO-237

Performance Curves: **VNDQ12** (See Section 7)

TO-92 BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN

TO-237 BOTTOM VIEW

1 SOURCE
2 GATE
3 & TAB – DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VN1206L	VN1206M	UNITS
Drain-Source Voltage		V_{DS}	120	120	V
Gate-Source Voltage		V_{GS}	±30	±30	
Continuous Drain Current	T_A = 25°C	I_D	0.23	0.26	A
	T_A = 100°C		0.15	0.16	
Pulsed Drain Current[1]		I_{DM}	2	2	
Power Dissipation	T_A = 25°C	P_D	0.8	1	W
	T_A = 100°C		0.32	0.40	
Operating Junction and Storage Temperature		T_j, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VN1206L	VN1206M	UNITS
Junction-to-Ambient	R_{thJA}	156	125	°C/W

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VN1206		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 100 µA	145	120		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.4	0.8	2	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±15 V	± 1		± 100	nA
		V_{DS} = 0 V, V_{GS} = ±15 V, T_J = 125°C	± 5		± 500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 120 V, V_{GS} = 0 V	0.001		10	µA
		V_{DS} = 120 V, V_{GS} = 0 V, T_J = 125°C	0.5		500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.6	1		A
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 2.5 V, I_D = 0.1 A	6		10	Ω
		V_{GS} = 10 V, I_D = 0.5 A	3.4		6	Ω
		V_{GS} = 10 V, I_D = 0.5 A, T_J = 125°C	7		14.8	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	425	300		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = 7.5 V, I_D = 0.1 A	400			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	35		125	pF
Output Capacitance	C_{oss}		15		50	pF
Reverse Transfer Capacitance	C_{rss}		2		20	pF
Turn-On Time	$t_{d(ON)}$	V_{DD} = 60 V, R_L = 150 Ω, I_D = 0.4 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	3		8	ns
	t_r		2.5		8	ns
Turn-Off Time	$t_{d(OFF)}$		7		18	ns
	t_f		2.5		12	ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

VN1210 SERIES

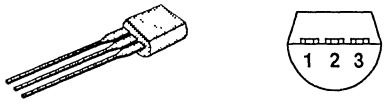
N-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN1210L	120	10	0.18	TO-92
VN1210M	120	10	0.20	TO-237

Performance Curves: **VNDQ12** (See Section 7)

TO-92 BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN

TO-237 BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN & TAB

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VN1210L	VN1210M	UNITS
Drain-Source Voltage		V_{DS}	120	120	V
Gate-Source Voltage		V_{GS}	±30	±30	
Continuous Drain Current	T_A = 25°C	I_D	0.18	0.20	A
	T_A = 100°C		0.11	0.13	
Pulsed Drain Current[1]		I_{DM}	2	2	
Power Dissipation	T_A = 25°C	P_D	0.8	1	W
	T_A = 100°C		0.32	0.40	
Operating Junction and Storage Temperature		T_j, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VN1210L	VN1210M	UNITS
Junction-to-Ambient	R_{thJA}	156	125	°C/W

[1]Pulse width limited by maximum junction temperature

Siliconix incorporated

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VN1210		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 100 µA	145	120		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.4	0.8	2.0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±15 V	± 1		±100	nA
		V_{DS} = 0 V, V_{GS} = ±15 V, T_J = 125°C	± 5		±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 120 V, V_{GS} = 0 V	0.001		10	µA
		V_{DS} = 120 V, V_{GS} = 0 V, T_J = 125°C	0.5		500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.6	1		A
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 2.5 V, I_D = 0.1 A	6		10	Ω
		V_{GS} = 10 V, I_D = 0.5 A	3.4		10	Ω
		V_{GS} = 10 V, I_D = 0.5 A, T_J = 125°C	7		24.7	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	425	300		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = 7.5 V, I_D = 0.1 A	400			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	35		125	pF
Output Capacitance	C_{oss}		15		50	pF
Reverse Transfer Capacitance	C_{rss}		2		20	pF
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = 60 V, R_L = 150 Ω, I_D = 0.4 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	3		8	ns
	t_r		2.5		8	ns
Turn-Off Time	$t_{d(OFF)}$		7		18	ns
	t_f		2.5		12	ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

VN1706B, VN1706D

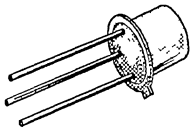
N-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

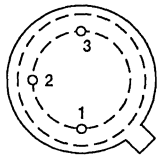
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN1706B	170	6	0.63	TO-205AD
VN1706D	170	6	1.12	TO-220

Performance Curves: **VNDB24** (See Section 7)

TO-205AD (TO-39)

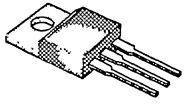


BOTTOM VIEW

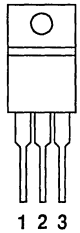


1 SOURCE
2 GATE
3 DRAIN & CASE

TO-220



TOP VIEW



1 2 3

1 GATE
2 & TAB – DRAIN
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VN1706B	VN1706D	UNITS
Drain-Source Voltage		V_{DS}	170	170	V
Gate-Source Voltage		V_{GS}	±20	±30	
Continuous Drain Current	T_C = 25°C	I_D	0.63	1.12	A
	T_C = 100°C		0.4	0.7	
Pulsed Drain Current[1]		I_{DM}	3	3	
Power Dissipation	T_C = 25°C	P_D	6.25	20	W
	T_C = 100°C		2.5	8	
Operating Junction and Storage Temperature		T_j, T_{stg}	–55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VN1706B	VN1706D	UNITS
Junction-to-Ambient	R_{thJA}	170	80	°C/W

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VN1706		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 100 µA	230	170		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.4	0.8	2.0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±15 V	±1		±100	nA
		T_C = 125°C	±5		±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 120 V, V_{GS} = 0 V	0.01		10	µA
		T_C = 125°C	1		500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.5	1		A
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 2.5 V, I_D = 0.1 A	7.5		10	Ω
		V_{GS} = 10 V, I_D = 0.5 V	5		6	Ω
		T_C = 125°C	10.8		14.8	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	530	300		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = 7.5 V, I_D = 0.5 A	475			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	105		125	pF
Output Capacitance	C_{oss}		25		50	pF
Reverse Transfer Capacitance	C_{rss}		5		20	pF
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = 60 V, R_L = 150 Ω, I_D = 0.4 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	3		8	ns
	t_r		2		8	ns
Turn-Off Time	$t_{d(OFF)}$		13		18	ns
	t_f		9		12	ns

NOTES: 1. T_C = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

VN1706L, VN1706M

N-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN1706L	170	6	0.22	TO-92
VN1706M	170	6	0.25	TO-237

Performance Curves: **VNDB24** (See Section 7)

TO-92 BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN

TO-237 BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VN1706L	VN1706M	UNITS
Drain-Source Voltage		V_{DS}	170	170	V
Gate-Source Voltage		V_{GS}	±30	±30	
Continuous Drain Current	T_A = 25°C	I_D	0.22	0.25	A
	T_A = 100°C		0.14	0.16	
Pulsed Drain Current[1]		I_{DM}	2.3	2.5	
Power Dissipation	T_A = 25°C	P_D	0.8	1.0	W
	T_A = 100°C		0.32	0.4	
Operating Junction and Storage Temperature		T_j, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VN1706L	VN1706M	UNITS
Junction-to-Ambient	R_{thJA}	156	125	°C/W

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VN1706		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 100 µA	230	170		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.4	0.8	2.0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±15 V	± 1		±100	nA
		T_J = 125°C	± 5		±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 120 V, V_{GS} = 0 V	0.01		10	µA
		T_J = 125°C	1		500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.2	1		A
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 2.5 V, I_D = 0.1 A	7.5		10	Ω
		V_{GS} = 10 V, I_D = 0.5 V	5		6	Ω
		T_J = 125°C	10.8		14.8	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	530	300		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = 7.5 V, I_D = 0.5 A	475			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	105		125	pF
Output Capacitance	C_{oss}		25		50	pF
Reverse Transfer Capacitance	C_{rss}		5		20	pF
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = 60 V, R_L = 150 Ω, I_D = 0.1 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	3		8	ns
	t_r		2		8	ns
Turn-Off Time	$t_{d(OFF)}$		13		18	ns
	t_f		9		12	ns

NOTES: 1. T_A = 25°C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

VN1710 SERIES

N-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN1710L	170	10	0.17	TO-92
VN1710M	170	10	0.19	TO-237

Performance Curves: **VNDB24** (See Section 7)

TO-92 BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN

TO-237 BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VN1710L	VN1710M	UNITS
Drain-Source Voltage		V_{DS}	170	170	V
Gate-Source Voltage		V_{GS}	±30	±30	
Continuous Drain Current	T_A = 25°C	I_D	0.17	0.19	A
	T_A = 100°C		0.11	0.12	
Pulsed Drain Current[1]		I_{DM}	0.47	0.54	
Power Dissipation	T_A = 25°C	P_D	0.8	1.0	W
	T_A = 100°C		0.32	0.4	
Operating Junction and Storage Temperature		T_j, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VN1710L	VN1710M	UNITS
Junction-to-Ambient	R_{thJA}	156	125	°C/W

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VN1710		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 100 µA	230	170		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.4	0.8	2.0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±15 V	±1		±100	nA
		T_J = 125°C	±5			nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 120 V, V_{GS} = 0 V	0.01		10	µA
		T_J = 125°C	1		500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.2	1		A
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 2.5 V, I_D = 0.1 A	8.5		10	Ω
		V_{GS} = 10 V, I_D = 0.5 A	6.5		10	Ω
		T_J = 125°C	14		24.7	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	530	300		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = 7.5 V, I_D = 0.5 A	475			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	110		125	pF
Output Capacitance	C_{oss}		30		50	pF
Reverse Transfer Capacitance	C_{rss}		5		20	pF
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = 60 V, R_L = 150 Ω, I_D = 0.4 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	3		8	ns
	t_r		2		8	ns
Turn-Off Time	$t_{d(OFF)}$		13		23	ns
	t_f		9		34	ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

VN2010 SERIES

N-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN2010L	200	10	0.19	TO-92
VN2020L	200	20	0.08	TO-92

TO-92 BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN

Performance Curves: **VNDQ20** (See Section 7)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VN2010L	VN2020L	UNITS
Drain-Source Voltage		V_{DS}	200	200	V
Gate-Source Voltage		V_{GS}	±30	±30	
Continuous Drain Current	T_A = 25°C	I_D	0.19	0.08	A
	T_A = 100°C		0.12	0.055	
Pulsed Drain Current[1]		I_{DM}	0.8	0.5	
Power Dissipation	T_A = 25°C	P_D	0.8	0.8	W
	T_A = 100°C		0.32	0.32	
Operating Junction and Storage Temperature		T_j, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VN2010L	VN2020L	UNITS
Junction-to-Ambient	R_{thJA}	156	156	°C/W

[1]Pulse width limited by maximum junction temperature

Siliconix incorporated

ELECTRICAL CHARACTERISTICS[1]			LIMITS					
				VN2010L		VN2020L		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 100 µA	220	200		200		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.3	0.8	1.8	0.8	2	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	± 1		±10		±10	nA
		V_{DS} = 0 V, V_{GS} = ±20 V, T_J = 125°C	± 5					nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 160 V, V_{GS} = 0 V	0.001		1		1	µA
		V_{DS} = 160 V, V_{GS} = 0 V, T_J = 125°C	1		100		100	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	700	100		100		mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 4.5 V, I_D = 50 mA	7		10		20	Ω
		V_{GS} = 4.5 V, I_D = 50 mA, T_J = 125°C	12.5		20		40	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 15 V, I_D = 100 mA	180	125		125		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = 15 V, I_D = 50 mA	150					µS
DYNAMIC								
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	35		60		60	pF
Output Capacitance	C_{oss}		9		30		30	pF
Reverse Transfer Capacitance	C_{rss}		1		15		15	pF
SWITCHING[4]								
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 250 Ω, I_D = 100 mA, V_{GEN} = 10 V, R_G = 25 Ω	5		20		20	ns
Turn-Off Time	t_{OFF}		21		30		30	ns

NOTES:
1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%
4. Switching time is essentially independent of operating temperature.

VN2222KM, VN2222L

N-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

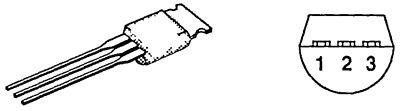
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN2222KM	60	7.5	0.25	TO-237
VN2222L	60	7.5	0.23	TO-92

Performance Curves: **VNDP06** (See Section 7)

TO-92 BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN

TO-237 BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VN2222KM	VN2222L	UNITS
Drain-Source Voltage		V_{DS}	60	60	V
Gate-Source Voltage[2]		V_{GS}	+15, −0.3	+15, −0.3	V
Continuous Drain Current	T_A = 25°C	I_D	0.25	0.23	A
	T_A = 100°C		0.16	0.14	A
Pulsed Drain Current[1]		I_{DM}	1	1	A
Power Dissipation	T_A = 25°C	P_D	1	0.8	W
	T_A = 100°C		0.4	0.32	W
Operating Junction and Storage Temperature		T_j, T_{stg}	−55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		°C

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VN2222KM	VN2222L	UNITS
Junction-to-Ambient	R_{thJA}	125	156	°C/W

[1] Pulse width limited by maximum junction temperature
[2] Features internal gate-source zener diode

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VN2222		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 100 µA	120	60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.3	0.6	2.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = 15 V	1		100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V	0.7		10	µA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 125°C	3		500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1000	750		mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.2 A	4		7.5	Ω
		V_{GS} = 10 V, I_D = 0.5 A	3		7.5	Ω
		V_{GS} = 10 V, I_D = 0.5 A, T_J = 125°C	5.6		13.5	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	300	100		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = 7.5 V, I_D = 50 mA	200			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	38		60	pF
Output Capacitance	C_{oss}		16		25	pF
Reverse Transfer Capacitance	C_{rss}		2		5	pF
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 15 V, R_L = 23 Ω, I_D = 0.6 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	7		10	ns
Turn-Off Time	t_{OFF}		9		10	ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%

VN2222LL, VN2222LM

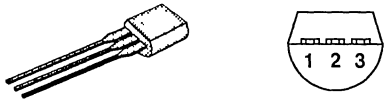
N-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN2222LL	60	7.5	0.23	TO-92
VN2222LM	60	7.5	0.26	TO-237

Performance Curves: **VNDS06** (See Section 7)

TO-92 BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN

TO-237 BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VN2222LL	VN2222LM	UNITS
Drain-Source Voltage		V_{DS}	60	60	V
Gate-Source Voltage		V_{GS}	±30	±30	
Continuous Drain Current	T_A = 25°C	I_D	0.23	0.26	A
	T_A = 100°C		0.14	0.16	
Pulsed Drain Current[1]		I_{DM}	1	1	
Power Dissipation	T_A = 25°C	P_D	0.8	1	W
	T_A = 100°C		0.32	0.4	
Operating Junction and Storage Temperature		T_j, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VN2222LL	VN2222LM	UNITS
Junction-to-Ambient	R_{thJA}	156	125	°C/W

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VN2222		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 100 µA	70	60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2.3	0.6	2.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	±1		±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V	0.02		10	µA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 125°C	1		500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1000	750		mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.2 A	5		7.5	Ω
		V_{GS} = 10 V, I_D = 0.5 A	2.5		7.5	Ω
		V_{GS} = 10 V, I_D = 0.5 A, T_J = 125°C	4.4		13.5	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	230	100		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = 10 V, I_D = 0.2 A	1200			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	16		60	pF
Output Capacitance	C_{oss}		11		25	pF
Reverse Transfer Capacitance	C_{rss}		2		5	pF
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 15 V, R_L = 23 Ω, I_D = 0.6 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	7		10	ns
Turn-Off Time	t_{OFF}		7		10	ns

NOTES: 1. T_A = 25°C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

VN2406B, VN2406D

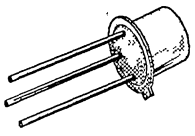
N-Channel Enhancement-Mode MOS Transistors

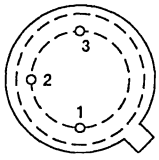
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN2406B	240	6	0.63	TO-205AD
VN2406D	240	6	1.12	TO-220

Performance Curves: **VNDB24** (See Section 7)

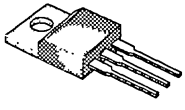
TO-205AD (TO-39) BOTTOM VIEW

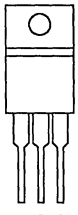




1 SOURCE
2 GATE
3 DRAIN & CASE

TO-220 FRONT VIEW





1 GATE
2 & TAB – DRAIN
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VN2406B	VN2406D	UNITS
Drain-Source Voltage		V_{DS}	240	240	V
Gate-Source Voltage		V_{GS}	±20	±30	
Continuous Drain Current	T_C = 25°C	I_D	0.63	1.12	A
	T_C = 100°C		0.4	0.7	
Pulsed Drain Current[1]		I_{DM}	3	3	
Power Dissipation	T_C = 25°C	P_D	6.25	20	W
	T_C = 100°C		2.5	8	
Operating Junction and Storage Temperature		T_j, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VN2406B	VN2406D	UNITS
Junction-to-Case	R_{thJC}	20	6.25	°C/W

[1]Pulse width limited by maximum junction temperature

Siliconix incorporated

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VN2406		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 100 µA	270	240		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.4	0.8	2.0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±15 V	±1		±100	nA
		T_C = 125°C	±5		±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 120 V, V_{GS} = 0 V	0.01		10	µA
		T_C = 125°C	1		500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.5	1		A
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 2.5 V, I_D = 0.1 A	7.5		10	Ω
		V_{GS} = 10 V, I_D = 0.5 V	5		6	Ω
		T_C = 125°C	10.8		14.8	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	530	300		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = 7.5 V, I_D = 0.5 A	475			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	110		125	pF
Output Capacitance	C_{oss}		30		50	pF
Reverse Transfer Capacitance	C_{rss}		5		20	pF
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = 60 V, R_L = 150 Ω, I_D = 0.4 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	3		8	ns
	t_r		2		8	ns
Turn-Off Time	$t_{d(OFF)}$		13		17	ns
	t_f		9		12	ns

NOTES: 1. T_C = 25°C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%

VN2406L, VN2406M

N-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

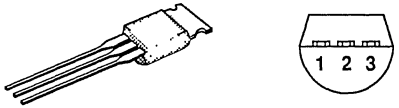
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN2406L	240	6	0.22	TO-92
VN2406M	240	6	0.25	TO-237

Performance Curves: **VNDB24** (See Section 7)

TO-92 BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN

TO-237 BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VN2406L	VN2406M	UNITS
Drain-Source Voltage		V_{DS}	240	240	V
Gate-Source Voltage		V_{GS}	±30	±30	
Continuous Drain Current	T_A = 25°C	I_D	0.17	0.19	A
	T_A = 100°C		0.11	0.12	
Pulsed Drain Current[1]		I_{DM}	1.7	2	
Power Dissipation	T_A = 25°C	P_D	0.8	1	W
	T_A = 100°C		0.32	0.4	
Operating Junction and Storage Temperature		T_j, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VN2406L	VN2406M	UNITS
Junction-to-Ambient	R_{thJA}	156	125	°C/W

[1]Pulse width limited by maximum junction temperature

Siliconix incorporated

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VN2406		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 100 µA	270	240		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.4	0.8	2	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±15 V	±1		±100	nA
		T_J = 125°C	±5		±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 120 V, V_{GS} = 0 V	0.01		10	µA
		T_J = 125°C	1		500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 15 V, V_{GS} = 10 V	1.5	1		A
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 2.5 V, I_D = 0.1 A	7.5		10	Ω
		V_{GS} = 10 V, I_D = 0.5 A	5		10	Ω
		T_J = 125°C	10.8		24.7	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	530	300		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = 7.5 V, I_D = 0.5 A	475			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	110		125	pF
Output Capacitance	C_{oss}		30		50	pF
Reverse Transfer Capacitance	C_{rss}		5		20	pF
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = 60 V, R_L = 150 Ω, I_D = 0.4 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	3		8	ns
	t_r		2		8	ns
Turn-Off Time	$t_{d(OFF)}$		13		23	ns
	t_f		9		34	ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

VN2410 SERIES

N-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

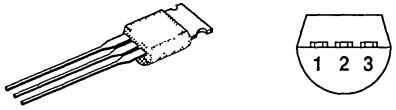
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN2410L	240	10	0.17	TO-92
VN2410M	240	10	0.19	TO-237

Performance Curves: **VNDB24** (See Section 7)

TO-92 BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN

TO-237 BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VN2410L	VN2410M	UNITS
Drain-Source Voltage		V_{DS}	240	240	V
Gate-Source Voltage		V_{GS}	±30	±30	
Continuous Drain Current	T_A = 25°C	I_D	0.17	0.19	A
	T_A = 100°C		0.11	0.12	
Pulsed Drain Current[1]		I_{DM}	1.7	2	
Power Dissipation	T_A = 25°C	P_D	0.8	1	W
	T_A = 100°C		0.32	0.4	
Operating Junction and Storage Temperature		T_j, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VN2410L	VN2410M	UNITS
Junction-to-Ambient	R_{thJA}	156	125	°C/W

[1]Pulse width limited by maximum junction temperature

Siliconix incorporated

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VN2410		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 100 µA	270	240		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.4	0.8	2	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±15 V	±1		±100	nA
		T_J = 125°C	±5			nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 120 V, V_{GS} = 0 V	0.01		10	µA
		T_J = 125°C	1		500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 15 V, V_{GS} = 10 V	1.2	1		A
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 2.5 V, I_D = 0.1 A	8.5		10	Ω
		V_{GS} = 10 V, I_D = 0.5 A	6.5		10	Ω
		T_J = 125°C	14		24.7	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	530	300		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = 7.5 V, I_D = 0.5 A	475			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	110		125	pF
Output Capacitance	C_{oss}		30		50	pF
Reverse Transfer Capacitance	C_{rss}		5		20	pF
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = 60 V, R_L = 150 Ω, I_D = 0.4 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	3		8	ns
	t_r		2		8	ns
Turn-Off Time	$t_{d(OFF)}$		13		23	ns
	t_f		9		34	ns

NOTES: 1. T_A = 25°C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

VN4012 SERIES

N-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

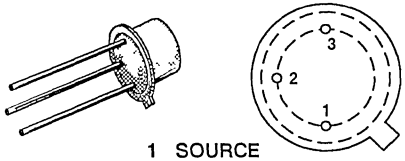
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN4012L	400	12	0.16	TO-92
VN4012B	400	12	0.42	TO-205AF
VN3515L	350	15	0.15	TO-92

Performance Curves: **VNDV40** (See Section 7)

TO-92 BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN

TO-205AF BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN & CASE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VN4012L	VN4012B[2]	VN3515L	UNITS
Drain-Source Voltage		V_{DS}	400	400	350	V
Gate-Source Voltage		V_{GS}	±30	±20	±30	
Continuous Drain Current	T_A = 25°C	I_D	0.16	0.42	0.15	A
	T_A = 100°C		0.10	0.27	0.09	
Pulsed Drain Current[1]		I_{DM}	0.65	1.3	0.60	
Power Dissipation	T_A = 25°C	P_D	0.80	5	0.80	W
	T_A = 100°C		0.32	2	0.32	
Operating Junction and Storage Temperature		T_j, T_{stg}	-55 to 150			°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300			

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VN4012L	VN4012B	VN3515L	UNITS
Junction-to-Ambient	R_{thJA}	156	125	156	°C/W

[1]Pulse width limited by maximum junction temperature
[2]Reference case for all temperature tests

Siliconix incorporated

ELECTRICAL CHARACTERISTICS[1]			LIMITS					
				VN4012		VN3515		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 100 µA	420	400		350		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.3	0.6	1.8	0.6	1.8	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	±1		±10		±10	nA
		T_J = 125°C	±5					
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V	0.002		1		1	µA
		T_J = 125°C	0.8		100		100	
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 4.5 V	300	150		150		mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 100 mA	9					Ω
		V_{GS} = 4.5 V, I_D = 100 mA	9.5		12		15	
		T_J = 125°C	17		30		35	
Forward Transconductance[3]	g_{FS}	V_{DS} = 15 V, I_D = 100 mA	350	125		125		mS
Common Source Output Conductance[3]	g_{OS}		17					µS
DYNAMIC								
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	80		90		90	pF
Output Capacitance	C_{oss}		10		20		20	
Reverse Transfer Capacitance	C_{rss}		2		5		5	
SWITCHING								
Turn-On Time	$t_{d(ON)}$	V_{DD} = 25 V, R_L = 250 Ω, I_D = 0.1 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	3.5		20		20	ns
	t_r		2		20		20	
Turn-Off Time	$t_{d(OFF)}$		25		65		65	
	t_f		15		65		65	

NOTES: 1. T_A = 25 °C unless otherwise noted, T_C = 25 °C for VN4012B.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

VN45350 SERIES

N-Channel Enhancement-Mode MOS Transistors

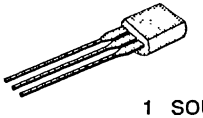
PRODUCT SUMMARY

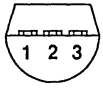
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN45350L	450	350	0.030	TO-92
VN45350T	450	350	0.020	SOT-23

Performance Curves: **VNDO50** (See Section 7)

PRODUCT MARKING	
VN45350T	V04

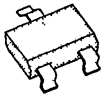
TO-92 BOTTOM VIEW

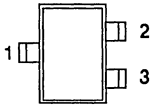




1 SOURCE
2 GATE
3 DRAIN

SOT-23 TOP VIEW





1 DRAIN
2 SOURCE
3 GATE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VN45350L	VN45350T	UNITS
Drain-Source Voltage		V_{DS}	450	450	V
Gate-Source Voltage		V_{GS}	±30	±30	
Continuous Drain Current	T_A = 25°C	I_D	0.030	0.020	A
	T_A = 100°C		0.019	0.013	
Pulsed Drain Current[1]		I_{DM}	0.12	0.08	
Power Dissipation	T_A = 25°C	P_D	0.80	0.35	W
	T_A = 100°C		0.32	0.14	
Operating Junction and Storage Temperature		T_j, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VN45350L	VN45350T	UNITS
Junction-to-Ambient	R_{thJA}	156	350	°C/W

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VN45350		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	490	450		V
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 10 µA	3.5	1.0	4.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	±1		±100	nA
		T_J = 125°C	±5		±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 250 V, V_{GS} = 0 V	0.003		0.050	µA
		T_J = 125°C	2		5	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 15 V, V_{GS} = 10 V	30	15		mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 10 mA	320		350	Ω
		V_{GS} = 10 V, I_D = 5 mA	300			Ω
		T_J = 125°C	650		820	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 15 V, I_D = 10 mA	14	5		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = 10 V, I_D = 1 mA	4.5			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	5		20	pF
Output Capacitance	C_{oss}		1.8		10	pF
Reverse Transfer Capacitance	C_{rss}		0.5		5	pF
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = 25 V, R_L = 2500 Ω, I_D = 10 mA, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	4.5		10	ns
	t_r		8		15	ns
Turn-Off Time	$t_{d(OFF)}$		15		30	ns
	t_f		60		100	ns

NOTES: 1. T_A = 25°C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

VN50300 SERIES

N-Channel Enhancement-Mode MOS Transistors

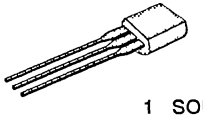
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VN50300L	500	300	0.033	TO-92
VN50300T	500	300	0.022	SOT-23

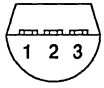
Performance Curves: **VNDO50** (See Section 7)

PRODUCT MARKING	
VN50300T	V01

TO-92

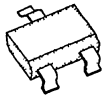


BOTTOM VIEW

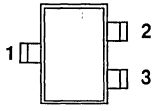


1 SOURCE
2 GATE
3 DRAIN

SOT-23



TOP VIEW



1 DRAIN
2 SOURCE
3 GATE

ABSOTUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VN50300L	VN50300T	UNITS
Drain-Source Voltage		V_{DS}	500	500	V
Gate-Source Voltage		V_{GS}	±30	±30	V
Continuous Drain Current	T_A = 25°C	I_D	0.033	0.022	A
	T_A = 100°C		0.021	0.013	A
Pulsed Drain Current[1]		I_{DM}	0.130	0.080	A
Power Dissipation	T_A = 25°C	P_D	0.80	0.35	W
	T_A = 100°C		0.32	0.14	W
Operating Junction and Storage Temperature		T_j, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		°C

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VN50300L	VN50300T	UNITS
Junction-to-Ambient	R_{thJA}	156	350	°C/W

[1]Pulse width limited by maximum junction temperature

Siliconix incorporated

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VN50300		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	520	500		V
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 10 µA	3.5	1.0	4.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	±1		±100	nA
		T_J = 125°C	±5		±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 250 V, V_{GS} = 0 V	3		50	µA
		T_J = 125°C	2		5	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	30	15		mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 10 mA	250		300	Ω
		V_{GS} = 10 V, I_D = 5 mA	240			Ω
		T_J = 125°C	525		700	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 15 V, I_D = 10 mA	14	5		mS
Common Source Output Conductance[3]	g_{OS}		4.5			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	5		20	pF
Output Capacitance	C_{oss}		1.8		10	pF
Reverse Transfer Capacitance	C_{rss}		0.5		5	pF
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = 25 V, R_L = 2500 Ω, I_D = 10 mA, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	4.5		8	ns
	t_r		8		12	ns
Turn-Off Time	$t_{d(OFF)}$		15		20	ns
	t_f		60		90	ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

VP0300 SERIES

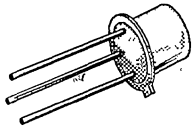
P-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

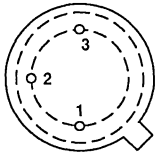
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VP0300B	-30	2.5	-1.25	TO-205AD
VP0300L	-30	2.5	-0.32	TO-92
VP0300M	-30	2.5	-0.5	TO-237

Performance Curves: **VPMH03** (See Section 7)

TO-205AD (TO-39)

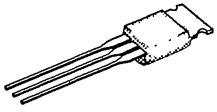


BOTTOM VIEW

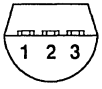


1 SOURCE
2 GATE
3 DRAIN & CASE

TO-237

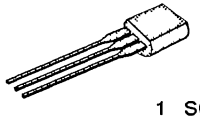


BOTTOM VIEW

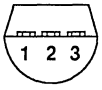


1 SOURCE
2 GATE
3 & TAB – DRAIN

TO-92



BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VP0300B[2]	VP0300L	VP0300M	UNITS
Drain-Source Voltage		V_{DS}	-30	-30	-30	V
Gate-Source Voltage		V_{GS}	±20	±30	±30	V
Continuous Drain Current	T_A = 25°C	I_D	-1.25	-0.32	-0.5	A
	T_A = 100°C		-0.79	-0.2	-0.32	A
Pulsed Drain Current[1]		I_{DM}	-3	-2.4	-3	A
Power Dissipation	T_A = 25°C	P_D	6.25	0.8	1	W
	T_A = 100°C		2.5	0.32	0.4	W
Operating Junction and Storage Temperature		T_j, T_{stg}	-55 to 150			°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300			°C

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VP0300B	VP0300L	VP0300M	UNITS
Junction-to-Ambient	R_{thJA}	170	156	125	°C/W

[1]Pulse width limited by maximum junction temperature
[2]Reference case temperature for all tests.

6

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VP0300[4]		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = -10 µA	-55	-30		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA	-3.6	-2	-4.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±30 V	±1		±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -25 V, V_{GS} = 0 V	-0.0001		-10	µA
		T_J = 125°C	-0.3		-500	µA
On-State Drain Current	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -12 V	-1.6	-1.5		A
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = -12 V, I_D = -1 A	1.8		2.5	Ω
		T_J = 125°C	3.1		3.63	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = -10 V, I_D = -0.5 A	290	200		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = -7.5 V, I_D = -0.05 A	800			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = -15 V, V_{GS} = 0 V, f = 1 MHz	130		150	pF
Output Capacitance	C_{oss}		75		100	pF
Reverse Transfer Capacitance	C_{rss}		20		60	pF
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = -25 V, R_L = 23 Ω, I_D = -1 A, V_{GEN} = -10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	16		30	ns
Turn-Off Time	t_{OFF}		13		30	ns

NOTES: 1. T_A = 25°C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.
4. Reference case temperature for VP0300B.

VP0610 SERIES

P-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

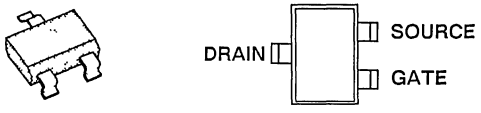
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VP0610E	-60	10	-0.25	TO-206AC
VP0610L	-60	10	-0.18	TO-92
VP0610T	-60	10	-0.12	SOT-23

Performance Curves: **VPDS06** (See Section 7)

TO-92 BOTTOM VIEW

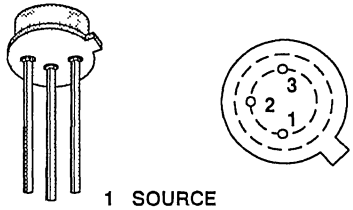
1 SOURCE
2 GATE
3 DRAIN

SOT-23 TOP VIEW



PRODUCT MARKING	
VP0610T	V50

TO-206AC (TO-52) BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN & CASE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VP0610E[2]	VP0610L	VP0610T	UNITS
Drain-Source Voltage		V_{DS}	-60	-60	-60	V
Gate-Source Voltage		V_{GS}	±20	±30	±30	V
Continuous Drain Current	T_A = 25°C	I_D	-0.25	-0.18	-0.12	A
	T_A = 100°C		-0.15	-0.11	-0.07	A
Pulsed Drain Current[1]		I_{DM}	-1	-0.8	-0.4	A
Power Dissipation	T_A = 25°C	P_D	1.5	0.80	0.36	W
	T_A = 100°C		0.6	0.32	0.14	W
Operating Junction and Storage Temperature		T_j, T_{stg}	-55 to 150			°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300			°C

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VP0610E	VP0610L	VP0610T	UNITS
Junction-to-Ambient	R_{thJA}	400	156	350	°C/W

[1]Pulse width limited by maximum junction temperature
[2]Reference T_C for all tests

ELECTRICAL CHARACTERISTICS[1]			LIMITS					
				VP0610E		VP0610L		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = -10 µA	-70	-60		-60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA	-2	-1	-3.5	-1	-3.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	±1		±10		±10	nA
		V_{DS} = 0 V, V_{GS} = ±20 V, T_J = 125°C	±5					nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -48 V, V_{GS} = 0 V	-0.02		-1		-1	µA
		V_{DS} = -48 V, V_{GS} = 0 V, T_J = 125°C	-0.2		-200		-200	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -10 V	-700	-600		-600		mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = -10 V, I_D = -0.5 A	8		10		10	Ω
		V_{GS} = -10 V, I_D = -0.5 A, T_J = 125°C	15		20		20	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = -10 V, I_D = -0.5 A	135	80		80		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = -10 V, I_D = -0.2 A	400					µS
DYNAMIC								
Input Capacitance	C_{iss}	V_{DS} = -25 V, V_{GS} = 0 V, f = 1 MHz	15		60		60	pF
Output Capacitance	C_{oss}		10		25		25	pF
Reverse Transfer Capacitance	C_{rss}		3		5		5	pF
SWITCHING								
Turn-On Time	$t_{d(ON)}$	V_{DD} = -25 V, R_L = 133 Ω, I_D = -0.18 A, V_{GEN} = -10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	6		10		10	ns
	t_r		10		15		15	ns
Turn-Off Time	$t_{d(OFF)}$		7		15		15	ns
	t_f		8		20		20	ns

NOTES: 1. T_A = 25°C unless otherwise noted, T_C = 25°C for VP0610E.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VP0610T		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = -10 µA	-70	-60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA	-2	-1	-3.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V	± 1		± 10	nA
		V_{DS} = 0 V, V_{GS} = ± 20 V, T_J = 125°C	± 5			nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -48 V, V_{GS} = 0 V	-0.02		-1	µA
		V_{DS} = -48 V, V_{GS} = 0 V, T_J = 125°C	-0.2		-200	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -10 V	-300	-220		mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = -10 V, I_D = -0.2 A	6		10	Ω
		V_{GS} = -10 V, I_D = -0.2 A, T_J = 125°C	12		20	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = -10 V, I_D = -0.1 A	90	70		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = -10 V, I_D = -0.2 A	400			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = -25 V, V_{GS} = 0 V, f = 1 MHz	15		60	pF
Output Capacitance	C_{oss}		10		25	pF
Reverse Transfer Capacitance	C_{rss}		3		5	pF
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = -25 V, R_L = 133 Ω, I_D = -0.18 A, V_{GEN} = -10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	6		10	ns
	t_r		10		15	ns
Turn-Off Time	$t_{d(OFF)}$		7		15	ns
	t_f		8		20	ns

NOTES: 1. T_A = 25°C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

VP0808 SERIES

Siliconix incorporated

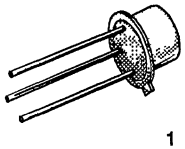
P-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

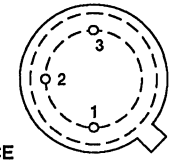
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VP0808B	–80	5	–0.88	TO-205AD
VP0808L	–80	5	–0.28	TO–92
VP0808M	–80	5	–0.31	TO-237

Performance Curves: **VPDV10** (See Section 7)

TO-205AD

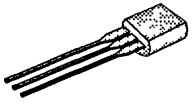


BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN & CASE

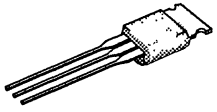
TO-92



BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN

TO-237



BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN & TAB

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)[3]

PARAMETERS/TEST CONDITIONS		SYMBOL	VP0808B[2]	VP0808L	VP0808M	UNITS
Drain-Source Voltage		V_{DS}	–80	–80	–80	V
Gate-Source Voltage		V_{GS}	±20	±30	±30	V
Continuous Drain Current	T_A = 25°C	I_D	–0.88	–0.28	–0.31	A
	T_A = 100°C		–0.53	–0.17	–0.20	A
Pulsed Drain Current[1]		I_{DM}	–3	–3	–3	A
Power Dissipation	T_A = 25°C	P_D	6.25	0.8	1	W
	T_A = 100°C		2.5	0.32	0.4	W
Operating Junction and Storage Temperature		T_J, T_{stg}	–55 to 150			°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300			°C

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VP0808B	VP0808L	VP0808M	UNITS
Junction-to-Ambient	R_{thJA}	170	156	125	°C/W

[1]Pulse width limited by maximum junction temperature
[2]Reference case temperature for all testing
[3]Absolute maximum ratings have been revised

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VP0808[4]		
PARAMETER	SYMBOL	TEST CONDITIONS[4]	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −10 µA	−110	−80		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −1 mA	−3.4	−2	−4.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	±1		±100	nA
		T_J = 125°C	±5		±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −80 V, V_{GS} = 0 V	−0.0005		−10	µA
		T_J = 125°C	−0.1		−500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = −15 V, V_{GS} = −10 V	−2	−1.1		A
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = −10 V, I_D = −1 A	2.5		5	Ω
		T_J = 125°C	4.3		8	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = −10 V, I_D = −0.5 A	325	200		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = −7.5 V, I_D = −0.1 A	450			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = −25 V, V_{GS} = 0 V, f = 1 MHz	75		150	pF
Output Capacitance	C_{oss}		40		60	pF
Reverse Transfer Capacitance	C_{rss}		18		25	pF
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = −25 V, R_L = 47 Ω, I_D = −0.5 A, V_{GEN} = −10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	11		15	ns
	t_r		30		40	ns
Turn-Off Time	$t_{d(OFF)}$		20		30	ns
	t_f		20		30	ns

NOTES: 1. T_A = 25 °C unless otherwise noted, T_C = 25 °C for VP0808B.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.
4. Data sheet limits and/or test conditions have been revised.

VP1008 SERIES

Siliconix incorporated

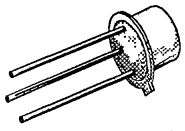
P-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

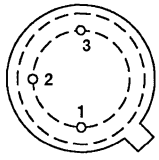
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VP1008B	–100	5	–0.79	TO-205AD
VP1008L	–100	5	–0.28	TO–92
VP1008M	–100	5	–0.31	TO-237

Performance Curves: **VPDV10** (See Section 7)

TO-205AD

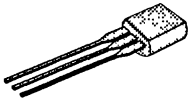


BOTTOM VIEW



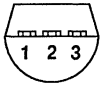
1 SOURCE
2 GATE
3 DRAIN & CASE

TO-92

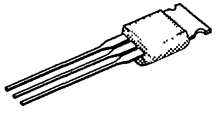


1 SOURCE
2 GATE
3 DRAIN

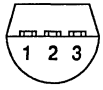
BOTTOM VIEW



TO-237



BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN & TAB

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)[3]

PARAMETERS/TEST CONDITIONS		SYMBOL	VP1008B[2]	VP1008L	VP1008M	UNITS
Drain-Source Voltage		V_{DS}	–100	–100	–100	V
Gate-Source Voltage		V_{GS}	±20	±30	±30	V
Continuous Drain Current	T_A = 25°C	I_D	–0.79	–0.28	–0.31	A
	T_A = 100°C		–0.53	–0.17	–0.20	A
Pulsed Drain Current[1]		I_{DM}	–3	–3	–3	A
Power Dissipation	T_A = 25°C	P_D	6.25	0.8	1	W
	T_A = 100°C		2.5	0.32	0.4	W
Operating Junction and Storage Temperature		T_j, T_{stg}	–55 to 150			°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300			°C

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VP1008B	VP1008L	VP1008M	UNITS
Junction-to-Ambient	R_{thJA}	170	156	125	°C/W

[1]Pulse width limited by maximum junction temperature
[2]Reference case temperature for all testing
[3]Absolute maximum ratings have been revised

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VP1008[4]		
PARAMETER	SYMBOL	TEST CONDITIONS[4]	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = -10 µA	-110	-100		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA	-3.4	-2	-4.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	±1		±100	nA
		T_J = 125°C	±5		±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -100 V, V_{GS} = 0 V	-0.0005		-10	µA
		T_J = 125°C	-0.1		-500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = -15 V, V_{GS} = -10 V	-2	-1.1		A
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = -10 V, I_D = -1 A	2.5		5	Ω
		T_J = 125°C	4.3		8	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = -10 V, I_D = -0.5 A	325	200		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = -7.5 V, I_D = -0.1 A	450			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = -25 V, V_{GS} = 0 V, f = 1 MHz	75		150	pF
Output Capacitance	C_{oss}		40		60	pF
Reverse Transfer Capacitance	C_{rss}		18		25	pF
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = -25 V, R_L = 47 Ω, I_D = -0.5 A, V_{GEN} = -10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	11		15	ns
	t_r		30		40	ns
Turn-Off Time	$t_{d(OFF)}$		20		30	ns
	t_f		20		30	ns

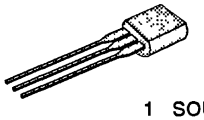
NOTES: 1. T_A = 25 °C unless otherwise noted, T_C = 25 °C for VP1008B.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.
4. Data sheet limits and/or test conditions have been revised.

VP2020 SERIES

Siliconix incorporated

P-Channel Enhancement-Mode MOS Transistors

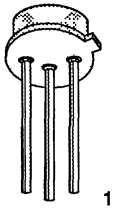
TO-92



BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN

TO-206AC (TO-52)



BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN & CASE

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VP2020L	–200	20	–0.12	TO-92
VP2020E	–200	20	–0.17	TO-206AC

Performance Curves: **VPDQ20** (See Section 7)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VP2020L	VP2020E[2]	UNITS
Drain-Source Voltage		V_{DS}	–200	–200	V
Gate-Source Voltage		V_{GS}	±30	±20	V
Continuous Drain Current	T_A = 25°C	I_D	–0.12	–0.17	A
	T_A = 100°C		–0.08	–0.10	A
Pulsed Drain Current[1]		I_{DM}	–0.48	–0.60	A
Power Dissipation	T_A = 25°C	P_D	0.80	1.50	W
	T_A = 100°C		0.32	0.60	W
Operating Junction and Storage Temperature		T_j, T_{stg}	–55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		°C

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VP2020L	VP2020E	UNITS
Junction-to-Ambient	R_{thJA}	156	400	°C/W

[1]Pulse width limited by maximum junction temperature
[2]Reference case for all temperature testing

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VP2020		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = -10 µA	-220	-200		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA	-1.9	-0.8	-2.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	±1		±10	nA
		T_J = 125°C	±5		±50	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -160, V_{GS} = 0 V	-0.02		-1	µA
		T_J = 125°C	-3		-100	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -4.5 V	-270	-100		mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = -4.5 V, I_D = -100 mA	15		20	Ω
		T_J = 125°C	27		40	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = -10 V, I_D = -100 mA	150	100		mS
Common Source Output Conductance[3]	g_{OS}		300			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = -25 V, V_{GS} = 0 V, f = 1 MHz	30		70	pF
Output Capacitance	C_{oss}		10		20	pF
Reverse Transfer Capacitance	C_{rss}		2		10	pF
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = -25 V, R_L = 250 Ω, I_D = -100 mA, V_{GEN} = -10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	6		10	ns
	t_r		8		15	ns
Turn-Off Time	$t_{d(OFF)}$		18		30	ns
	t_f		17		25	ns

NOTES: 1. T_A = 25°C unless otherwise noted, T_C = 25°C for VP2020E.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

6

VP2410 SERIES

Siliconix incorporated

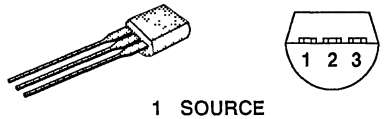
P-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VP2410L	–240	10	–0.18	TO-92
VP2410B	–240	10	–0.17	TO-205AF

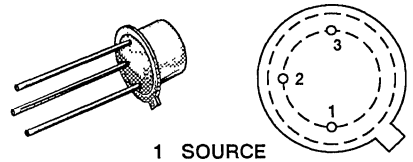
Performance Curves: **VPDV24** (See Section 7)

TO-92 BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN

TO-205AF BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN & CASE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VP2410L	VP2410B	UNITS
Drain-Source Voltage		V_{DS}	–240	–240	V
Gate-Source Voltage		V_{GS}	±30	±20	
Continuous Drain Current	T_A = 25°C	I_D	–0.18	–0.17	A
	T_A = 100°C		–0.11	–0.10	
Pulsed Drain Current[1]		I_{DM}	–0.72	–0.70	
Power Dissipation	T_A = 25°C	P_D	0.80	0.73	W
	T_A = 100°C		0.32	0.22	
Operating Junction and Storage Temperature		T_j, T_{stg}	–55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VP2410L	VP2410B	UNITS
Junction-to-Ambient	R_{thJA}	156	170	°C/W

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VP2410		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = -5 µA	-255	-240		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -2.5 mA	-2.25	-0.8	-2.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	±1		±10	nA
		T_J = 125°C	±5		±50	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -180 V, V_{GS} = 0 V	-0.001		-1.0	µA
		T_J = 125°C	-0.40		-100	µA
On-State Drain Current [3]	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -4.5 V	-300	-150		mA
Drain-Source On-Resistance [3]	$r_{DS(ON)}$	V_{GS} = -10 V, I_D = -100 mA	7			Ω
		V_{GS} = -4.5 V, I_D = -100 mA	8.5		10	Ω
		T_J = 125°C	15.5		20	Ω
Forward Transconductance [3]	g_{FS}	V_{DS} = -10 V, I_D = -100 mA	175	125		mS
Common Source Output Conductance [3]	g_{OS}	V_{DS} = -10 V, I_D = -50 mA	125			
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = -25 V, V_{GS} = 0 V, f = 1 MHz	65		95	pF
Output Capacitance	C_{oss}		20		30	pF
Reverse Transfer Capacitance	C_{rss}		8		15	pF
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = -25 V, R_L = 250 Ω, I_D = -100 mA, V_{GEN} = -10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	7		15	ns
	t_r		18		30	ns
Turn-Off Time	$t_{d(OFF)}$		45		70	ns
	t_f		45		60	ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

6

VQ1000 SERIES

Siliconix incorporated

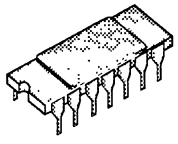
N-Channel Enhancement-Mode MOS Transistor Arrays

PRODUCT SUMMARY

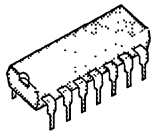
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VQ1000J	60	5.5	0.225	Plastic
VQ1000P	60	5.5	0.225	Side Braze

Performance Curves: **VNDS06** (See Section 7)

14-PIN DIP
SIDE BRAZE

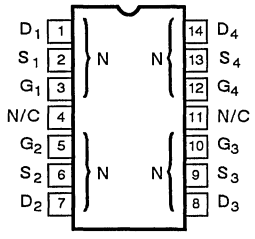


14-PIN PLASTIC



TOP VIEW

Dual-In-Line Package



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VQ1000J	VQ1000P	UNITS
Drain-Source Voltage		V_{DS}	60	60	V
Gate-Source Voltage		V_{GS}	±30	±20	
Continuous Drain Current	T_A = 25°C	I_D	0.225	0.225	A
	T_A = 100°C		0.14	0.14	
Pulsed Drain Current[1]		I_{DM}	±1	±1	
Power Dissipation – Single	T_A = 25°C	P_D	1.3	1.3	W
	T_A = 100°C		0.52	0.52	
Power Dissipation – Quad	T_A = 25°C		2	2	
	T_A = 100°C		0.8	0.8	
Operating Junction and Storage Temperature		T_J, T_{stg}	–55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VQ1000J	VQ1000P	UNITS
Junction-to-Ambient – Single	R_{thJA}	96.2	96.2	°C/W
Junction-to-Ambient – Quad		62.5	62.5	

[1]Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS [1]			LIMITS			
			VQ1000			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 100 µA	70	60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2.3	0.8	2.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±10 V	±1		±100	nA
		V_{DS} = 0 V, V_{GS} = ±10 V, T_J = 125°C	±5		±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V	0.02		10	µA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 125°C	1		500	µA
On-State Drain Current [3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1000	500		mA
Drain-Source On-Resistance [3]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.2 A	5		7.5	Ω
		V_{GS} = 10 V, I_D = 0.3 A	2.5		5.5	Ω
		V_{GS} = 10 V, I_D = 0.3 A, T_J = 125°C	4.4		7.6	Ω
Forward Transconductance [3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	230	100		mS
Common Source Output Conductance [3]	g_{OS}	V_{DS} = 7.5 V, I_D = 50 mA	500			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	16		60	pF
Output Capacitance	C_{oss}		11		25	pF
Reverse Transfer Capacitance	C_{rss}		2		5	pF
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 15 V, R_L = 23 Ω, I_D = 0.6 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	7		10	ns
Turn-Off Time	t_{OFF}		7		10	ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

6

VQ1001 SERIES

Siliconix incorporated

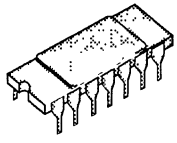
N-Channel Enhancement-Mode MOS Transistor Arrays

PRODUCT SUMMARY

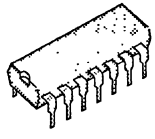
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VQ1001J	30	1	0.85	Plastic
VQ1001P	30	1	0.85	Side Braze

Performance Curves: **VNDQ03** (See Section 7)

14-PIN DIP
SIDE BRAZE

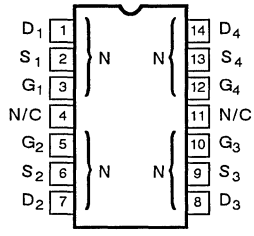


14-PIN PLASTIC



TOP VIEW

Dual-In-Line Package



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VQ1001J	VQ1001P	UNITS
Drain-Source Voltage		V_{DS}	30	30	V
Gate-Source Voltage		V_{GS}	±30	±20	
Continuous Drain Current	T_A = 25°C	I_D	0.85	0.85	A
	T_A = 100°C		0.53	0.53	
Pulsed Drain Current[1]		I_{DM}	±3	±3	
Power Dissipation – Single	T_A = 25°C	P_D	1.3	1.3	W
	T_A = 100°C		0.52	0.52	
Power Dissipation – Quad	T_A = 25°C		2	2	
	T_A = 100°C		0.80	0.80	
Operating Junction and Storage Temperature		T_j, T_{stg}	–55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VQ1001J	VQ1001P	UNITS
Junction to Ambient – Single	R_{thJA}	96.2	96.2	°C/W
Junction to Ambient – Quad		62.5	62.5	

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS [1]			LIMITS			
			VQ1001			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	65	30		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.5	0.8	2.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±15 V	± 1		± 100	nA
		V_{DS} = 0 V, V_{GS} = ±15 V, T_J = 125°C	± 5		± 500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V	0.0001		10	µA
		V_{DS} = 24 V, V_{GS} = 0 V, T_J = 125°C	0.2		500	µA
On-State Drain Current [3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 12 V	3	2		A
Drain-Source On-Resistance [3]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.2 A	1.4		1.75	Ω
		V_{GS} = 12 V, I_D = 1 A	0.85		1	Ω
		V_{GS} = 12 V, I_D = 1 A, [4] T_J = 125°C	1.65		2	Ω
Forward Transconductance [3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	500	200		mS
Common Source Output Conductance [3]	g_{OS}	V_{DS} = 10 V, I_D = 0.1 A	1500			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	38		110	pF
Output Capacitance	C_{oss}		28		110	pF
Reverse Transfer Capacitance	C_{rss}		8		35	pF
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 15 V, R_L = 23 Ω, I_D = 0.6 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	9		30	ns
Turn-Off Time	t_{OFF}		13		30	ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.
4. This parameter has been revised from previous data sheet.

6

VQ1004 SERIES

Siliconix incorporated

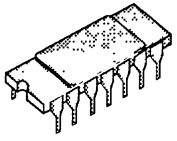
N-Channel Enhancement-Mode MOS Transistor Arrays

PRODUCT SUMMARY

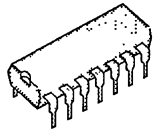
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VQ1004J	60	3.5	0.46	Plastic
VQ1004P	60	3.5	0.46	Side Braze

Performance Curves: **VNDQ06** (See Section 7)

14-PIN DIP
SIDE BRAZE

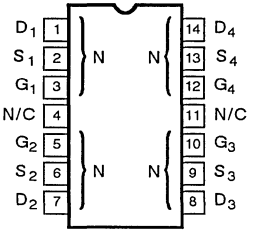


14-PIN PLASTIC



TOP VIEW

Dual-In-Line Package



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VQ1004J	VQ1004P	UNITS
Drain-Source Voltage		V_{DS}	60	60	V
Gate-Source Voltage		V_{GS}	±30	±20	
Continuous Drain Current	T_A = 25°C	I_D	0.46	0.46	A
	T_A = 100°C		0.26	0.26	
Pulsed Drain Current[1]		I_{DM}	±2	±2	
Power Dissipation – Single	T_A = 25°C	P_D	1.3	1.3	W
	T_A = 100°C		0.52	0.52	
Power Dissipation – Quad	T_A = 25°C		2	2	
	T_A = 100°C		0.8	0.8	
Operating Junction and Storage Temperature		T_j, T_{stg}	–55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VQ1004J	VQ1004P	UNITS
Junction to Ambient – Single	R_{thJA}	96.2	96.2	°C/W
Junction to Ambient – Quad		62.5	62.5	

[1]Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS [1]			LIMITS			
			VQ1004			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	70	60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.5	0.8	2.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±15 V	±1		±100	nA
		V_{DS} = 0 V, V_{GS} = ±15 V, T_J = 125°C	±5		±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V	0.05		1	µA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 125°C	0.3		500	µA
On-State Drain Current [3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.8	1.5		A
Drain-Source On-Resistance [3]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.3 A	1.8		5	Ω
		V_{GS} = 10 V, I_D = 1 A	1.3		3.5	Ω
		V_{GS} = 10 V, I_D = 1 A, T_J = 125°C	2.6		4.9	Ω
Forward Transconductance [3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	350	170		mS
Common Source Output Conductance [3]	g_{OS}	V_{DS} = 10 V, I_D = 0.1 A	1100			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	35		60	pF
Output Capacitance	C_{oss}		25		50	pF
Reverse Transfer Capacitance	C_{rss}		5		10	pF
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	8		10	ns
Turn-Off Time	t_{OFF}		9		10	ns

NOTES: 1. T_A = 25°C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%

VQ1006 SERIES

Siliconix incorporated

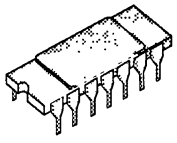
N-Channel Enhancement-Mode MOS Transistor Arrays

PRODUCT SUMMARY

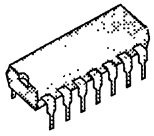
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VQ1006J	90	4.5	0.40	Plastic
VQ1006P	90	4.5	0.40	Side Braze

Performance Curves: **VNDQ09** (See Section 7)

14-PIN DIP SIDE BRAZE

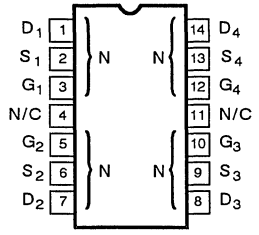


14-PIN PLASTIC



TOP VIEW

Dual-In-Line Package



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VQ1006J	VQ1006P	UNITS
Drain-Source Voltage		V_{DS}	90	90	V
Gate-Source Voltage		V_{GS}	±30	±20	
Continuous Drain Current	T_A = 25°C	I_D	0.40	0.40	A
	T_A = 100°C		0.23	0.23	
Pulsed Drain Current[1]		I_{DM}	±2	±2	
Power Dissipation – Single	T_A = 25°C	P_D	1.3	1.3	W
	T_A = 100°C		0.52	0.52	
Power Dissipation – Quad	T_A = 25°C		2	2	
	T_A = 100°C		0.8	0.8	
Operating Junction and Storage Temperature		T_j, T_{stg}	–55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VQ1006J	VQ1006P	UNITS
Junction-to-Ambient – Single	R_{thJA}	96.2	96.2	°C/W
Junction-to-Ambient – Quad		62.5	62.5	

[1]Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
			VQ1006			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	120	90		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.6	0.8	2.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±15 V	±1		±100	nA
		V_{DS} = 0 V, V_{GS} = ±15 V, T_J = 125°C	±5		±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 90 V, V_{GS} = 0 V	0.03		1	µA
		V_{DS} = 72 V, V_{GS} = 0 V, T_J = 125°C	0.3		500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.8	1.5		A
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 5 V, I_D = 0.3 A	4.7		5	Ω
		V_{GS} = 10 V, I_D = 1 A	4.1		4.5	Ω
		V_{GS} = 10 V, I_D = 1 A, [4] T_J = 125°C	7.7		8.6	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	350	170		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = 10 V, I_D = 0.1 A	225			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	35		60	pF
Output Capacitance	C_{oss}		15		50	pF
Reverse Transfer Capacitance	C_{rss}		2		10	pF
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	6		10	ns
Turn-Off Time	t_{OFF}		8		10	ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.
4. This parameter has been revised from previous data sheet.

VQ2000 SERIES

Siliconix incorporated

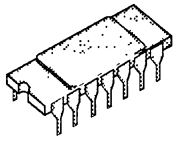
P-Channel Enchancement-Mode MOS Transistor Arrays

PRODUCT SUMMARY

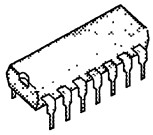
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VQ2000J	-60	10	-0.24	Plastic
VQ2000P	-60	10	-0.24	Side Braze

Performance Curves: **VPDS06** (See Section 7)

14-PIN DIP
SIDE BRAZE

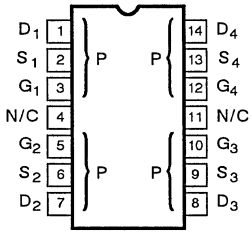


14-PIN PLASTIC



TOP VIEW

Dual-In-Line Package



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VQ2000J	VQ2000P	UNITS
Drain-Source Voltage		V_{DS}	-60	-60	V
Gate-Source Voltage		V_{GS}	±30	±20	
Continuous Drain Current	T_A = 25°C	I_D	-0.24	-0.24	A
	T_A = 100°C		-0.15	-0.15	
Pulsed Drain Current[1]		I_{DM}	±0.8	±0.8	
Power Dissipation – Single	T_A = 25°C	P_D	1.3	1.3	W
	T_A = 100°C		0.52	0.52	
Power Dissipation – Quad	T_A = 25°C		2	2	
	T_A = 100°C		0.8	0.8	
Operating Junction and Storage Temperature		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VQ2000J	VQ2000P	UNITS
Junction-to-Ambient – Single	R_{thJA}	96.2	96.2	°C/W
Junction-to-Ambient – Quad		62.5	62.5	

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
				VQ2000		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = -10 µA	-70	-60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA	-1.7	-1	-3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	±1		±10	nA
		T_J = 125°C	±5		±50	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -48 V, V_{GS} = 0 V	-0.02		-1	µA
		T_J = 125°C	-0.2		-200	
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -4.5 V	-80	-40		mA
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = -4.5 V, I_D = -25 mA	15		25	Ω
		V_{GS} = -10 V, I_D = -0.25 A	8		10	
		T_J = 125°C	15		20	
Forward Transconductance[3]	g_{FS}	V_{DS} = -10 V, I_D = -0.1 A	90	60		mS
Common Source Output Conductance[3]	g_{OS}	V_{DS} = -10 V, I_D = -0.1 A	400			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = -25 V, V_{GS} = 0 V, f = 1 MHz	15		60	pF
Output Capacitance	C_{oss}		10		25	
Reverse Transfer Capacitance	C_{rss}		3		5	
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = -25 V, R_L = 133 Ω, I_D = -0.18 A, V_{GEN} = -10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	6		15	ns
	t_r		10		20	
Turn-Off Time	$t_{d(OFF)}$		7		15	
	t_f		8		20	

NOTES: 1. T_A = 25°C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

VQ2001 SERIES

Siliconix incorporated

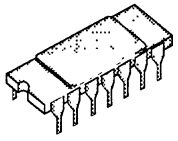
P-Channel Enhancement-Mode MOS Transistor Arrays

PRODUCT SUMMARY

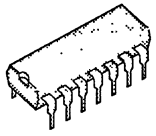
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VQ2001J	-30	2	-0.6	Plastic
VQ2001P	-30	2	-0.6	Side Braze

Performance Curves: **VPMH03** (See Section 7)

14-PIN DIP
SIDE BRAZE

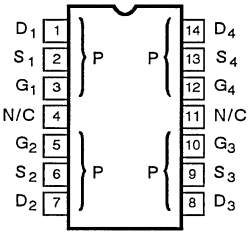


14-PIN PLASTIC



TOP VIEW

Dual-In-Line Package



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VQ2001J	VQ2001P	UNITS
Drain-Source Voltage		V_{DS}	-30	-30	V
Gate-Source Voltage		V_{GS}	±30	±20	
Continuous Drain Current	T_A = 25°C	I_D	-0.6	-0.6	A
	T_A = 100°C		-0.12	-0.12	
Pulsed Drain Current[1]		I_{DM}	±2	±2	
Power Dissipation – Single	T_A = 25°C	P_D	1.3	1.3	W
	T_A = 100°C		0.52	0.52	
Power Dissipation – Quad	T_A = 25°C		2	2	
	T_A = 100°C		0.8	0.8	
Operating Junction and Storage Temperature		T_j, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VQ2001J	VQ2001P	UNITS
Junction-to-Ambient – Single	R_{thJA}	96.2	96.2	°C/W
Junction-to-Ambient – Quad		62.5	62.5	

[1]Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS [1]			LIMITS			
			VQ2001			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = -10 µA	-55	-30		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA	-3.6	-2	-4.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±16 V	±1		±100	nA
		V_{DS} = 0 V, V_{GS} = ±16 V, T_J = 125°C	±5		±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -30 V, V_{GS} = 0 V	-0.0001		-10	µA
		V_{DS} = -30 V, V_{GS} = 0 V, T_J = 125°C	-0.3		-500	µA
On-State Drain Current [3]	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -12 V	-1.6	-1.5		A
Drain-Source On-Resistance [3]	$r_{DS(ON)}$	V_{GS} = -12 V, I_D = -1 A	1.8		2	Ω
		V_{GS} = -12 V, I_D = -1 A, T_J = 125°C	3.1		3.6	Ω
Forward Transconductance [3]	g_{FS}	V_{DS} = -10 V, I_D = -0.5 A	290	200		mS
Common Source Output Conductance [3]	g_{OS}	V_{DS} = -7.5 V, I_D = -0.05 A	800			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = -15 V, V_{GS} = 0 V, f = 1 MHz	130		150	pF
Output Capacitance	C_{oss}		75		100	pF
Reverse Transfer Capacitance	C_{rss}		20		60	pF
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = -15 V, R_L = 23 Ω, I_D = -0.6 A, V_{GEN} = -10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	18		30	ns
Turn-Off Time	t_{OFF}		13		30	ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.

VQ2004 SERIES

Siliconix incorporated

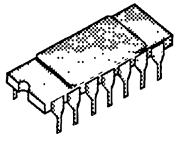
P-Channel Enhancement-Mode MOS Transistor Arrays

PRODUCT SUMMARY

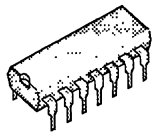
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VQ2004J	-60	5	-0.41	Plastic
VQ2004P	-60	5	-0.41	Side Braze

Performance Curves: **VPDV10** (See Section 7)

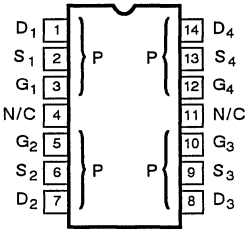
14-PIN DIP
SIDE BRAZE



14-PIN PLASTIC



TOP VIEW
Dual-In-Line Package



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VQ2004J	VQ2004P	UNITS
Drain-Source Voltage		V_{DS}	-60	-60	V
Gate-Source Voltage		V_{GS}	±30	±20	
Continuous Drain Current	T_A = 25°C	I_D	-0.41	-0.41	A
	T_A = 100°C		-0.23	-0.23	
Pulsed Drain Current[1]		I_{DM}	±3	±3	
Power Dissipation - Single	T_A = 25°C	P_D	1.3	1.3	W
	T_A = 100°C		0.52	0.52	
Power Dissipation - Quad	T_A = 25°C		2	2	
	T_A = 100°C		0.8	0.8	
Operating Junction and Storage Temperature		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VQ2004J	VQ2004P	UNITS
Junction-to-Ambient - Single	R_{thJA}	96.2	96.2	°C/W
Junction-to-Ambient - Quad		62.5	62.5	

[1]Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS [1]			LIMITS			
				VQ2004 [4]		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = -10 µA	-110	-60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA	-3.4	-2	-4.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±30 V	±1		±100	nA
		T_J = 125°C	±5		±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -60 V, V_{GS} = 0 V	-0.0005		-10	µA
		T_J = 125°C	-0.1		-500	µA
On-State Drain Current [3]	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -10 V	-2	-1		A
Drain-Source On-Resistance [3]	$r_{DS(ON)}$	V_{GS} = -10 V, I_D = -1 A	2.5		5	Ω
		T_J = 125°C	4.3		8	Ω
Forward Transconductance [3]	g_{FS}	V_{DS} = -10 V, I_D = -0.5 A	325	200		mS
Common Source Output Conductance [3]	g_{OS}	V_{DS} = -7.5 V, I_D = -0.1 A	450			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = -25 V, V_{GS} = 0 V, f = 1 MHz	75		150	pF
Output Capacitance	C_{oss}		40		60	pF
Reverse Transfer Capacitance	C_{rss}		18		25	pF
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = -25 V, R_L = 47 Ω, I_D = -0.5 A, V_{GEN} = -10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	11		15	ns
	t_r		30		40	ns
Turn-Off Time	$t_{d(OFF)}$		20		30	ns
	t_f		20		30	ns

NOTES: 1. T_A = 25°C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.
4. Data sheet limits have been revised.

6

VQ2006 SERIES

Siliconix incorporated

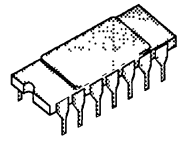
P-Channel Enhancement-Mode MOS Transistor Arrays

PRODUCT SUMMARY

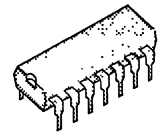
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VQ2006J	-90	5	-0.41	Plastic
VQ2006P	-90	5	-0.41	Side Braze

Performance Curves: **VPDV10** (See Section 7)

14-PIN DIP
SIDE BRAZE

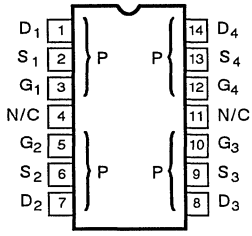


14-PIN PLASTIC



TOP VIEW

Dual-In-Line Package



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VQ2006J	VQ2006P	UNITS
Drain-Source Voltage		V_{DS}	-90	-90	V
Gate-Source Voltage		V_{GS}	±30	±20	V
Continuous Drain Current	T_A = 25°C	I_D	-0.41	-0.41	A
	T_A = 100°C		-0.23	-0.23	A
Pulsed Drain Current[1]		I_{DM}	±3	±3	A
Power Dissipation - Single	T_A = 25°C	P_D	1.3	1.3	W
	T_A = 100°C		0.52	0.52	W
Power Dissipation - Quad	T_A = 25°C		2	2	W
	T_A = 100°C		0.8	0.8	W
Operating Junction and Storage Temperature		T_j, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300		°C

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VQ2006J	VQ2006P	UNITS
Junction-to-Ambient - Single	R_{thJA}	96.2	96.2	°C/W
Junction-to-Ambient - Quad		62.5	62.5	°C/W

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS [1]			LIMITS			
				VQ2006 [4]		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = -10 µA	-110	-90		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA	-3.4	-2	-4.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±30 V	±1		±100	nA
		T_J = 125°C	±5		±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -90 V, V_{GS} = 0 V	-0.0005		-10	µA
		T_J = 125°C	-0.1		-500	µA
On-State Drain Current [3]	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -10 V	-2	-1		A
Drain-Source On-Resistance [3]	$r_{DS(ON)}$	V_{GS} = -10 V, I_D = -1 A	2.5		5	Ω
		T_J = 125°C	4.3		8	Ω
Forward Transconductance [3]	g_{FS}	V_{DS} = -10 V, I_D = -0.5 A	325	200		mS
Common Source Output Conductance [3]	g_{OS}	V_{DS} = -7.5 V, I_D = -0.1 A	450			µS
DYNAMIC						
Input Capacitance	C_{iss}	V_{DS} = -25 V, V_{GS} = 0 V, f = 1 MHz	75		150	pF
Output Capacitance	C_{oss}		40		60	pF
Reverse Transfer Capacitance	C_{rss}		18		25	pF
SWITCHING						
Turn-On Time	$t_{d(ON)}$	V_{DD} = -25 V, R_L = 47 Ω, I_D = -0.5 A, V_{GEN} = -10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	11		15	ns
	t_r		30		40	ns
Turn-Off Time	$t_{d(OFF)}$		20		30	ns
	t_f		20		30	ns

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.
4. Data sheet limits have been revised.

6

VQ3001 SERIES

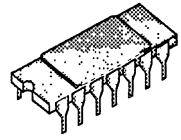
Siliconix incorporated

N- and P-Channel Enhancement-Mode MOS Transistor Arrays

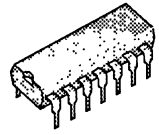
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	PACKAGE
VQ3001J	30/–30	N = 1 P = 2	N = 0.85 P = 0.6	Plastic
VQ3001P	30/–30	N = 1 P = 2	N = 0.85 P = 0.6	Side Braze

14-PIN DIP
SIDE BRAZE

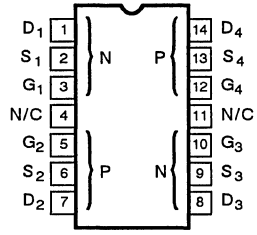


14-PIN PLASTIC



TOP VIEW

Dual-In-Line Package



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	VQ3001J		VQ3001P		UNITS
			N-Channel	P-Channel	N-Channel	P-Channel	
Drain-Source Voltage		V_{DS}	30	–30	30	–30	V
Gate-Source Voltage		V_{GS}	± 30	± 30	± 20	± 20	
Continuous Drain Current	T_A = 25°C	I_D	± 0.85	± 0.6	± 0.85	± 0.6	A
	T_A = 100°C		± 0.52	± 0.37	± 0.52	± 0.37	
Pulsed Drain Current[1]		I_{DM}	±3	±2	±3	±2	
Power Dissipation – Single	T_A = 25°C	P_D	1.3		1.3		W
	T_A = 100°C		0.52		0.52		
Power Dissipation – Quad	T_A = 25°C		2		2		
	T_A = 100°C		0.8		0.8		
Operating Junction and Storage Temperature		T_j, T_{stg}	–55 to 150				°C
Lead Temperature (1/16" from case for 10 seconds)		T_L	300				

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VQ3001J	VQ3001P	UNITS
Junction-to-Ambient – Single	R_{thJA}	96.2	96.2	°C/W
Junction-to-Ambient – Quad		62.5	62.5	

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS[1]			LIMITS						
			N-Channel			P-Channel			
PARAMETER	SYMBOL	TEST CONDITIONS[5]	TYP[2]	MIN	MAX	TYP[2]	MIN	MAX	UNIT
STATIC									
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 mA	55	30		-55	-30		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2	0.8	2.5	-3.5	-2	-4.5	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±16 V	± 0.1		± 100	± 0.1		± 100	nA
		V_{DS} = 0 V, V_{GS} = ±16 V, T_J = 125°C	± 5		± 500	± 5		± 500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24 V, V_{GS} = 0 V	0.005		10	-0.005		-10	µA
		V_{DS} = 24 V, V_{GS} = 0 V, T_J = 125°C	0.5		500	-0.5		-500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 12 V	3	2		-2	-1.5		A
Drain-Source On-Resistance[3]	$r_{DS(ON)}$	V_{GS} = 12 V, I_D = 1 A	0.8		1	1.8		2	Ω
		V_{GS} = 12 V, I_D = 1 A, T_J = 125°C	1.4		1.75	3.1		3.5	Ω
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	360	250		280	200		mS
DYNAMIC									
Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	85		110	130		150	pF
Output Capacitance	C_{oss}		83		110	75		100	pF
Reverse Transfer Capacitance	C_{rss}		20		35	20		60	pF
SWITCHING[4]									
Turn-On Time	t_{ON}	V_{DD} = 15 V, R_L = 23 Ω, I_D = 0.65 A, V_{GEN} = 10 V, R_G = 25 Ω	10		30	18		30	ns
Turn-Off Time	t_{OFF}		13.5		30	26		30	ns

NOTES:
1. T_A = 25°C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse Test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
4. Switching time is essentially independent of operating temperature.
5. Test conditions are at (-) polarities.

6

VQ7254 SERIES

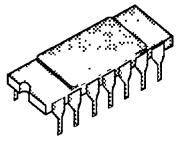
Siliconix incorporated

N- and P-Channel Enhancement-Mode MOS Transistor Arrays

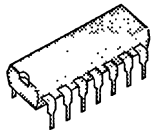
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ $Q_1 + Q_2$ or $Q_3 + Q_4$	I_D (A)	PACKAGE
VQ7254J	20/–20	3 Ω	2	Plastic
VQ7254P	20/–20	3 Ω	2	Side Braze

14-PIN DIP
SIDE BRAZE

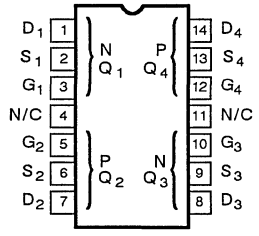


14-PIN PLASTIC



TOP VIEW

Dual-In-Line Package



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

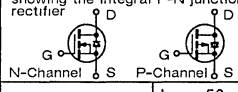
PARAMETERS/TEST CONDITIONS		SYMBOL	VQ7254J		VQ7254P		UNITS
			N-Channel	P-Channel	N-Channel	P-Channel	
Drain-Source Voltage		V_{DS}	20	–20	20	–20	V
Gate-Source Voltage		V_{GS}	±30	±30	±20	±20	
Continuous Drain Current (T_A = 25°C)		I_D	2	–2	2	–2	A
Pulsed Drain Current[1]		I_{DM}	±3	±3	±3	±3	
Power Dissipation – Single	T_A = 25°C	P_D	1.75	1.75	1.75	1.75	W
	T_A = 80°C		1.05	1.05	1.05	1.05	
Operating Junction		T_j	–40 to 100				°C
Storage Temperature		T_{stg}	–40 to 150				
Lead Temperature (1/16" from case for 10 seconds)		T_L	300				
Thermal Coupling Factor – Single (K)–Q_1–Q_4 or Q_2–Q_3			60				%
Thermal Coupling Factor – Single (K)–Q_1–Q_2–Q_3–Q_4, Q_1–Q_3 or Q_2–Q_4			50				

THERMAL RESISTANCE

THERMAL RESISTANCE	SYMBOL	VQ7254J	VQ7254P	UNITS
Junction-to-Ambient – Single	R_{thJA}	96.2	96.2	°C/W
Junction-to-Ambient – Quad		62.5	62.5	

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS[1]			LIMITS			
			VQ7254			
PARAMETER	SYMBOL	TEST CONDITIONS[6]	TYP[2]	MIN	MAX	UNIT
STATIC[4]						
Drain-Source On Voltage	$V_{DS(ON)}$	V_{GS} = 11.4 V, I_D = 1 A ($Q_1 + Q_2$) or ($Q_3 + Q_4$)	2.5	2	3	V
Drain-Source On-Resistance[3]	$r_{DS(ON)}$		2.5	2	3	Ω

			N-Channel			P-Channel			
PARAMETER	SYMBOL	TEST CONDITIONS[6]	TYP[2]	MIN	MAX	TYP[2]	MIN	MAX	UNIT
STATIC									
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	-40	20		-55	-20		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	1.5	0.8		-3.6	-0.8		
		T_J = 85°C	1.2	0.65		-3.3	-0.65		
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±12 V	±1		±100	±1		±100	nA
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	0.1		500	-0.1		-500	µA
On-State Drain Current[3]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V	1.8			-1.6			A
Forward Transconductance[3]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A	500	200		290	200		mS
DYNAMIC									
Input Capacitance	C_{iss}	V_{DS} = 12 V, V_{GS} = 0 V, f = 1 MHz	85		175	130		190	pF
Output Capacitance	C_{oss}		80		95	75		100	
Reverse Transfer Capacitance	C_{rss}		18		25	20		60	
SWITCHING[5]									
Turn-On Time	t_{ON}	V_{DD} = 17 V, R_L = 15 Ω, I_D = 1.1 A, V_{GEN} = 10 V, R_G = 25 Ω	12		20	20		30	ns
Turn-Off Time	t_{OFF}		14		20	20		30	
DYNAMIC									
Continuous Source Current (Body Diode)	I_S	Modified MOSPOWER symbol showing the integral P-N junction rectifier 			2			-2	A
Source Current (Body Diode)	I_{SM}				3			-3	
Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, T_C = 25°C, I_S = 50 mA	0.6		0.75	-0.6		-0.75	V
		I_S = 1 A	1		1.2	-1		-1.2	

NOTES:
1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 2%.
4. $r_{DS(ON)}$ and $V_{DS(ON)}$ limits are not specified for individual transistors but are measured as the sum of a n- and p-channel pair.
5. Switching time is essentially independent of operating temperature.
6. Reverse polarity for p-channel devices.

N-Channel Enhancement-Mode DMOS FET

DESIGNED FOR:

- Ultra-High Speed Switching
- High Gain Amplifiers

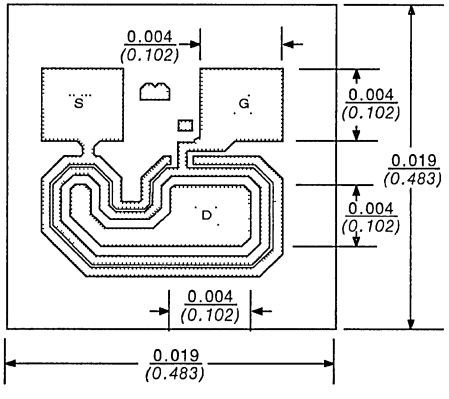
FEATURES

- < 1 ns Switching t_{ON}
  Ultra-Low Capacitance C_G < 3.5 pF
- g_{fs} (gain) > 10000 μmhos

TYPE	PACKAGE	DEVICE
Single	TO-72	• SD210DE, SD211DE, SD212DE, SD213DE, SD214DE, SD215DE
	SOT-143	• SST211, SST213, SST215
Quads	Dual-In-Line 16-Pin Side Braze	• SD5000I, SD5001I, SD5002I
	Dual-In-Line 16-Pin Plastic	• SD5000N, SD5001N, SD5002N
	Surface Mount	• SD5400CY, SD5401CY, SD5402CY
	Chip/ Wafer	• Available as above specifications

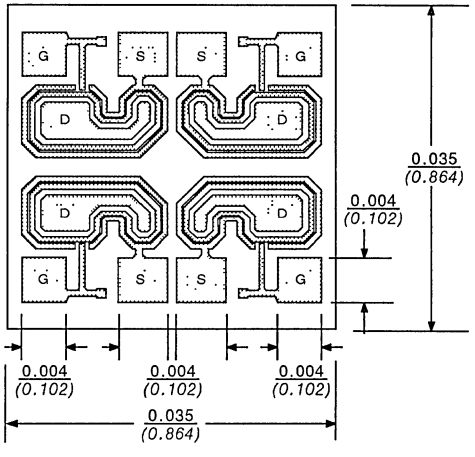
GEOMETRY DIAGRAMS

DMCB Single



Note: For Switching Circuit
See LPD-10 (Section 9)

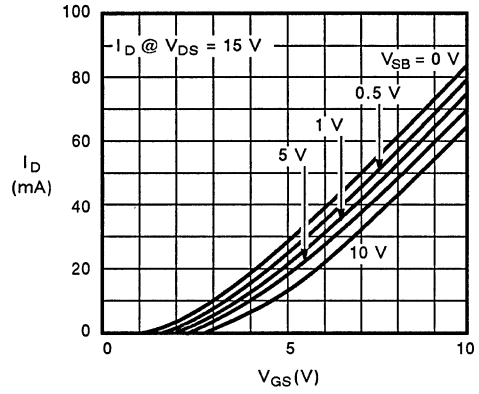
DMCA Quad



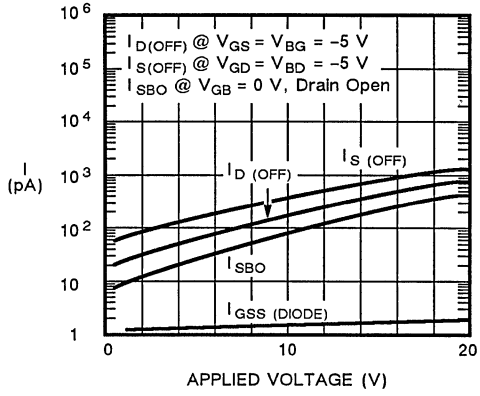
7

TYPICAL CHARACTERISTICS

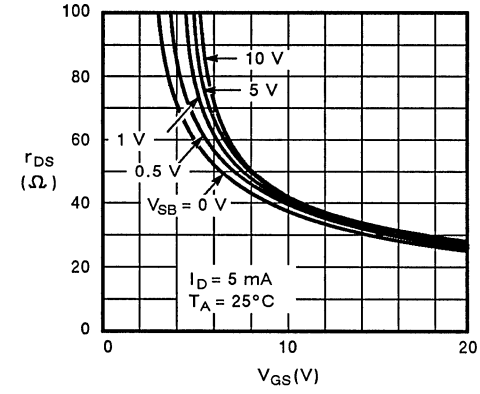
Drain Current vs. Gate-Source Voltage



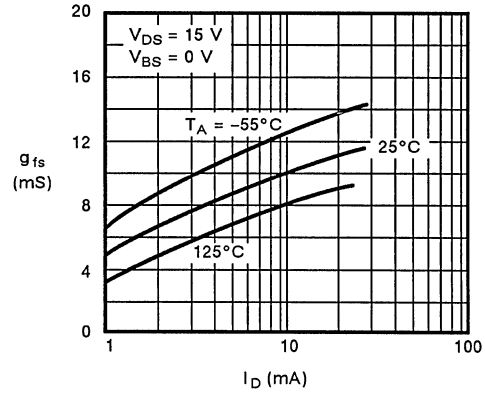
Leakage Current vs. Applied Voltage



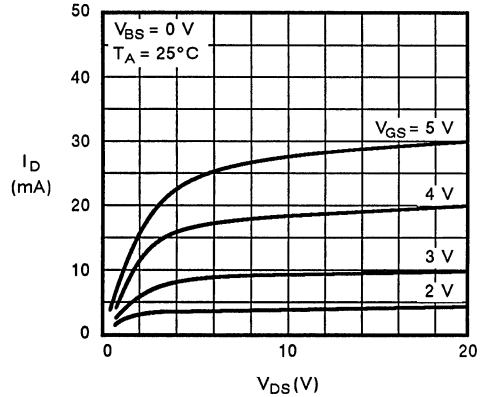
On-Resistance vs. Gate-Source Voltage



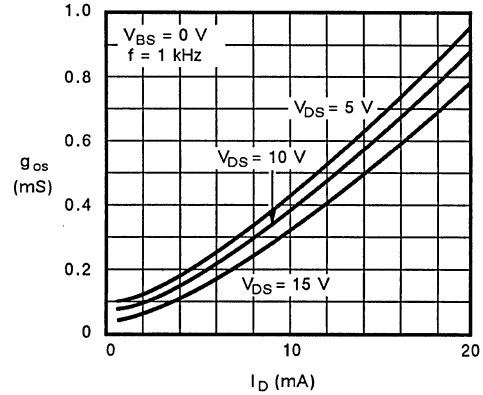
Common-Source Forward Transconductance vs. Drain Current



Output Characteristics

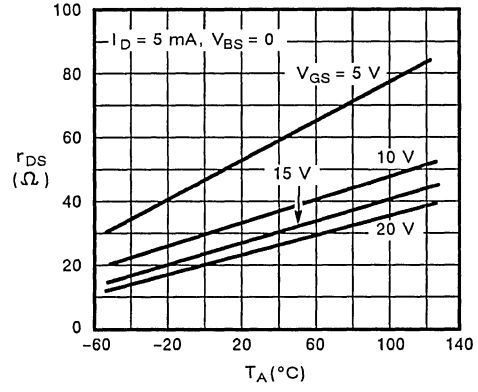


Output Conductance vs. Drain Current

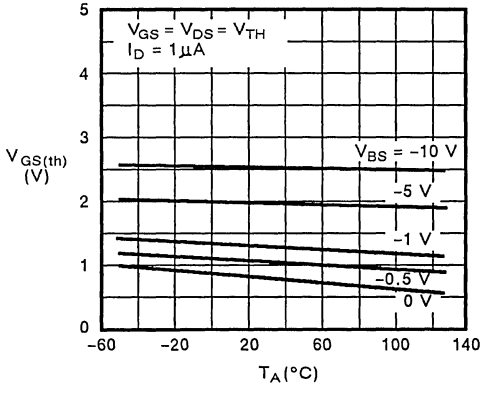


TYPICAL CHARACTERISTICS

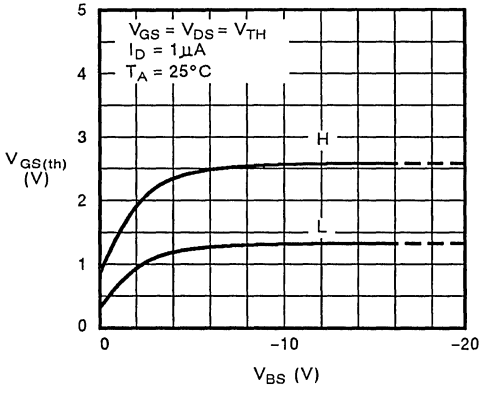
On-Resistance vs. Temperature



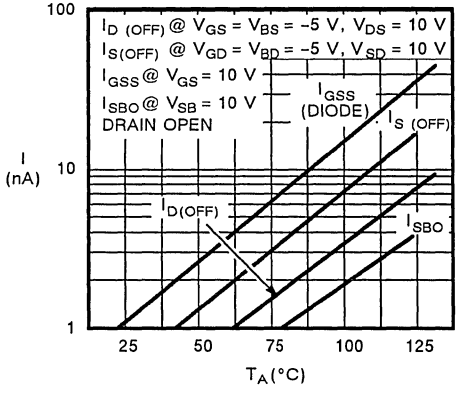
Threshold Voltage vs. Temperature



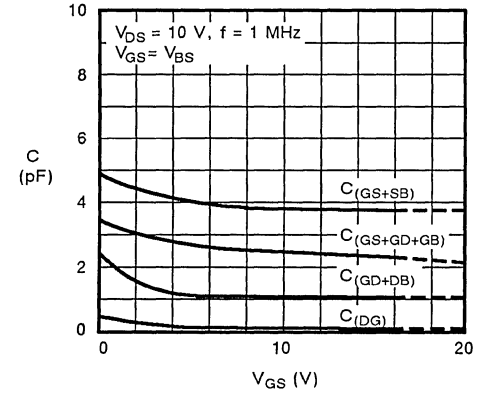
Threshold Voltage vs. Substrate-Source Voltage



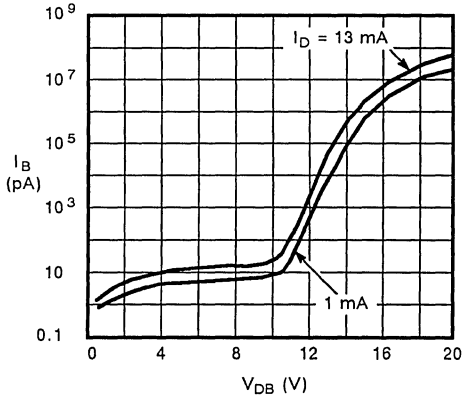
Leakage Currents vs. Temperature



Capacitance vs. Gate-Source Voltage



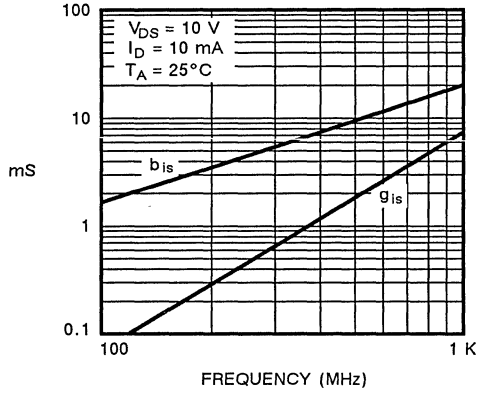
Body Leakage Current vs. Drain-Body Voltage



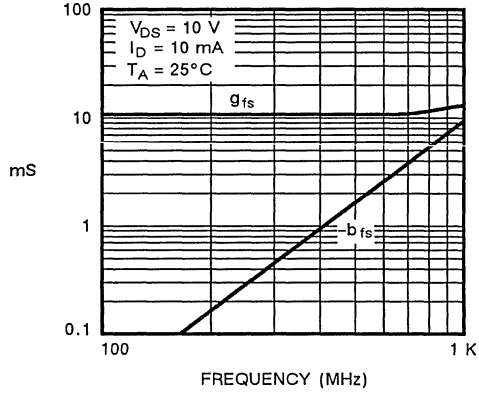
7

TYPICAL CHARACTERISTICS

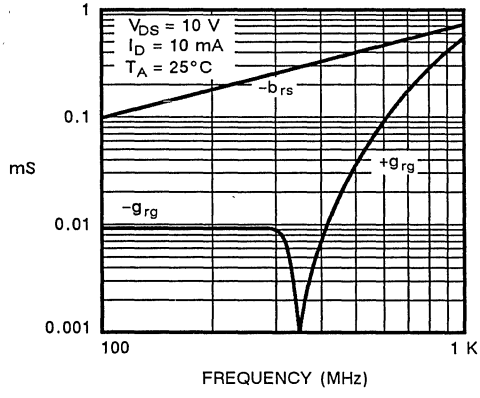
Input Admittance



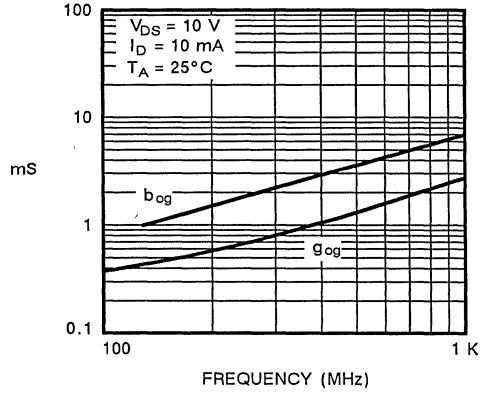
Forward Admittance



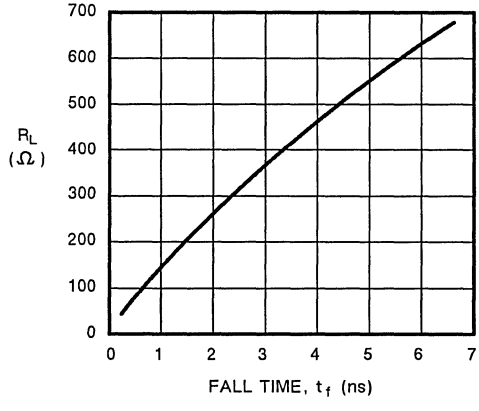
Reverse Admittance



Output Admittance



Switching Characteristics



N-Channel Depletion-Mode MOSFET

DESIGNED FOR:

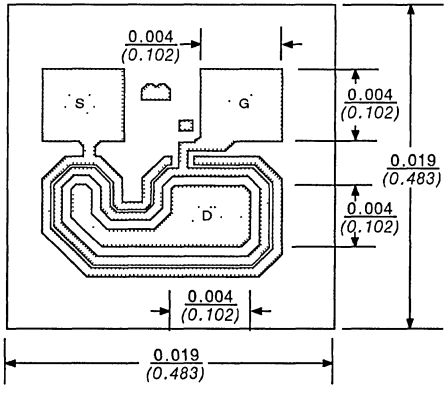
- High Gain Amplification
- Analog Switching

TYPE	PACKAGE	DEVICE
Single	To-72	• SD2100
	Chip	• Available as above specification

FEATURES

- High g_{fs} > 10 mS (Typically)

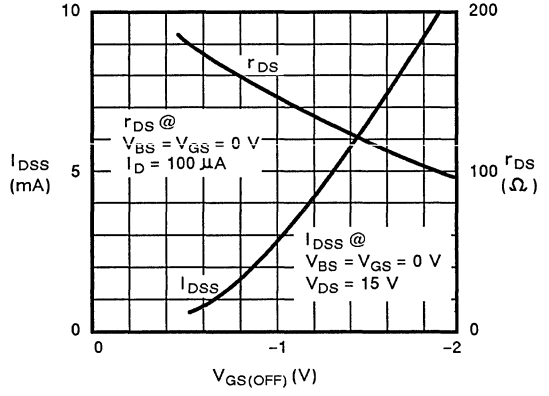
GEOMETRY DIAGRAM



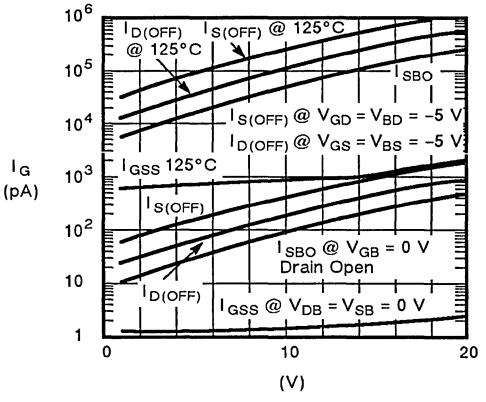
7

TYPICAL CHARACTERISTICS (DEPLETION-MODE)

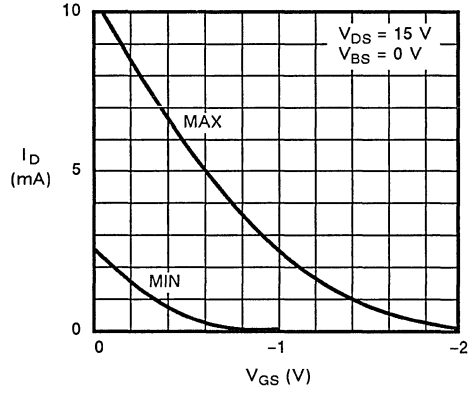
Depletion Mode – Drain Current & On-Resistance vs. Gate-Source Cutoff Voltage



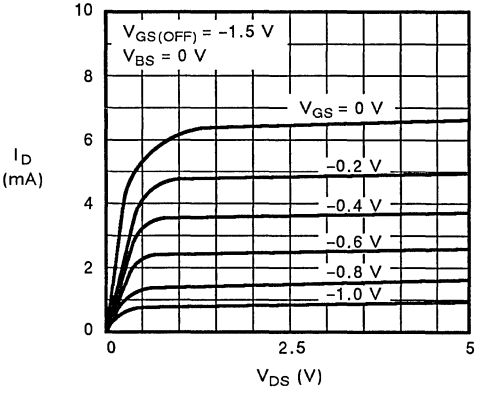
Leakage Currents vs. Applied Voltage



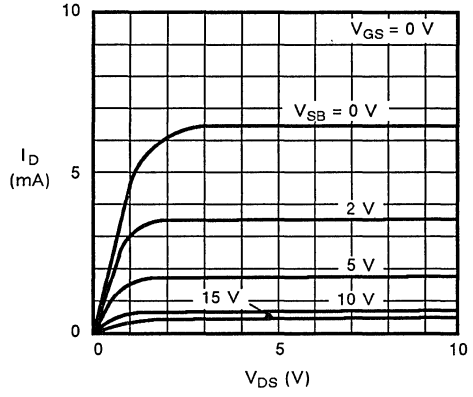
Drain Current vs. Gate-Source Voltage



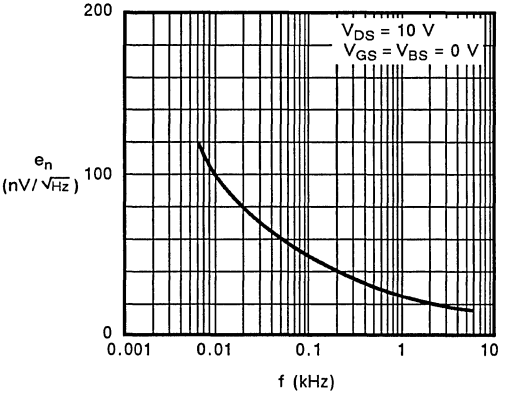
Drain Current vs. Drain-Source Voltage



Output Characteristics ($V_{GS(OFF)}$ = -1.5 V)

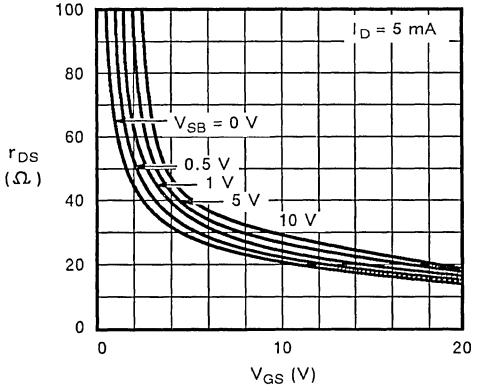


Equivalent Input Noise Voltage vs. Frequency

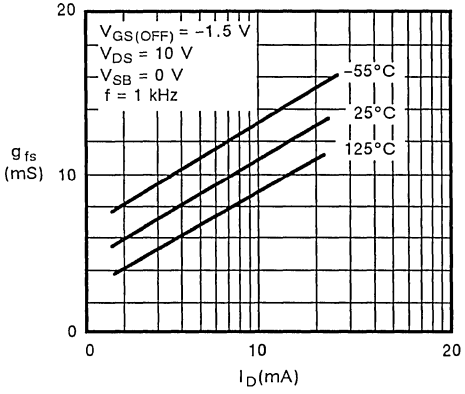


TYPICAL CHARACTERISTICS (ENHANCEMENT-MODE)

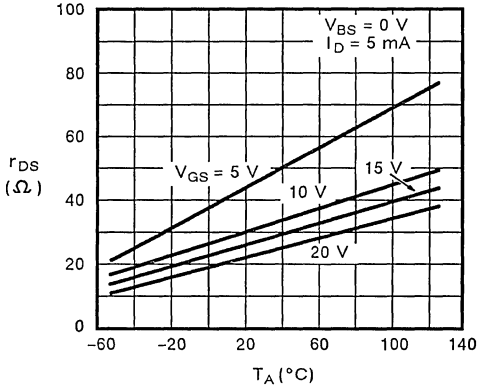
Drain-Source On-Resistance vs. Gate-Source Voltage



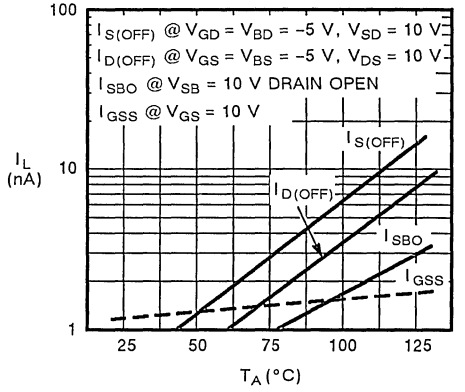
Common-Source Forward Transconductance vs. Drain Current



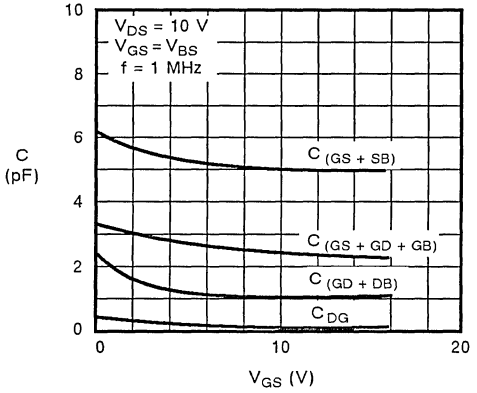
On-Resistance vs. Temperature



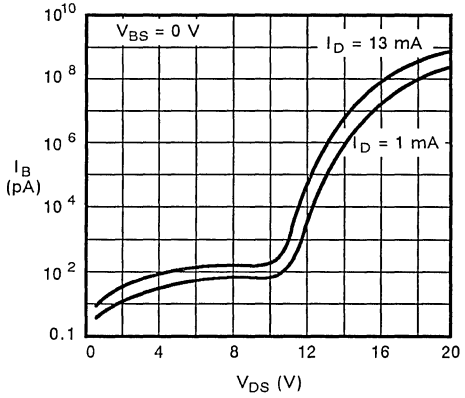
Leakage Current vs. Temperature



Capacitance vs. Gate-Source Voltage



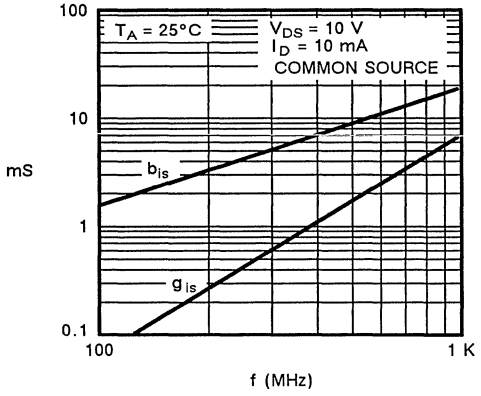
Body-Channel Leakage Current vs. Drain-Source Voltage



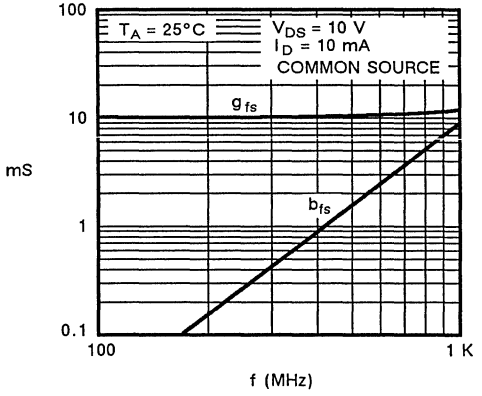
7

TYPICAL CHARACTERISTICS (ENHANCEMENT-MODE)

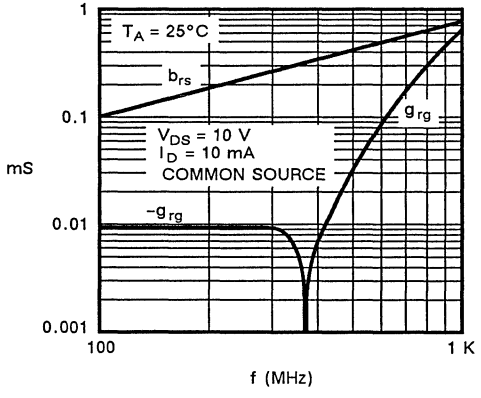
Input Admittance



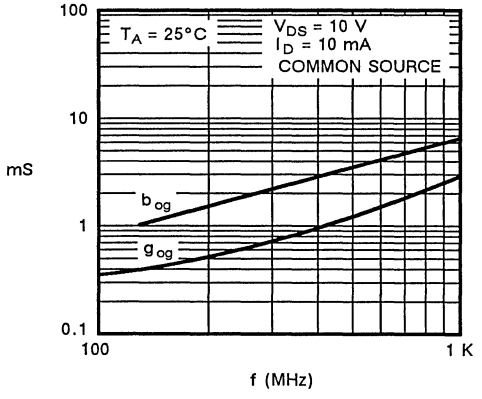
Forward Admittance



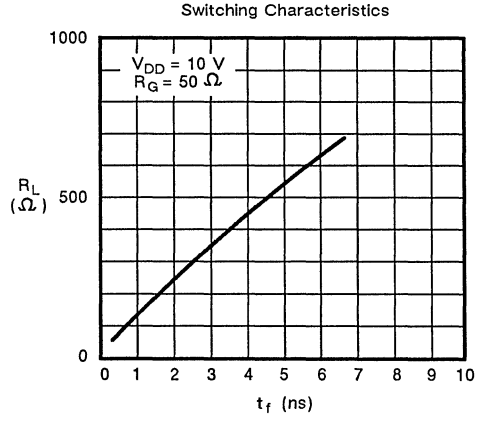
Reverse Admittance



Output Admittance



Switching Characteristics



P-Channel Enhancement-Mode MOSFET

DESIGNED FOR:

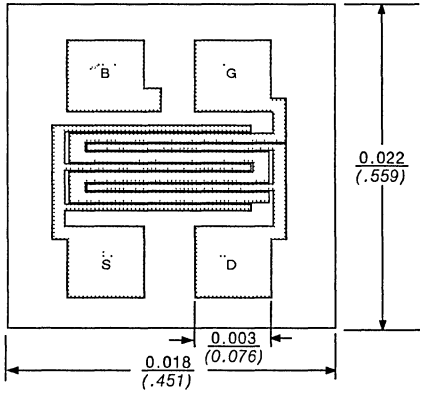
- Analog and Digital Switching
- General Purpose Amplifiers
- Smoke Detectors

FEATURES

- High Gate Transient Voltage Breakdown Eliminates need for Gate Protective Diode
- Ultra-High Input Imedance
- Normally Off

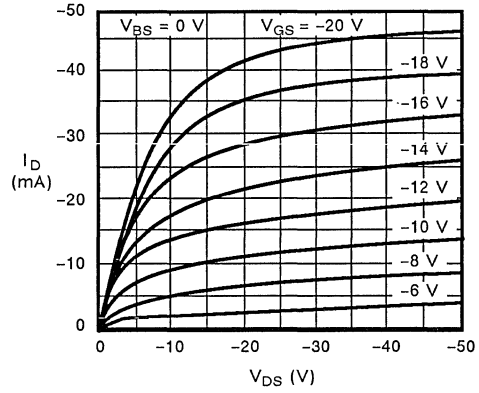
TYPE	PACKAGE	DEVICE
Single	TO-18	• MFE823
	TO-72	• 3N163, 3N164
	Chip/ Wafer	• Available as above specifications

GEOMETRY DIAGRAM

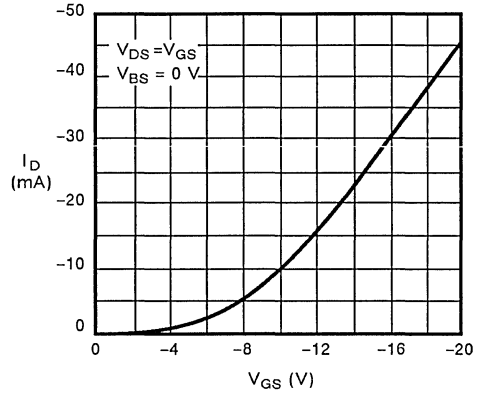


TYPICAL CHARACTERISTICS

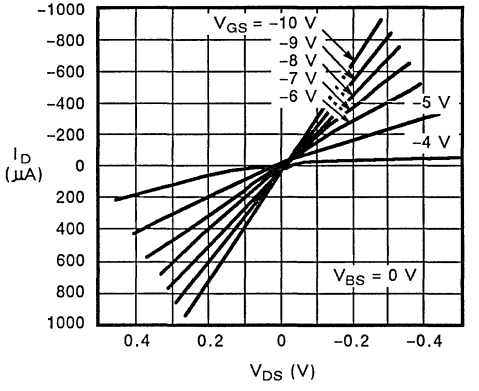
Output Characteristics



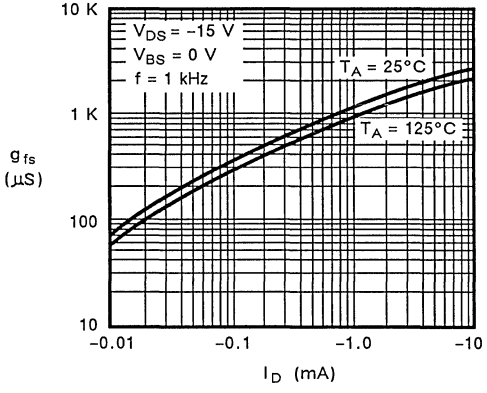
Transfer Characteristics



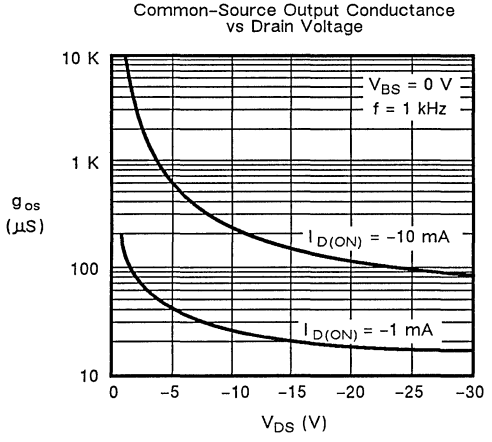
Low-Level Output Characteristics



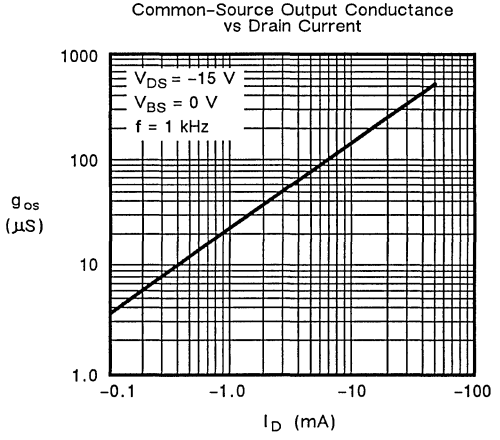
Common-Source Forward Transconductance vs Drain Current



Common-Source Output Conductance vs Drain Voltage

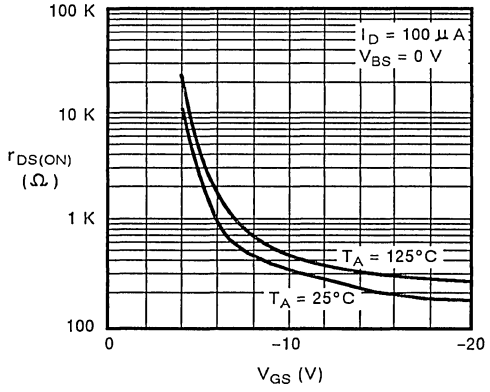


Common-Source Output Conductance vs Drain Current

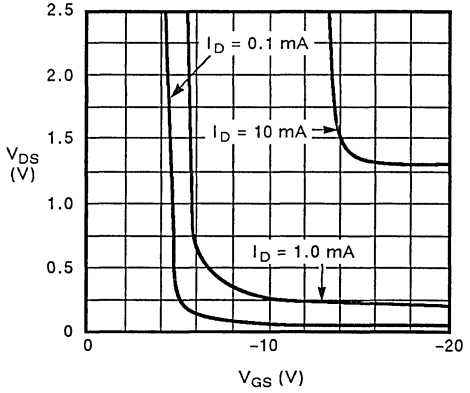


TYPICAL CHARACTERISTICS

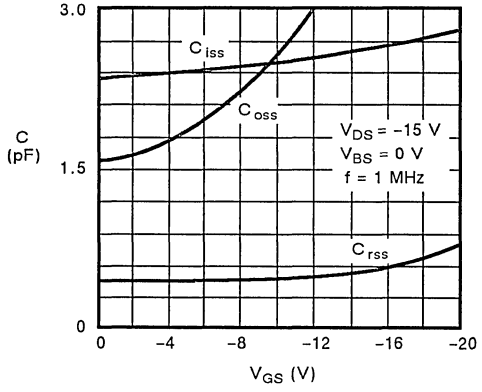
Drain Source On-Resistance vs. Gate-Source Voltage



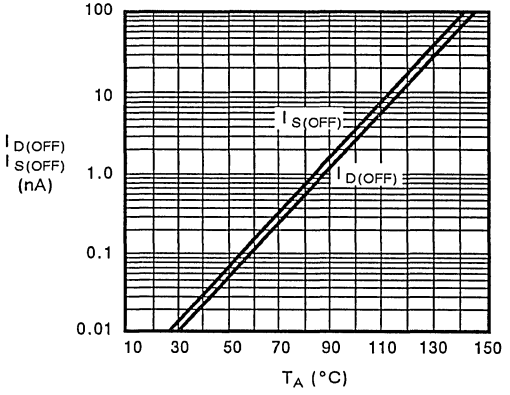
Low-Level ON Drain-Source Voltage vs. Gate-Source Voltage



Capacitance vs. Gate-Source Voltage



Drain-Source Leakage Current vs. Temperature



7

Siliconix incorporated

N-Channel JFET Circuit

DESIGNED FOR:

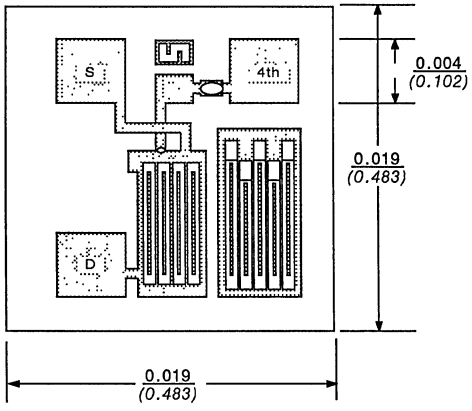
- Pre-Amplifiers
- Infrared Detectors

FEATURES

- Low Leakage < 2 pA Typically
- Low Noise < 10 nV/√Hz at 10 Hz

TYPE	PACKAGE	DEVICE
Single	SOT-143	• SST6908, SST6909, SST6910
	TO-72	• 2N6908, 2N6909, 2N6910

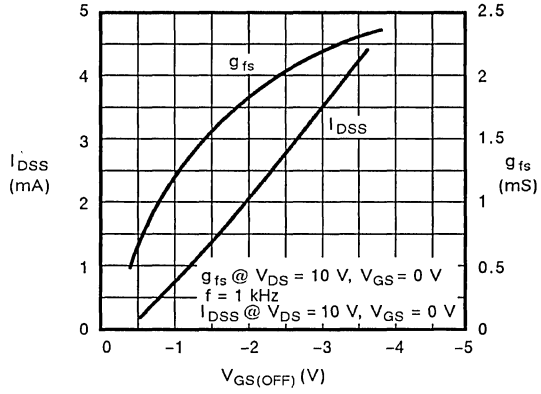
GEOMETRY DIAGRAM



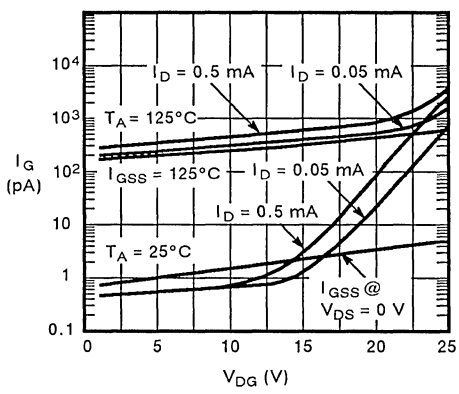
Gate is backside contact

TYPICAL CHARACTERISTICS

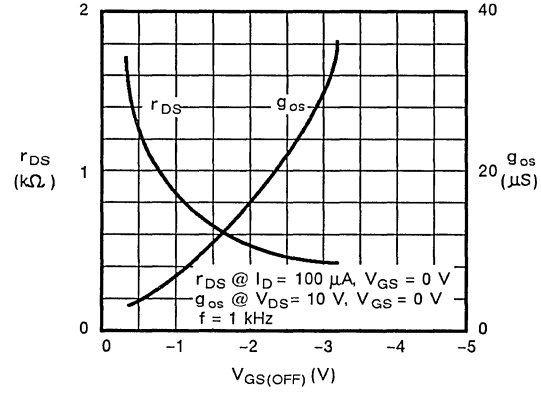
Drain Current & Transconductance vs. Gate-Source Cutoff Voltage



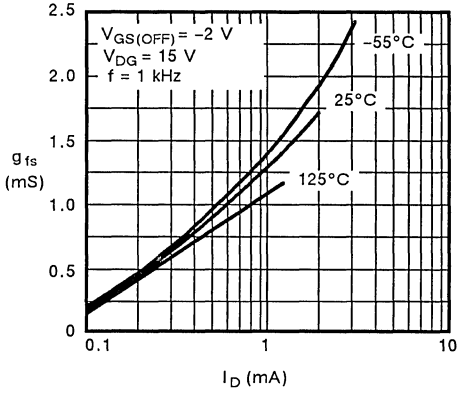
Operating Gate Current



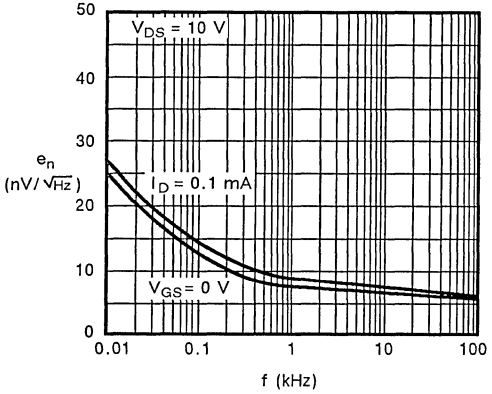
On-Resistance & Output Conductance vs. Gate-Source Cutoff Voltage



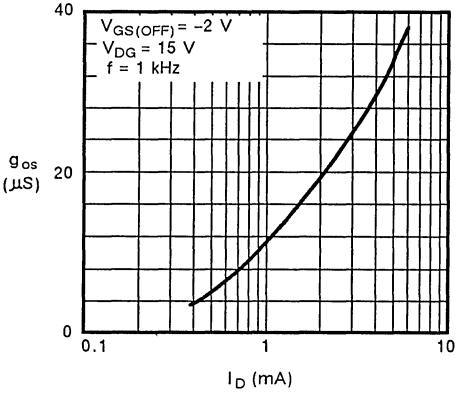
Common-Source Forward Transconductance vs. Drain Current



Equivalent Input Noise Voltage vs. Frequency



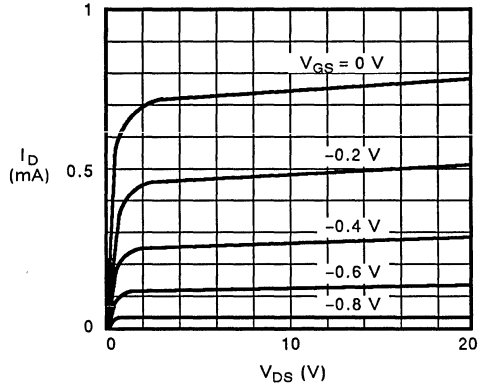
Output Conductance vs. Drain Current



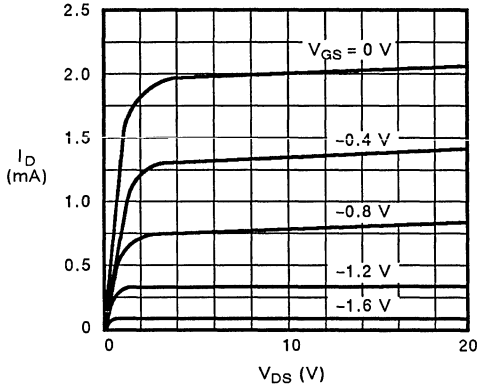
7

TYPICAL CHARACTERISTICS

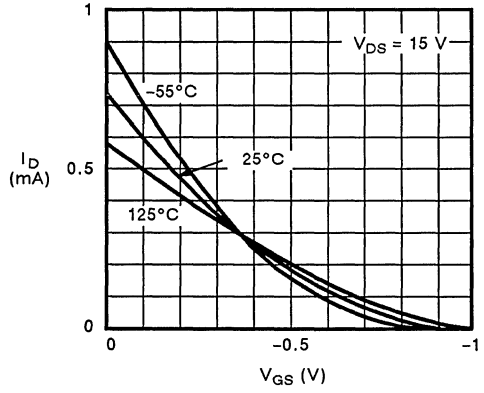
Output Characteristics ($V_{GS(OFF)}$ = -1 V)



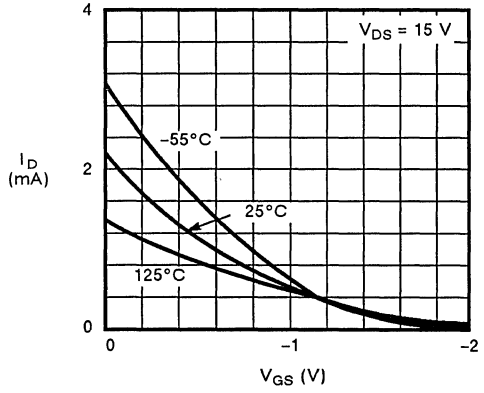
Output Characteristics ($V_{GS(OFF)}$ = -2 V)



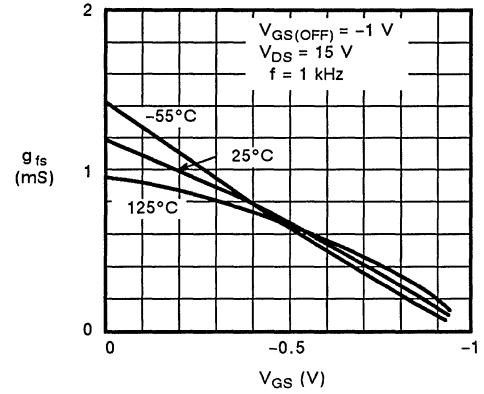
Transfer Characteristics ($V_{GS(OFF)}$ = -1 V)



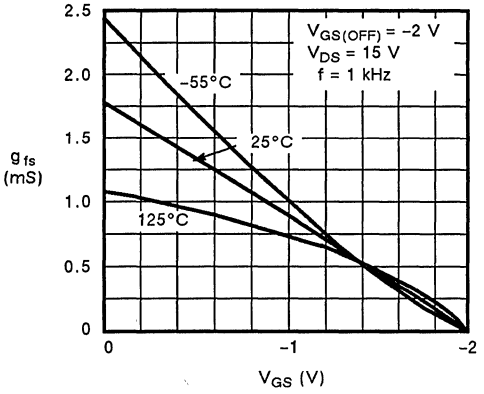
Transfer Characteristics ($V_{GS(OFF)}$ = -2 V)



Transconductance vs. Gate-Source Voltage

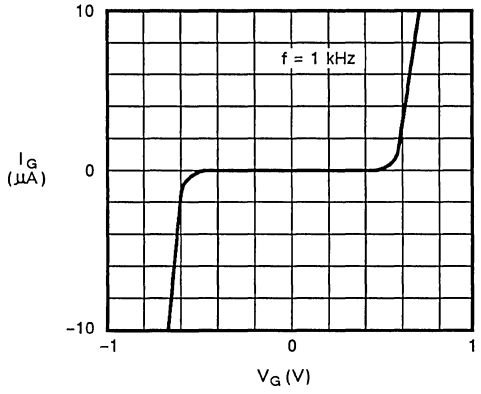


Transconductance vs. Gate-Source Voltage

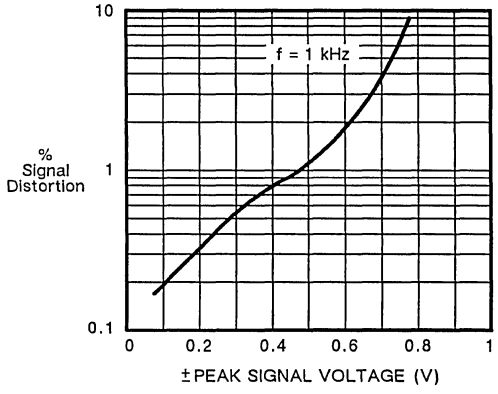


TYPICAL CHARACTERISTICS

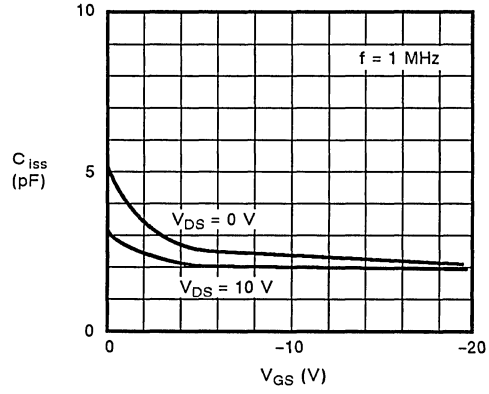
Input Current vs. Input Voltage



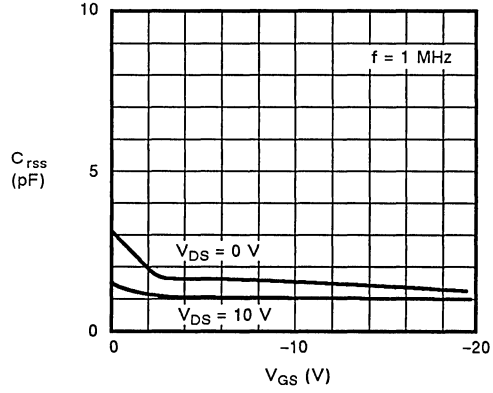
Signal Distortion vs. Signal Voltage



Common-Source Input Capacitance vs. Gate-Source Voltage



Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



7

Siliconix incorporated

N-Channel JFET

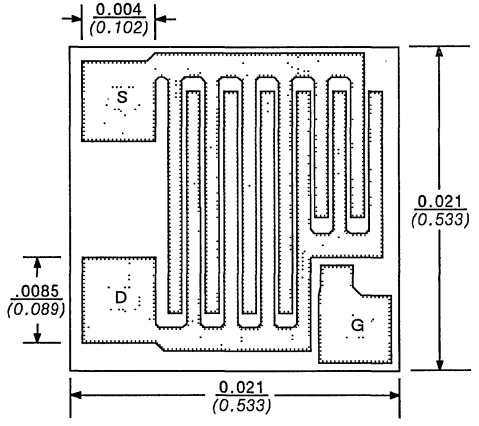
DESIGNED FOR:

- Analog Switches
- Commutators
- Choppers
- Voltage Controlled Resistors
- Integrator Reset Switch

FEATURES

- High Speed t_{ON} < 20 ns
- High Off-Isolation $I_{D(OFF)}$ < 100 pA
- No Offset or Error Voltages Generated by Closed Switch. Purely Resistive. High Isolation Resistance from Driver

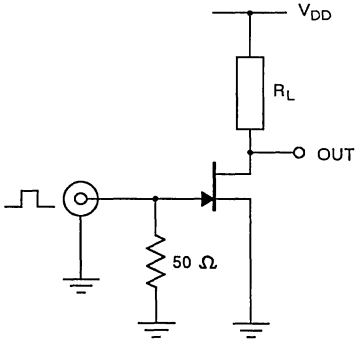
GEOMETRY DIAGRAM



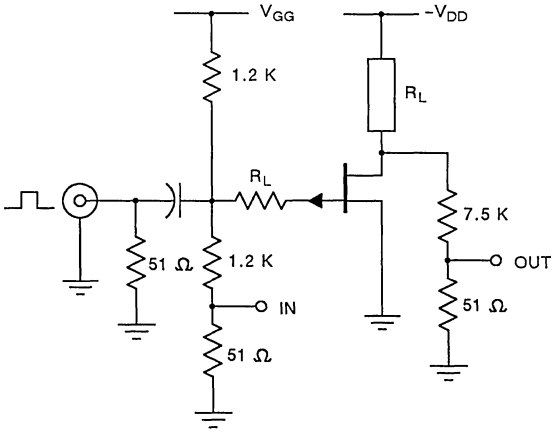
Gate also backside contact

TYPE	PACKAGE	DEVICE
Single	TO-92	• 2N5638, 2N5639, 2N5640 J111, J12, J113 J111A, J112A, J113A PN4091, PN4092, PN4093 PN4391, PN4392, PN4393 U1897, U1898, U1899
	SOT-23	• SST111, SST112, SST113 SST4091, SST4092, SST4093 SST4391, SST4392, SST4393 SST4856, SST4857, SST4858, SST4859, SST4860, SST4861
	TO-18	• 2N4091, 2N4092, 2N4093 2N4391, 2N4392, 2N4393 2N4856, 2N4857, 2N4858, 2N4859, 2N4860, 2N4861 2N4856A, 2N4857A, 2N4858A, 2N4859A, 2N4860A, 2N4861A VCR2N
Dual	TO-71	• 2N5564, 2N5565, 2N5566
Single	Chip	• All of the above specifications are available
Dual	Chip	• 2N5566 specification available

SWITCHING CIRCUITS



2N4091 through 2N4093
2N4856 through 2N4861

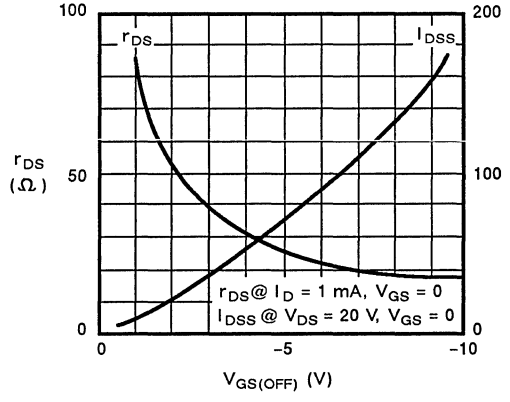


2N4391 through 2N4393

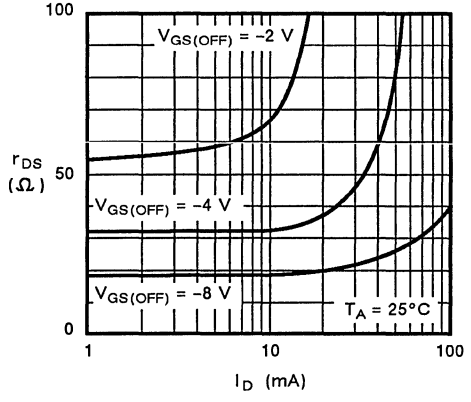
7

TYPICAL CHARACTERISTICS

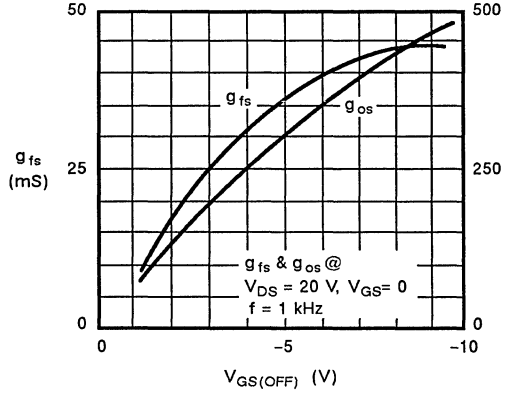
On-Resistance & Drain Current vs. Gate-Source Cutoff Voltage



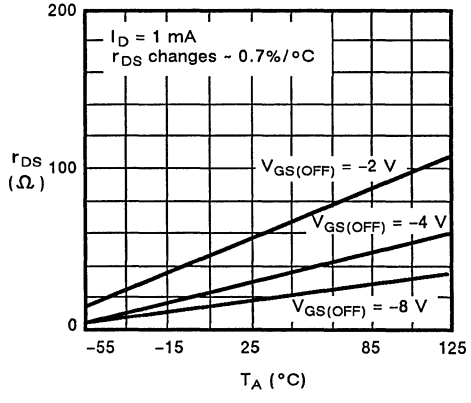
On-Resistance vs. Drain Current



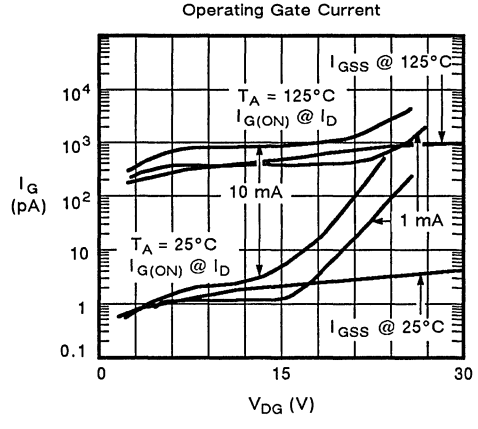
Forward Transconductance & Output Conductance vs. Gate-Source Cutoff Voltage



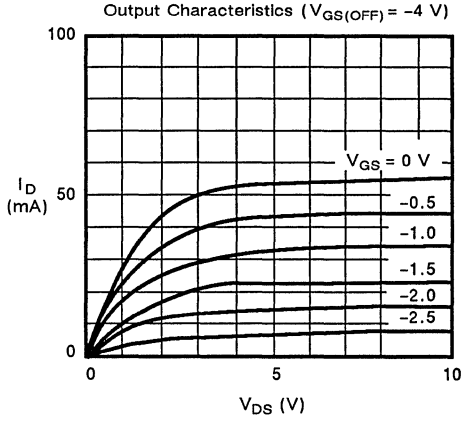
On-Resistance vs. Temperature



Operating Gate Current

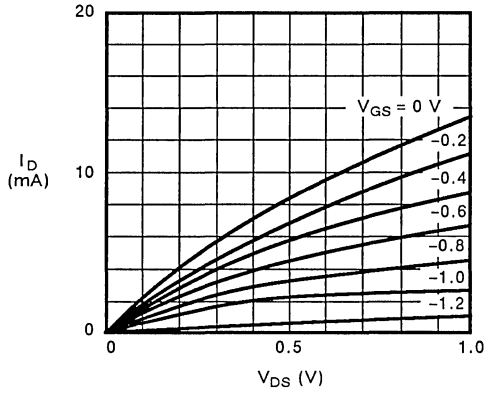


Output Characteristics ($V_{GS(OFF)}$ = -4 V)

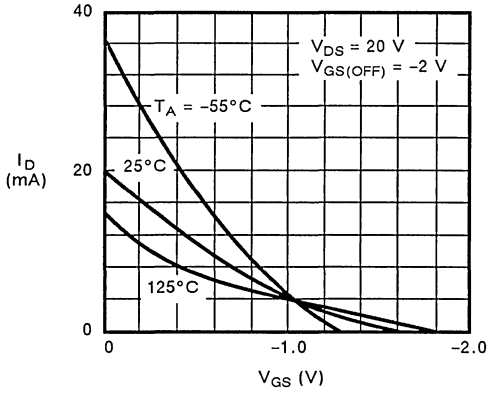


TYPICAL CHARACTERISTICS

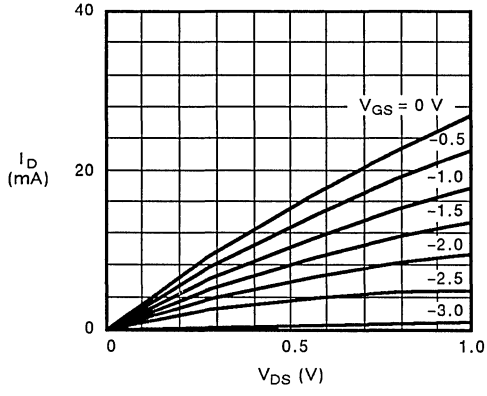
Output Characteristics ($V_{GS(OFF)}$ = -2 V)



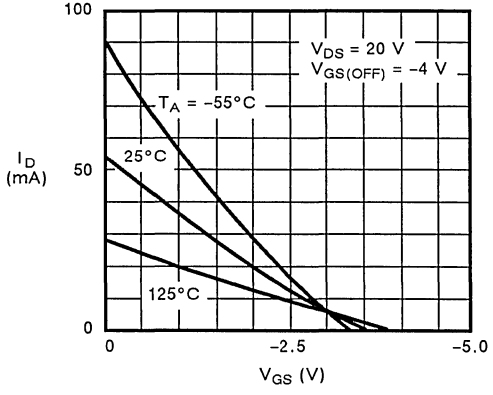
Transfer Characteristics



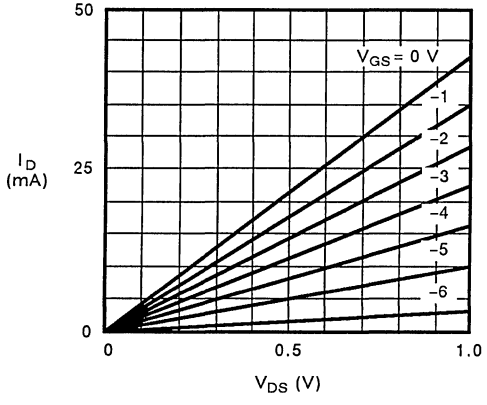
Output Characteristics ($V_{GS(OFF)}$ = -4 V)



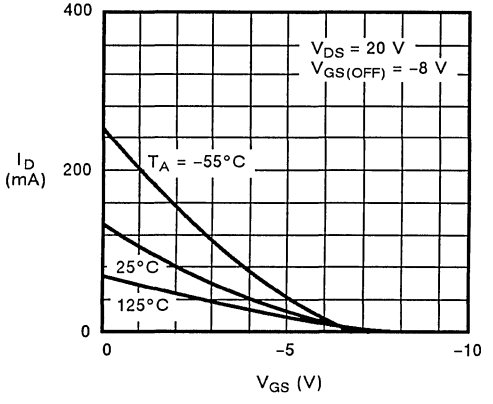
Transfer Characteristics



Output Characteristics ($V_{GS(OFF)}$ = -8 V)



Transfer Characteristics



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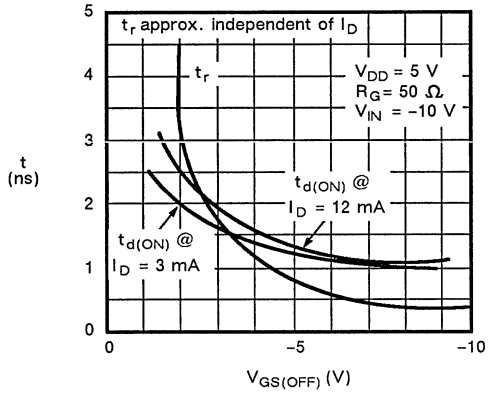
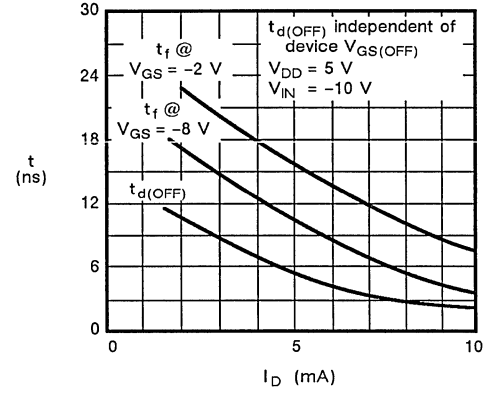
TYPICAL CHARACTERISTICS

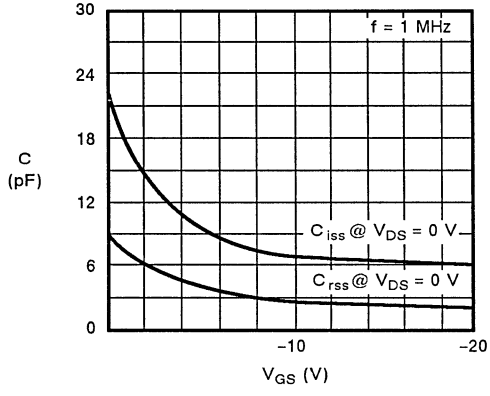
Turn-On Switching



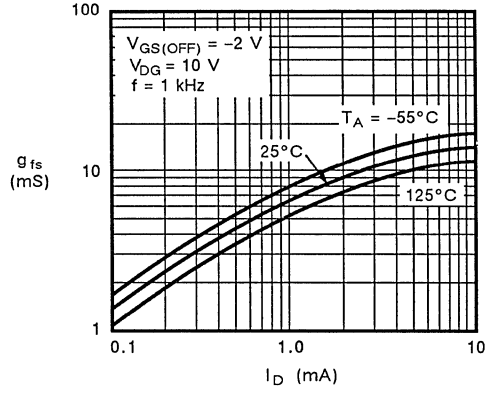
Turn-Off Switching



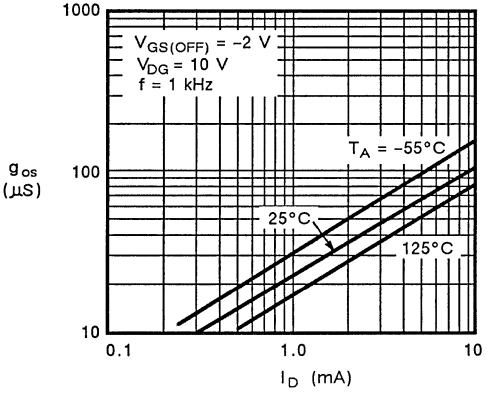
Capacitance vs. Gate-Source Voltage



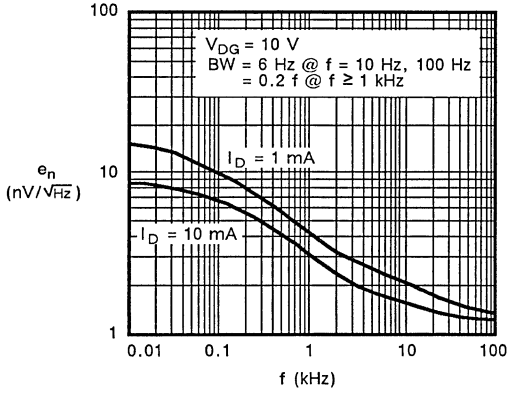
Transconductance vs. Drain Current



Output Conductance vs. Drain Current

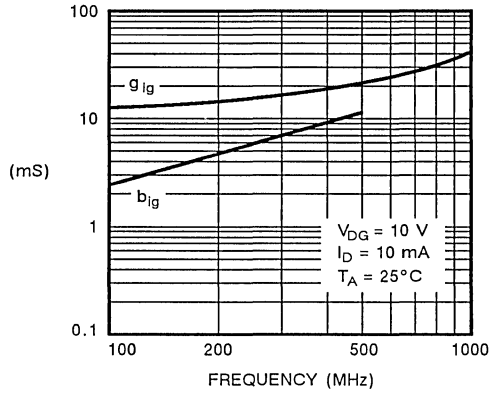


Noise Voltage vs. Frequency

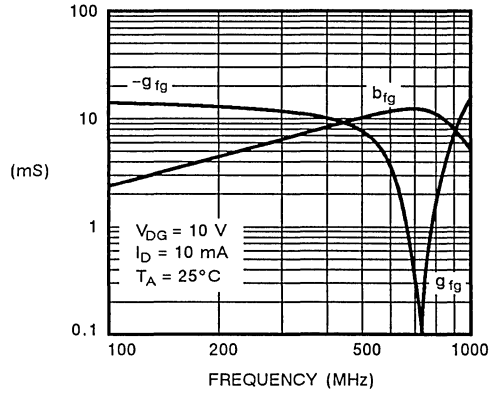


TYPICAL CHARACTERISTICS

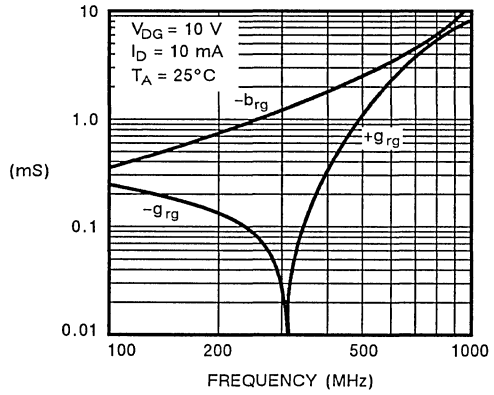
Common-Gate Input Admittance



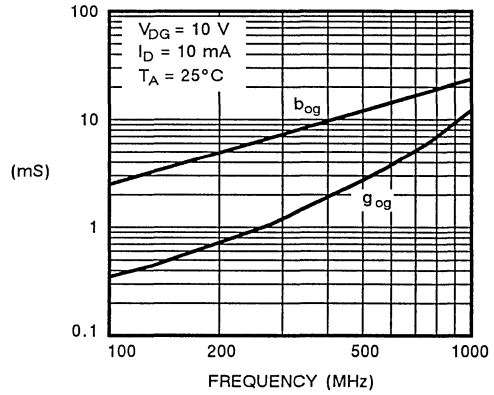
Common-Gate Forward Admittance



Common-Gate Reverse Admittance



Common-Gate Output Admittance



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N-Channel JFET Current Regulator Diode

DESIGNED FOR:

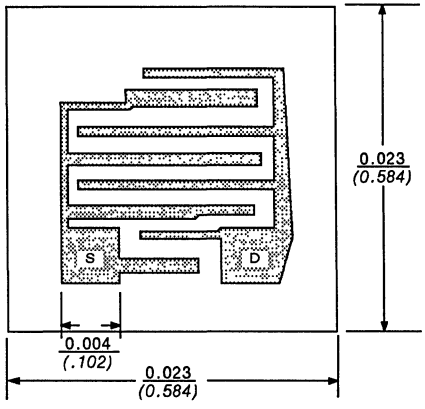
- Current Regulation
- Current Limiting
- Biasing

FEATURES

- Simple Two Lead Current Source
- 1 to 100 V Operation
- 0 Temperature Coefficient
- Simplifies Floating Current Sources
  No power supplies required

TYPE	PACKAGE	DEVICE
Single	TO-92	• J501, J502, J503, J505, J506, J507, J508, J509, J510, J511 J553, J554, J555, J556, J557
	Chip	• Available as above specifications

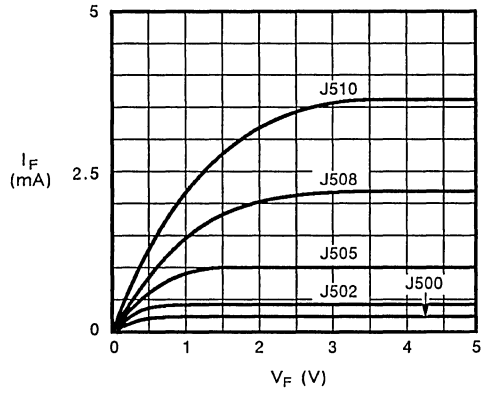
GEOMETRY DIAGRAM



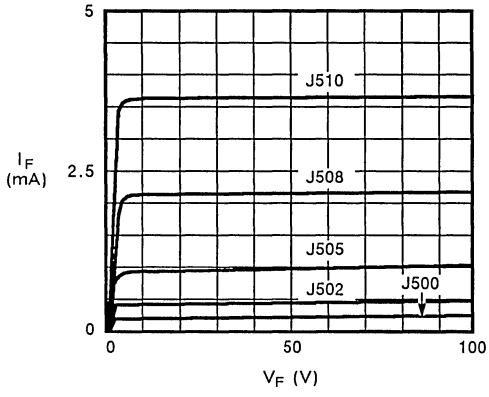
Gate is backside contact

TYPICAL CHARACTERISTICS

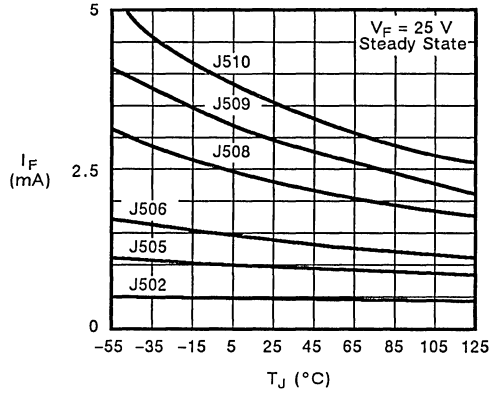
Output Current vs. Forward Voltage



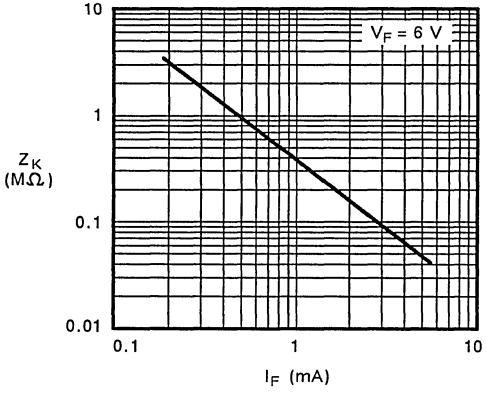
Output Current vs. Forward Voltage



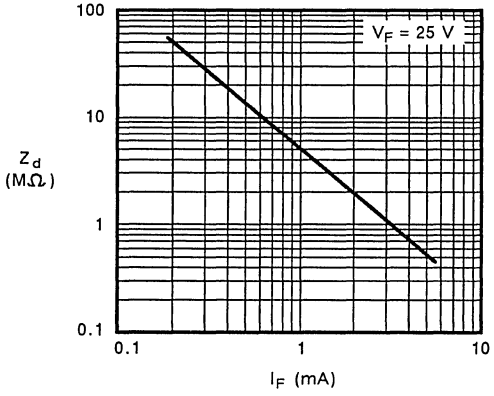
Limiting Current vs. Temperature



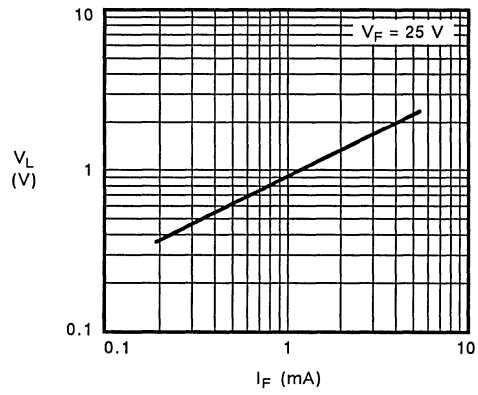
Knee Impedance vs. Regulator Current



Dynamic Impedance vs. Regulator Current



Limiting Voltage @ 0.8 I_F vs. Regulator Current



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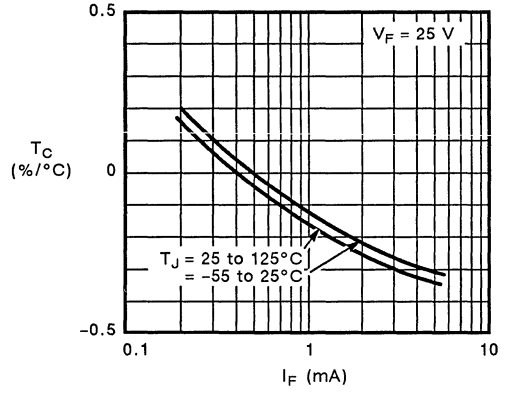
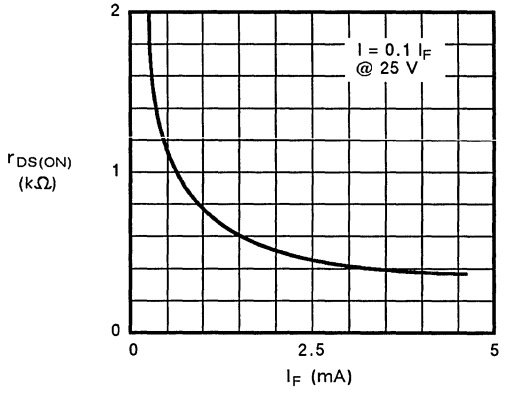
TYPICAL CHARACTERISTICS

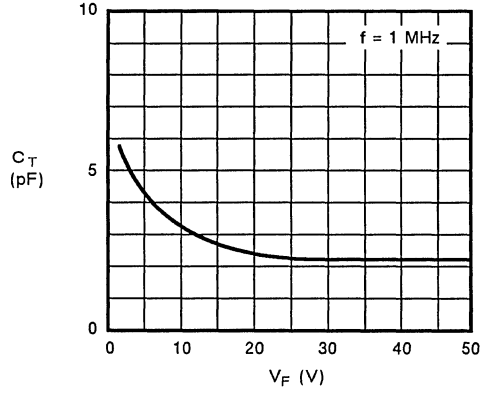
Temperature Coefficient vs. Regulator Current



On-Resistance vs. Regulator Current



Capacitance vs. Forward Voltage



N-Channel JFET

DESIGNED FOR:

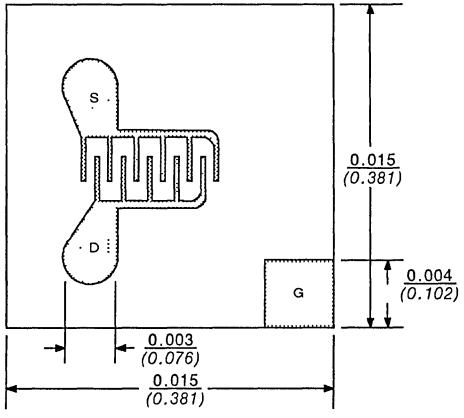
- VHF/UFF Amplifiers
- Oscillators
- Mixers
- Low Input Capacitance High Speed Switch

FEATURES

- Low Noise
  nF = 3 dB Typical at 400 MHz
- Wideband High g_{fs}/C_{iss} Ratio

TYPE	PACKAGE	DEVICE
Single	TO-92	• 2N3819 2N5484, 2N5485, 2N5486 BF244A, BF244B, BF244C BF245A,BF245B, BF245C J304, J305 PN4416
	SOT-23	• SST4416
	TO-72	• 2N4416, 2N4416A
	Chip	• Available as above specifications

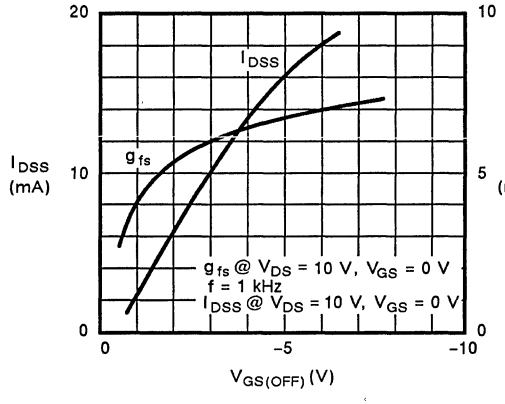
GEOMETRY DIAGRAM



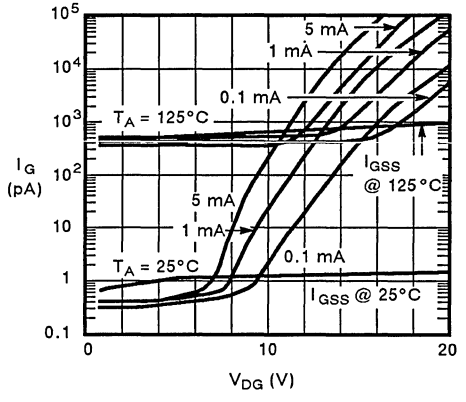
Gate also backside contact

TYPICAL CHARACTERISTICS

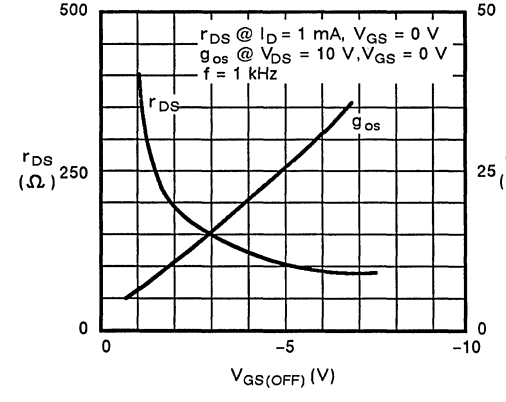
Drain Current & Transconductance vs. Gate-Source Cutoff Voltage



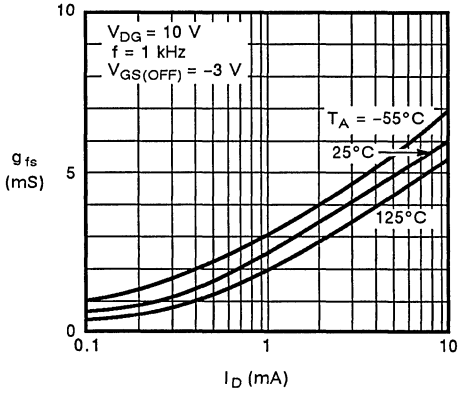
Leakage Current vs. Drain Voltage



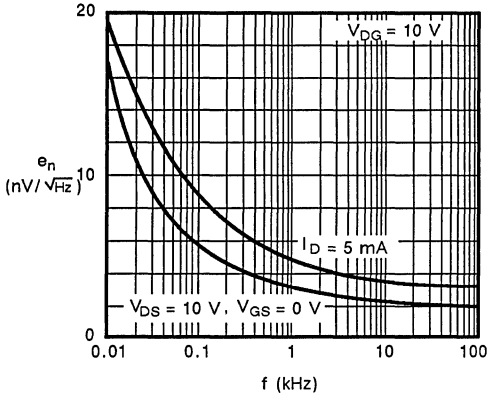
On-Resistance & Output Conductance vs. Gate-Source Cutoff Voltage



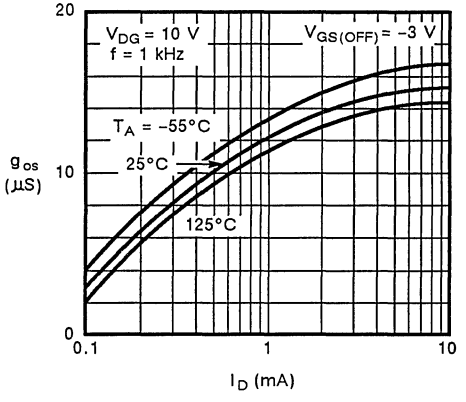
Common-Source Forward Transconductance vs. Drain Current



Equivalent Input Noise Voltage vs. Frequency

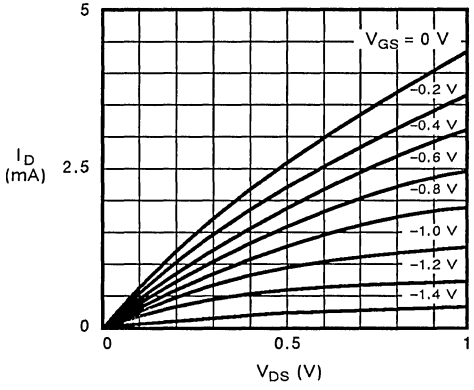


Output Conductance vs. Drain Current

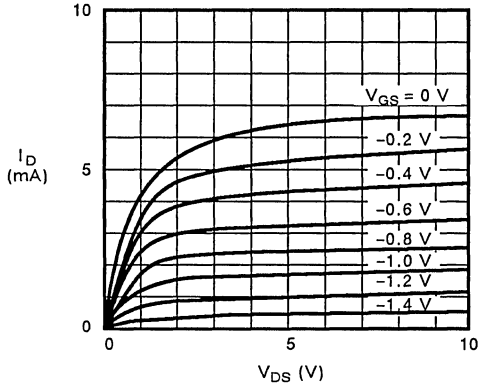


TYPICAL CHARACTERISTICS

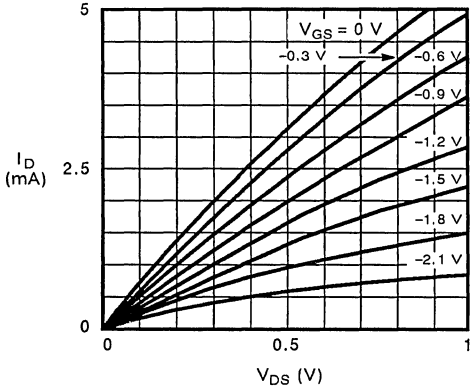
Output Characteristics ($V_{GS(OFF)}$ = −2 V)



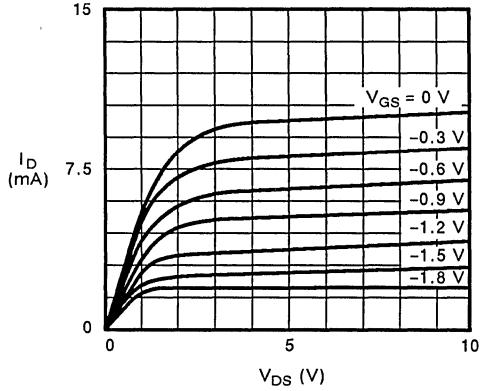
Output Characteristics ($V_{GS(OFF)}$ = −2 V)



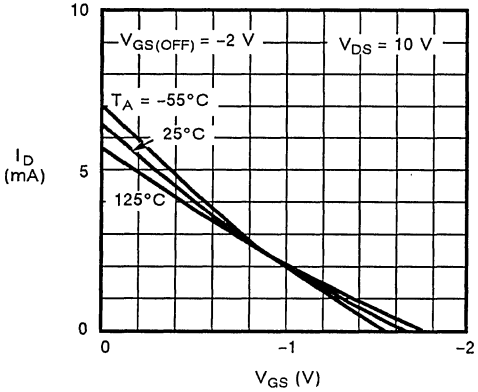
Output Characteristics ($V_{GS(OFF)}$ = −3 V)



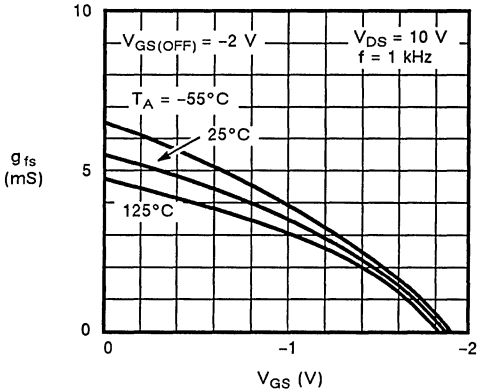
Output Characteristics ($V_{GS(OFF)}$ = −3 V)



Transfer Characteristics



Transconductance vs. Gate-Source Voltage



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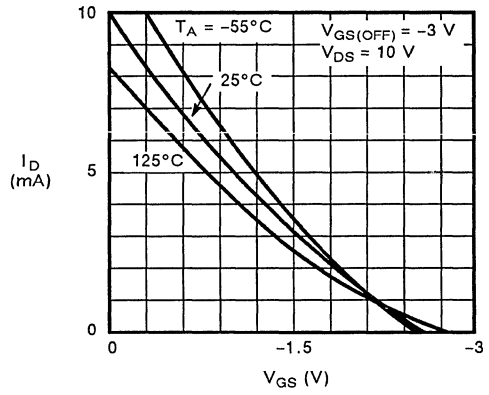
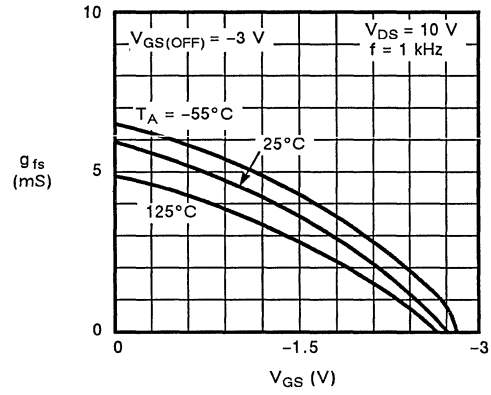
TYPICAL CHARACTERISTICS

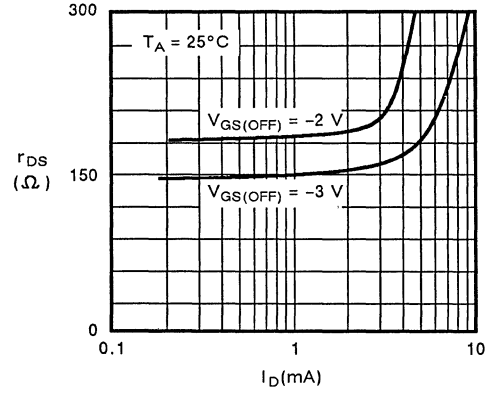
Transfer Characteristics



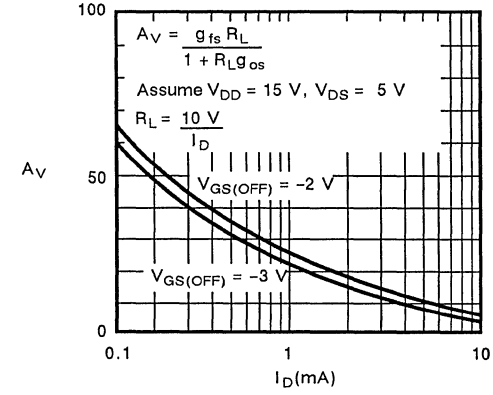
Transconductance vs. Gate-Source Voltage



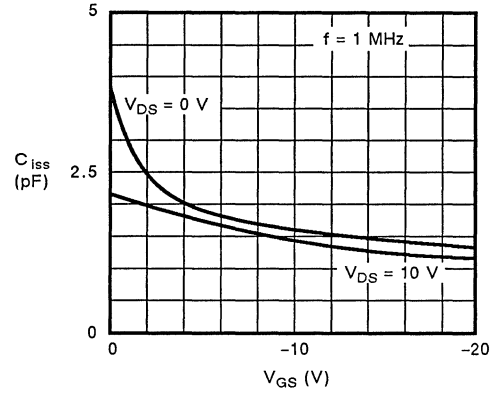
On-Resistance vs. Drain Current



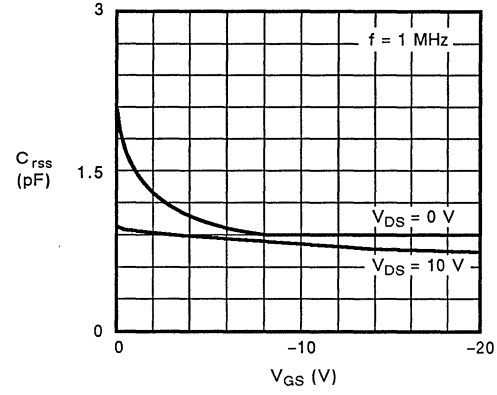
Circuit Voltage Gain vs. Drain Current



Common-Source Input Capacitance vs. Gate-Source Voltage

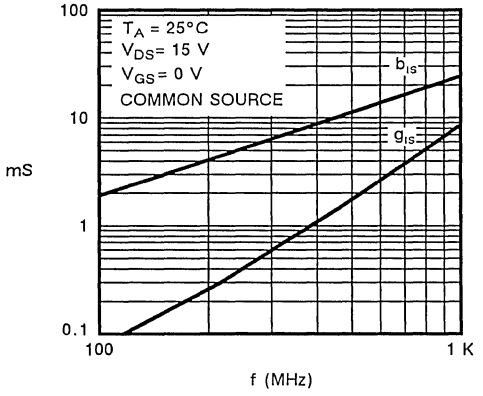


Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage

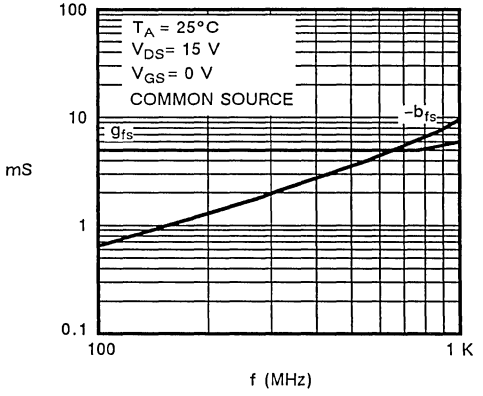


TYPICAL CHARACTERISTICS

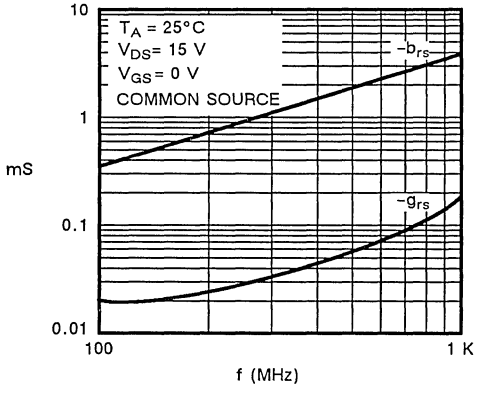
Input Admittance



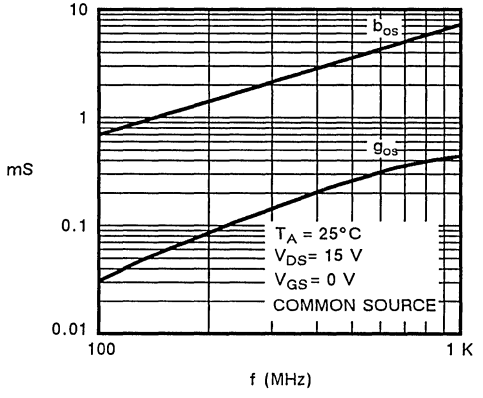
Forward Admittance



Reverse Admittance



Output Admittance



7

Siliconix incorporated

N-Channel JFET

DESIGNED FOR:

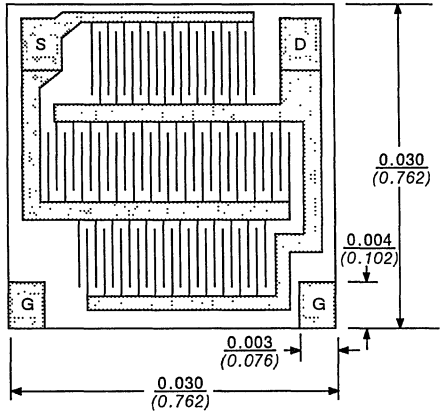
- Low ON Resistance Analog Switches
- Commutators
- Choppers
- Integrator Reset Capacitors
- Low Noise Audio Amplifiers

TYPE	PACKAGE	DEVICE
Single	TO-92	• J108, J109, J110, J110A
	SOT-23	• SST108, SST109, SST110
	TO-52	• 2N5432, 2N5433, 2N5434
	Chip	• Available as above specifications

FEATURES

- Low Insertion Loss
- Small Error in Measurement Systems
  $V_{DS(on)}$ < 50 mV (2N5432)
- High Off-Isolation $I_{D(OFF)}$ < 200 pA
- High Speed $t_{d(on)}$ < 4 ns
  Low Noise Audio-Frequency Amplification
  $\bar{e}_n$ < 2 nV/$\sqrt{Hz}$ at 1 kHz

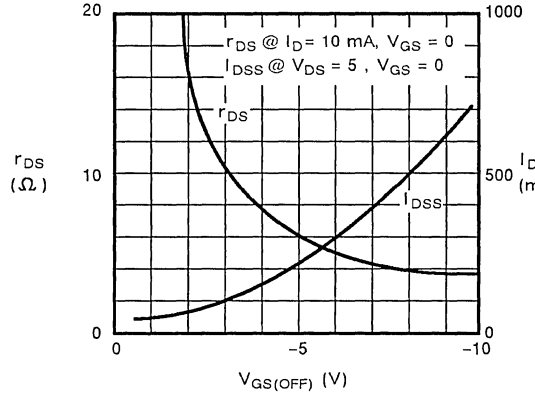
GEOMETRY DIAGRAM



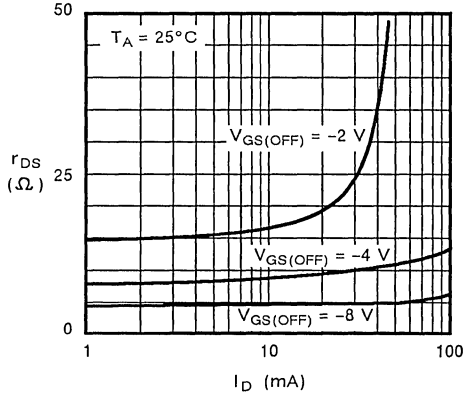
Gate also backside contact

TYPICAL CHARACTERISTICS

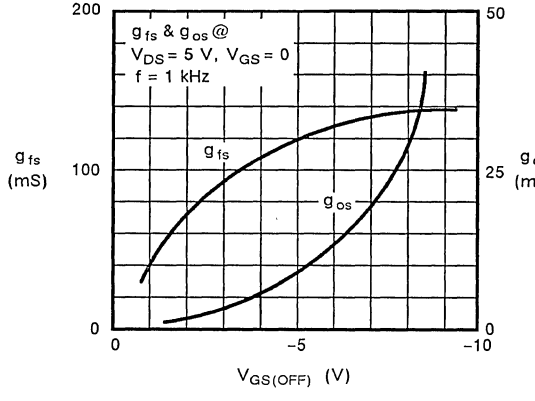
On-Resistance & Drain Current vs. Gate-Source Cutoff Voltage



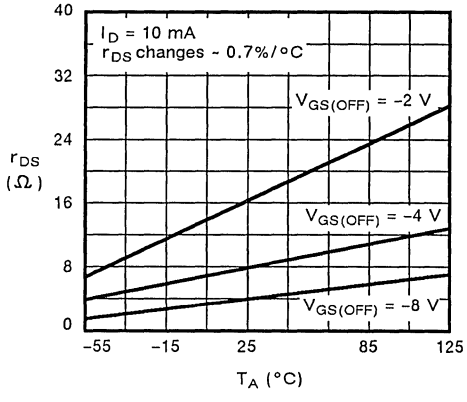
On-Resistance vs. Drain Current



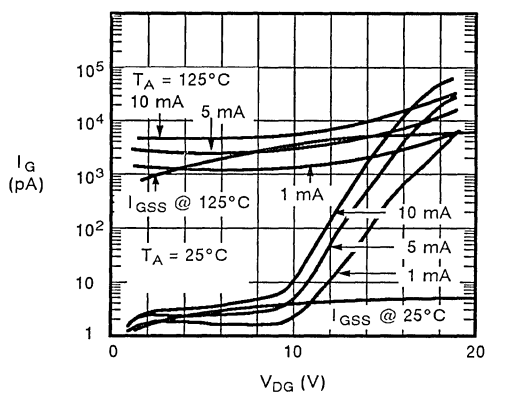
Forward Transconductance & Output Conductance vs. Gate-Source Cutoff Voltage



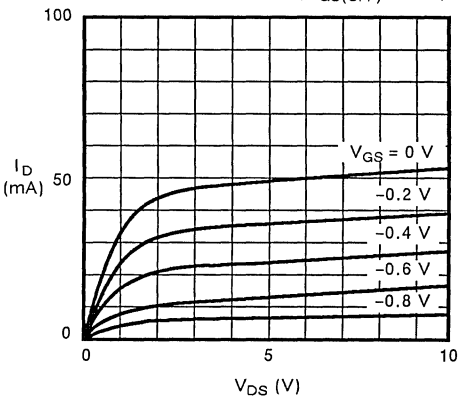
On-Resistance vs. Temperature



Operating Gate Current



Output Characteristics ($V_{GS(OFF)}$ = -2 V)



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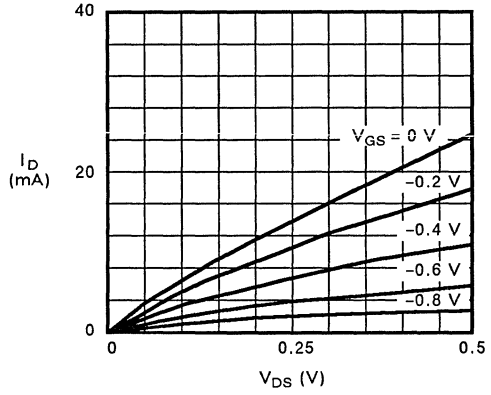
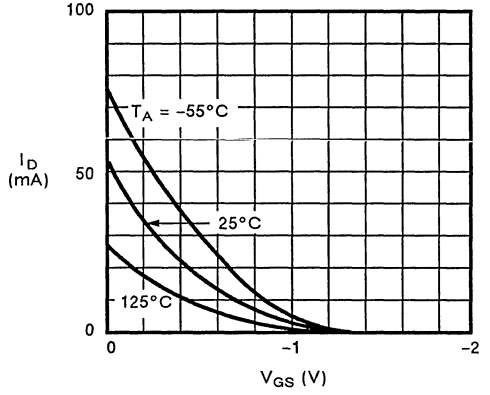
TYPICAL CHARACTERISTICS

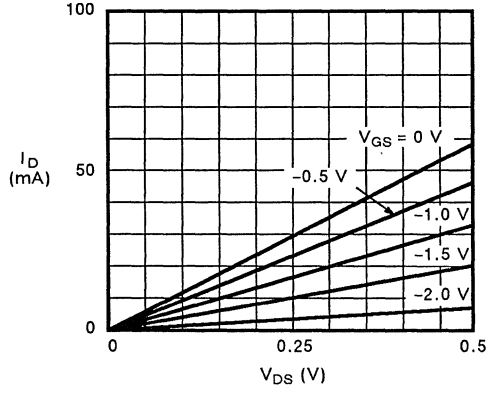
Output Characteristics ($V_{GS(OFF)}$ = −2 V)



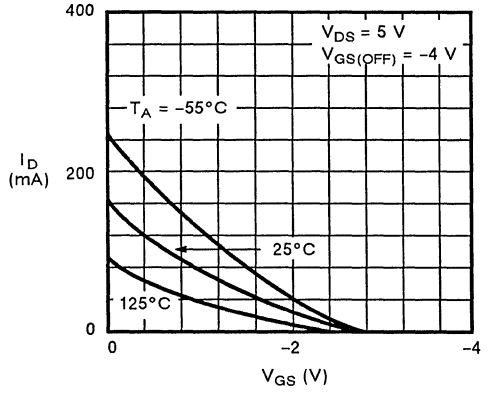
Transfer Characteristics



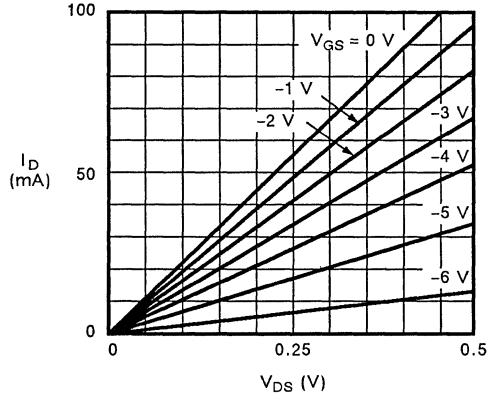
Output Characteristics ($V_{GS(OFF)}$ = −4 V)



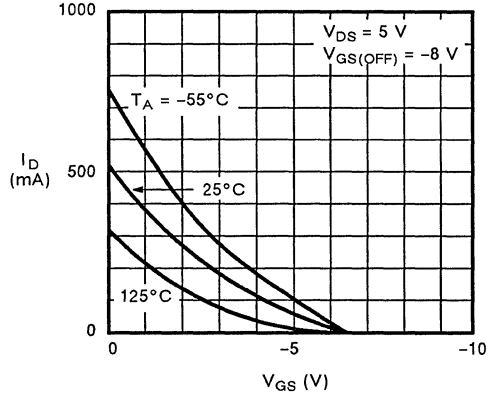
Transfer Characteristics



Output Characteristics ($V_{GS(OFF)}$ = −8 V)

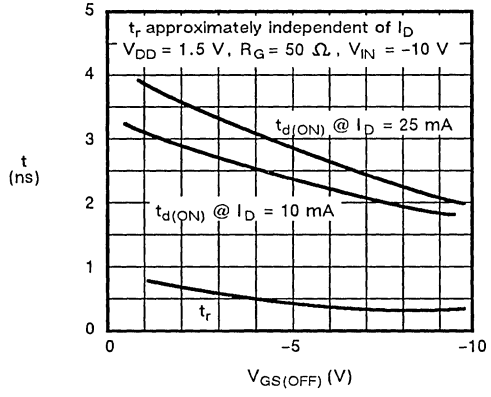


Transfer Characteristics

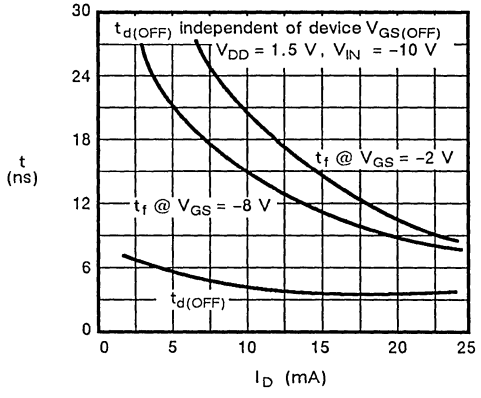


TYPICAL CHARACTERISTICS

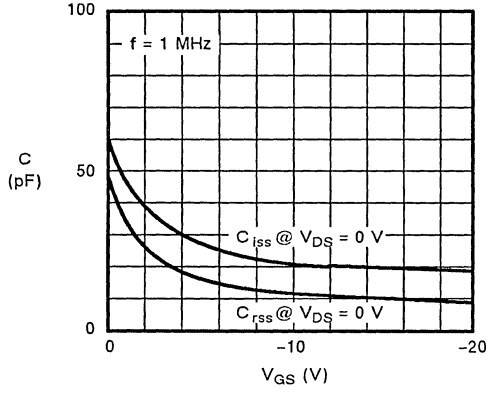
Turn-On Switching



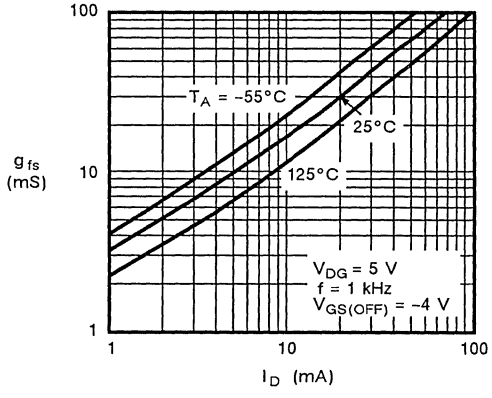
Turn-Off Switching



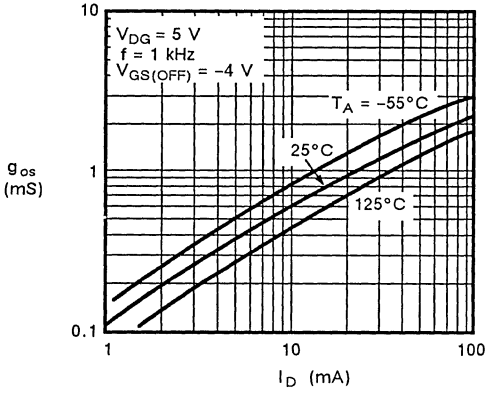
Capacitance vs. Gate-Source Voltage



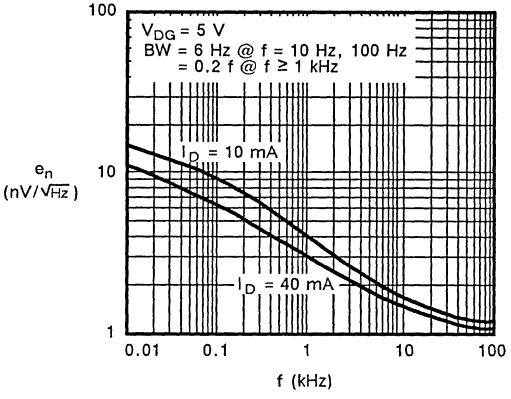
Transconductance vs. Drain Current



Output Conductance vs. Drain Current



Noise Voltage vs. Frequency



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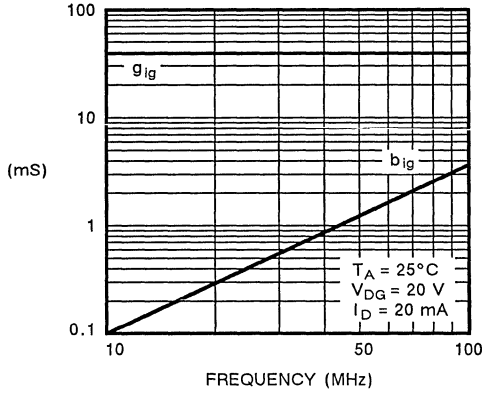
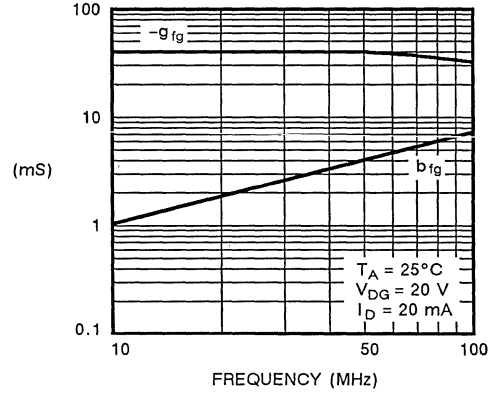
TYPICAL CHARACTERISTICS

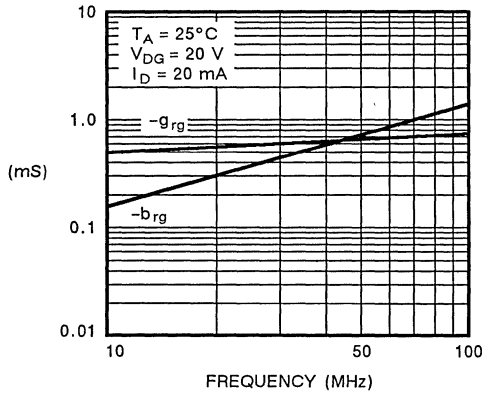
Common Gate Input Admittance



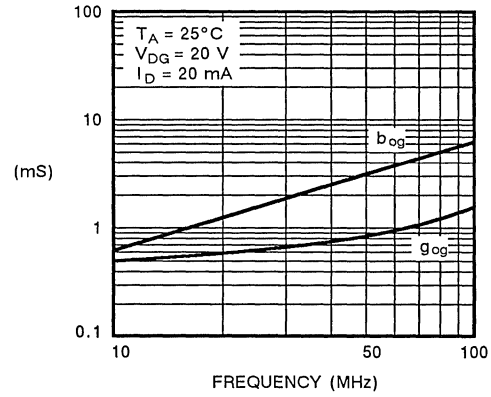
Common Gate Forward Admittance



Common Gate Reverse Admittance



Common Gate Output Admittance



N-Channel JFET Current Regulator Diode

DESIGNED FOR:

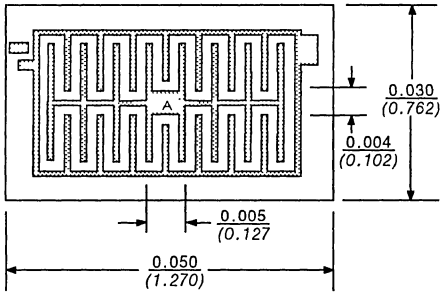
- Current Regulation
- Current Limiting
- Baising
- Low Voltage References

TYPE	PACKAGE	DEVICE
Single	TO-18	• CR022 through CR062 CRR0240 through CRR0560
	Chip	• Available as above specifications

FEATURES

- Simple Two Leaded Current Source
- Current Insensitive to Temperature Changes
- Tempurature Coefficient Better than 0.15 %/° on all Devices
- Simplifies Floating Current Sources No Power Supply Required

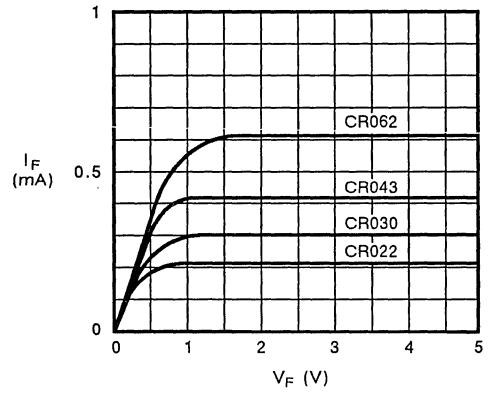
GEOMETRY DIAGRAM



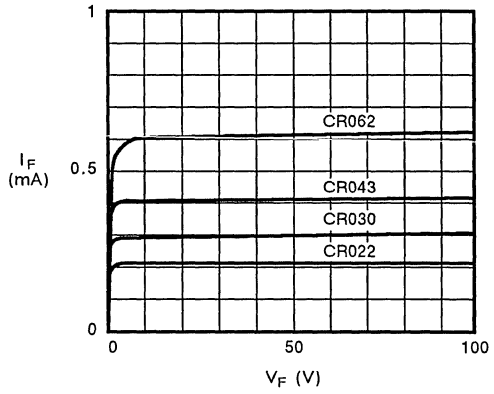
Cathode is backside contact

TYPICAL CHARACTERISTICS

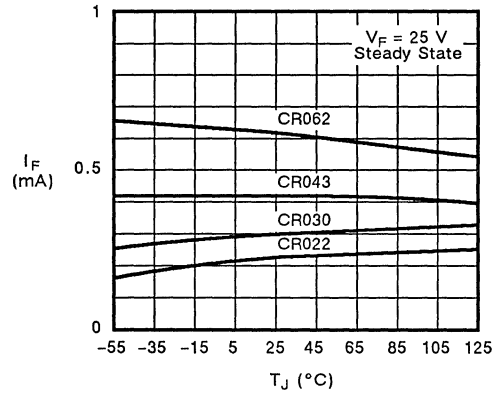
Output Current vs. Forward Voltage



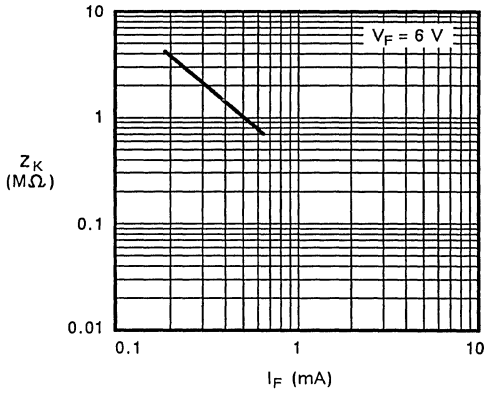
Output Current vs. Forward Voltage



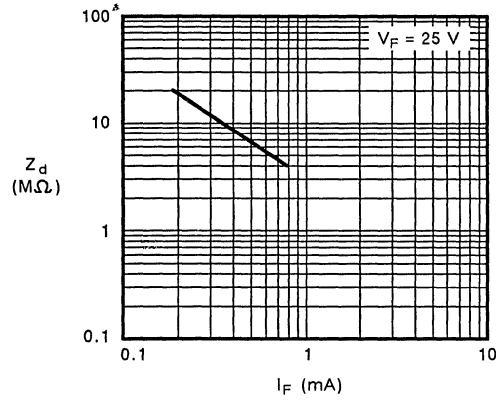
Limiting Current vs. Temperature



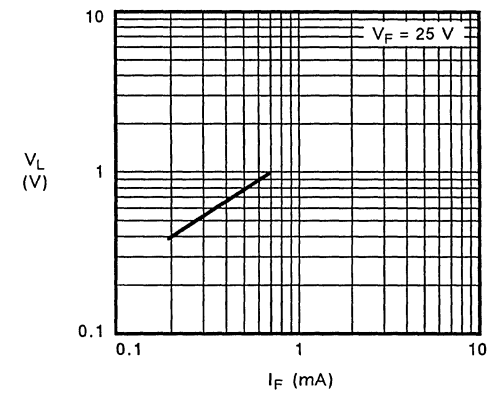
Knee Impedance vs. Regulator Current



Dynamic Impedance vs. Regulator Current

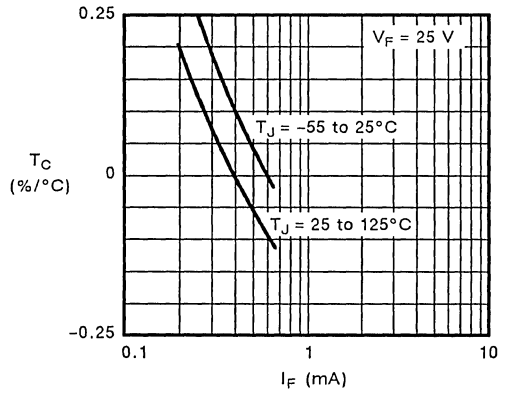


Limiting Voltage @ 0.8 I_F vs. Regulator Current

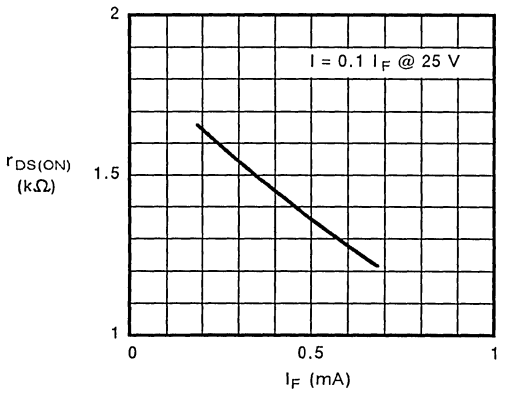


TYPICAL CHARACTERISTICS

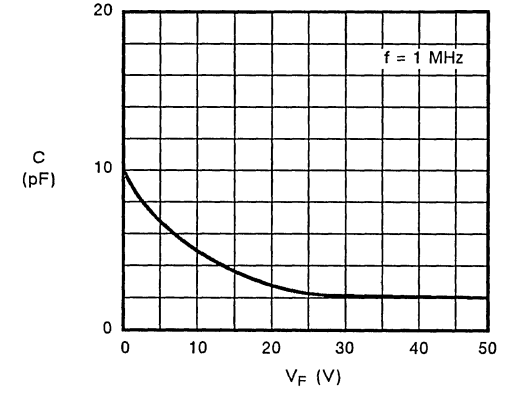
Temperature Coefficient vs. Regulator Current



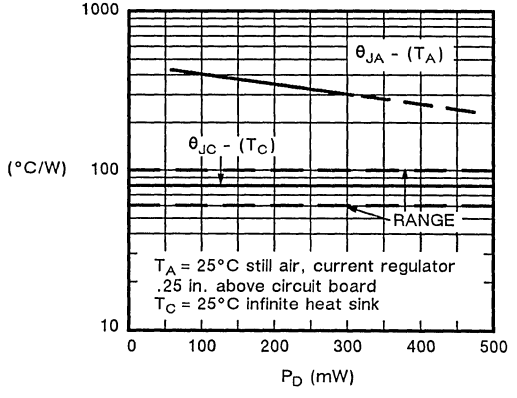
On-Resistance vs. Regulator Current



Capacitance vs. Forward Voltage



Thermal Resistance vs. Power Dissipation



7

N-Channel JFET Current Regulator Diode

DESIGNED FOR:

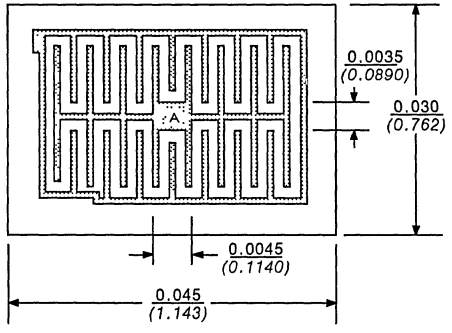
- Current Regulation
- Current Limiting
- Baising
- Low Voltage References

TYPE	PACKAGE	DEVICE
Single	TO-18	• CR068 through CR150 CRR0800 through CRR1250
	Chip	• Available as above specifications

FEATURES

- Simple Two Leaded Current Source
- Current Insensitive to Temperature Changes
- Tempurature Coefficient Better than 0.15 %/°C on all Devices
- Simplifies Floating Current Sources No Power Supply Required

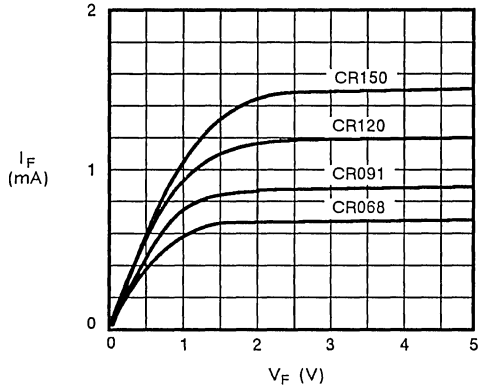
GEOMETRY DIAGRAM



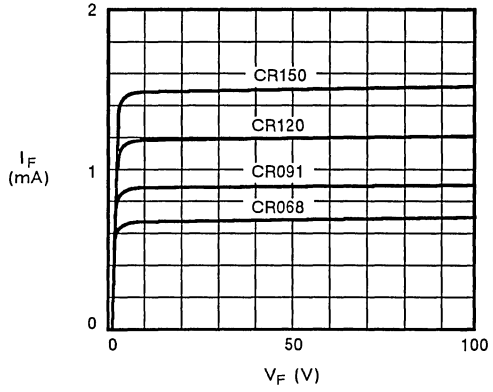
Cathode is backside contact

TYPICAL CHARACTERISTICS

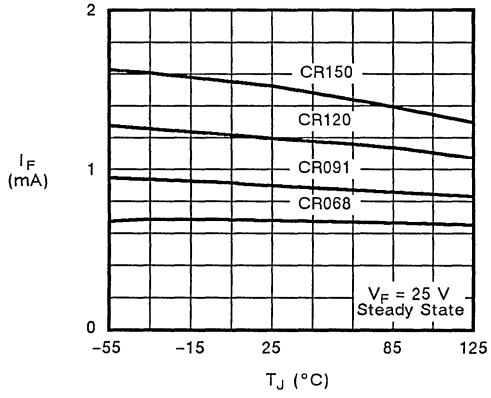
Output Current vs. Forward Voltage



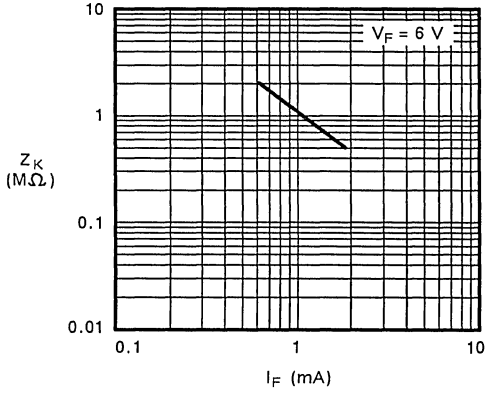
Output Current vs. Forward Voltage



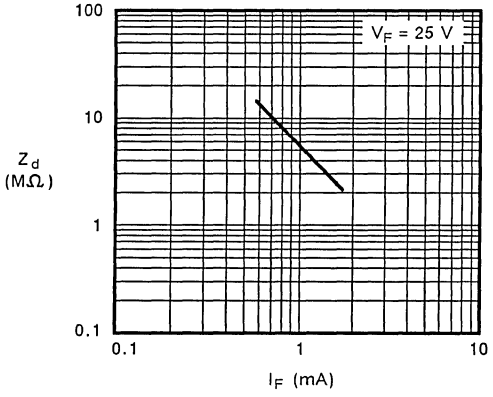
Limiting Current vs. Junction Temperature



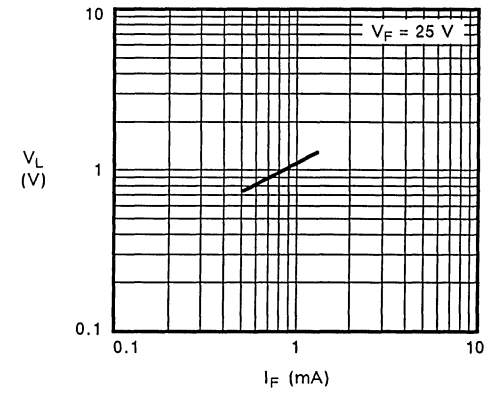
Knee Impedance vs. Regulator Current



Dynamic Impedance vs. Regulator Current



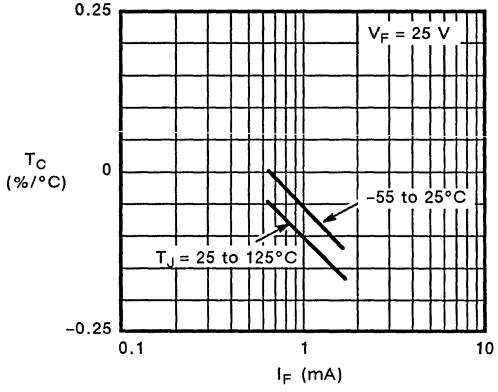
Limiting Voltage @ 0.8 I_F vs. Regulator Current



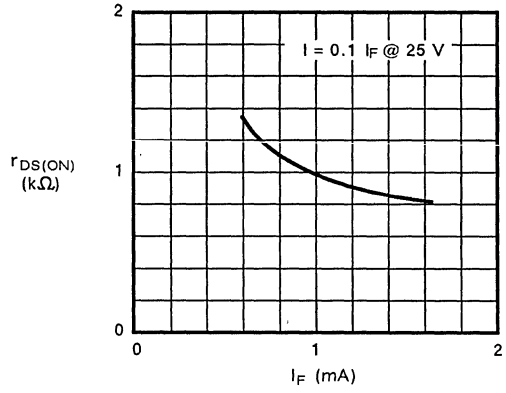
7

TYPICAL CHARACTERISTICS

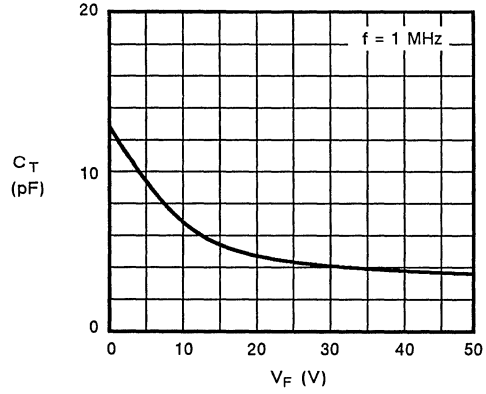
Temperature Coefficient vs. Regulator Current



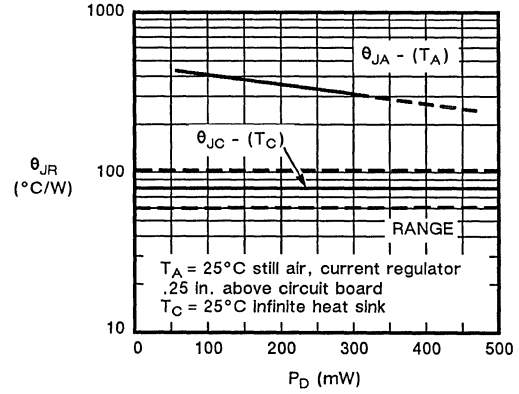
On-Resistance vs. Regulator Current



Capacitance vs. Forward Voltage



Thermal Resistance vs. Power Dissipation



N-Channel JFET Current Regulator Diode

DESIGNED FOR:

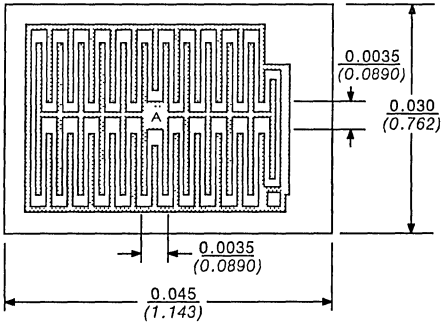
- Current Regulation
- Current Limiting
- Baising
- Low Voltage References

TYPE	PACKAGE	DEVICE
Single	TO-18	• CR160 through CR530 CRR1950 through CRR4300
	Chip	• Available as above specifications

FEATURES

- Simple Two Leaded Current Source
- Current Insensitive to Temperature Changes
- Tempurature Coefficient Better than 0.15 %/°C on all Devices
- Simplifies Floating Current Sources No Power Supply Required

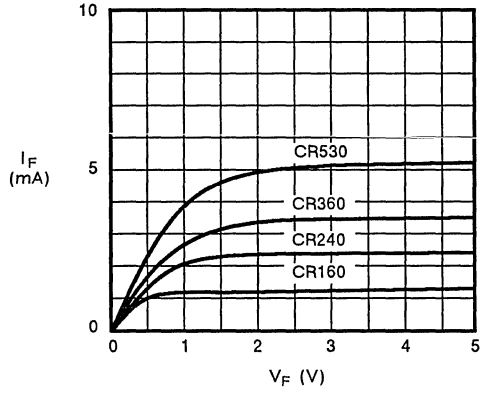
GEOMETRY DIAGRAM



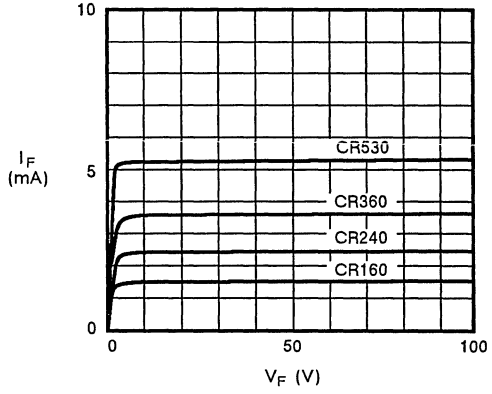
Cathode is backside contact

TYPICAL CHARACTERISTICS

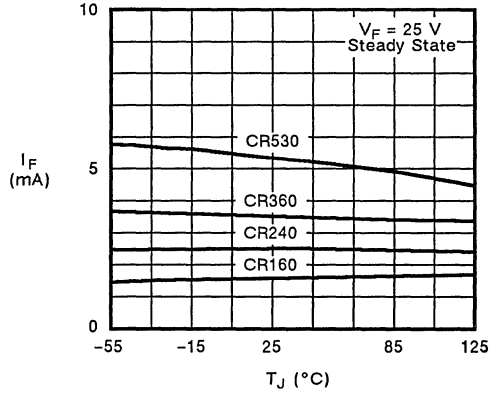
Output Current vs. Forward Voltage



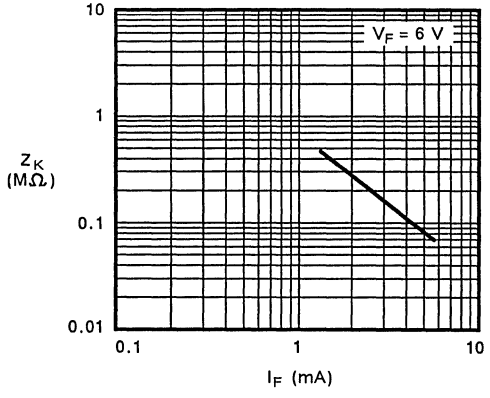
Output Current vs. Forward Voltage



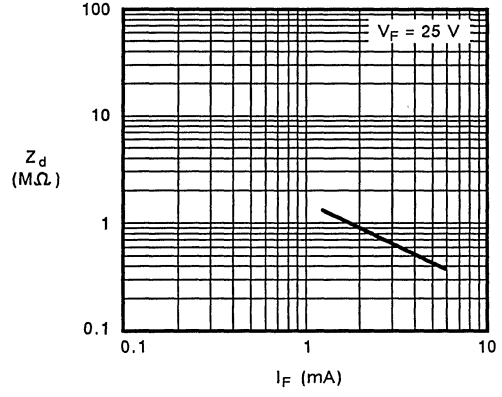
Limiting Current vs. Temperature



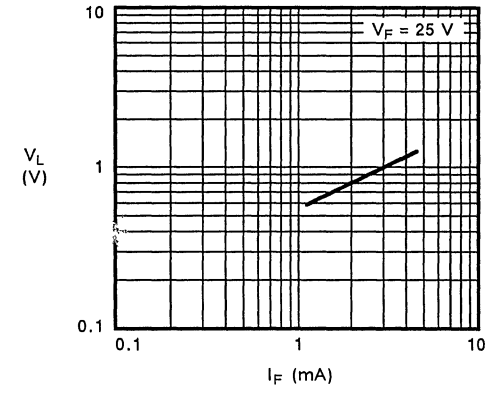
Knee Impedance vs. Regulator Current



Dynamic Impedance vs. Regulator Current

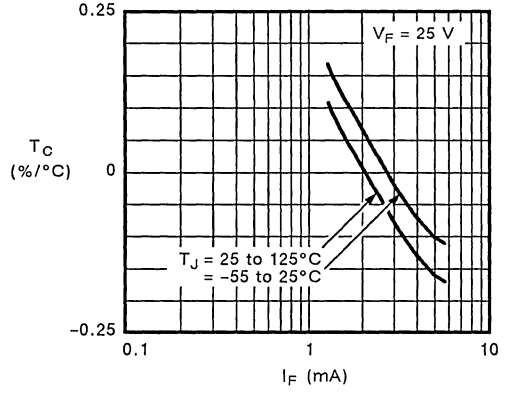


Limiting Voltage @
0.8 I_F vs. Regulator Current

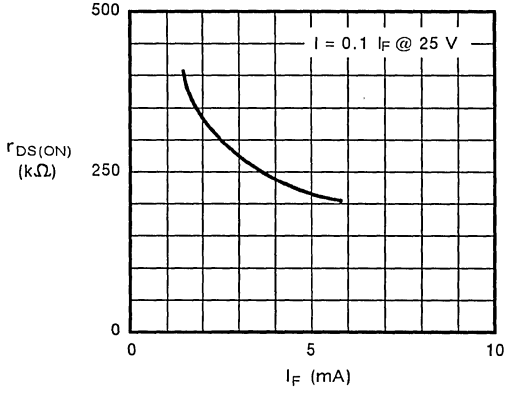


TYPICAL CHARACTERISTICS

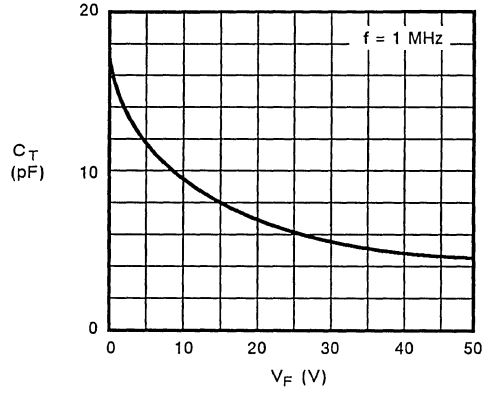
Temperature Coefficient vs. Regulator Current



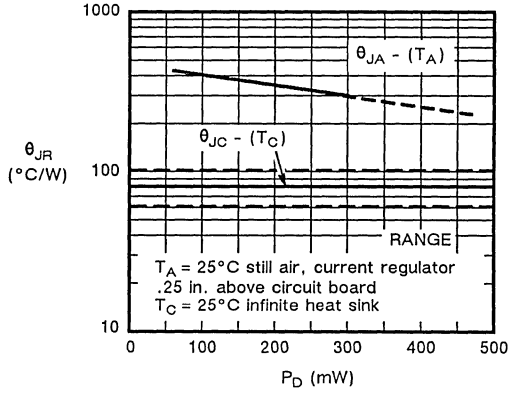
On-Resistance vs. Regulator Current



Capacitance vs. Forward Voltage



Thermal Resistance vs. Power Dissipation



7

Siliconix incorporated

N-Channel JFET Dual Monolithic

DESIGNED FOR:

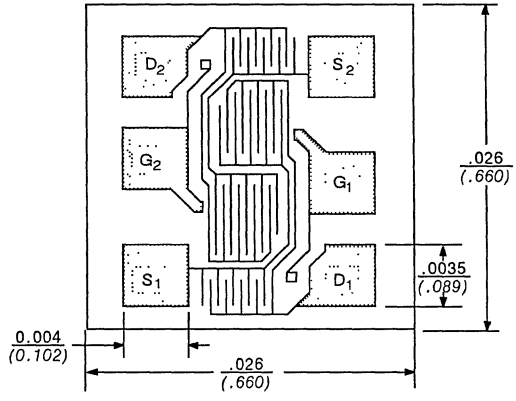
- FET Input Amplifiers
- Low and Medium Frequency Amplifiers
- Impedance Converters
- Precision Instrumentation Amplifiers
- Comparators

TYPE	PACKAGE	DEVICE
Dual	SOIC-8	• SST404, SST405, SST406
	TO-71	• 2N6905, 2N6906, 2N6907 U401, U402, U403, U404, U405, U406
	Chip	• Available as above specifications for U404, U405, & U406 only

FEATURES

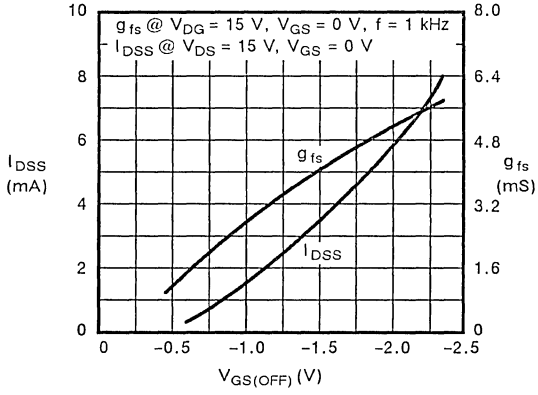
- Minimum System Error and Calibration
  5 mV Offset (U401)
  95 dB Minimum CMRR
- Low Drift with Temperature
  10 μV/°C (U401)
- Simplifies Amplifier Design
  Output Conductance < 2 μS
- Low Noise
  $\bar{e}_n$ = 6 nV/$\sqrt{Hz}$ at 10 Hz Typical

GEOMETRY DIAGRAM

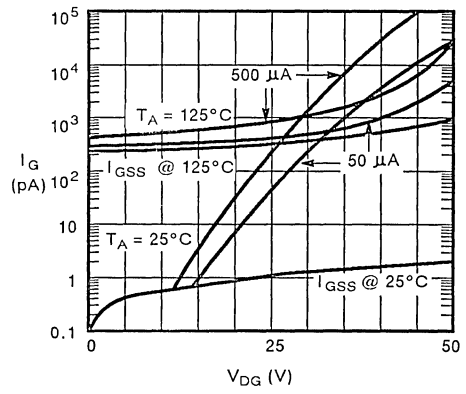


TYPICAL CHARACTERISTICS

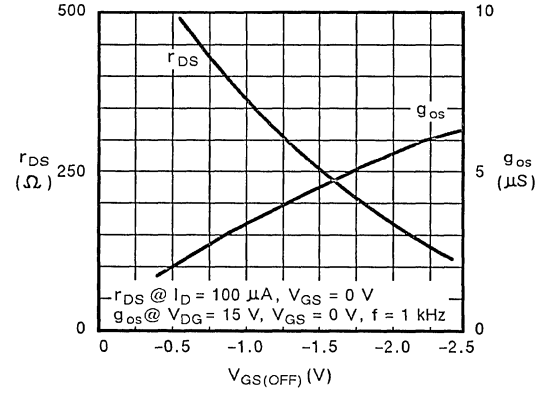
Drain Current & Transconductance vs. Gate-Source Cutoff Voltage



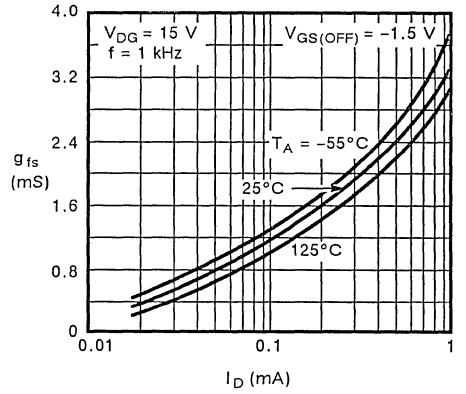
Operating Gate Current



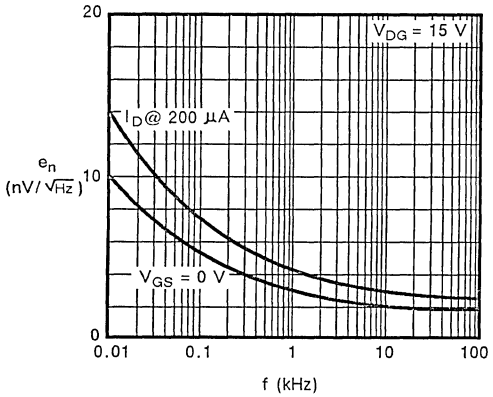
On-Resistance & Output Conductance vs. Gate-Source Cutoff Voltage



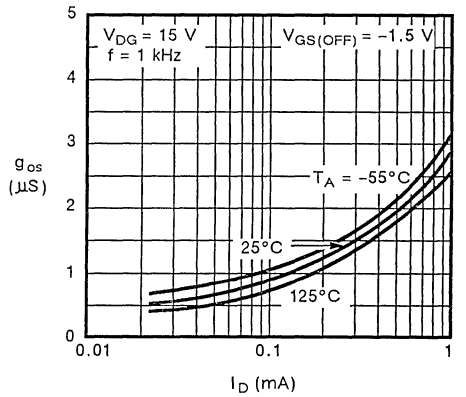
Common-Source Forward Transconductance vs. Drain Current



Equivalent Input Noise Voltage vs. Frequency



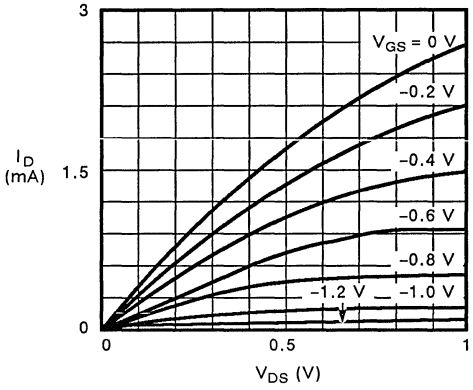
Output Conductance vs. Drain Current



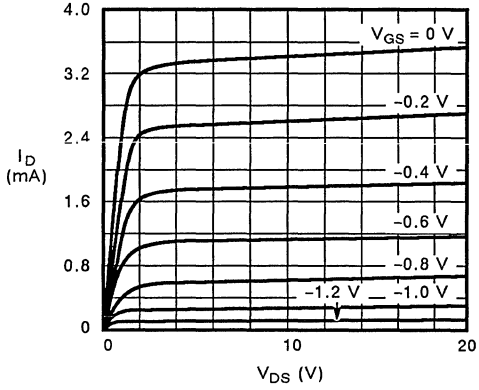
7

TYPICAL CHARACTERISTICS

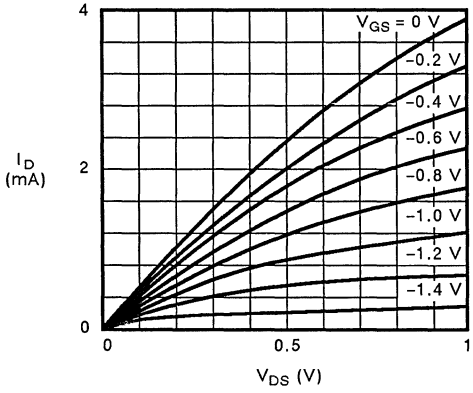
Output Characteristics ($V_{GS(OFF)}$ = -1.5 V)



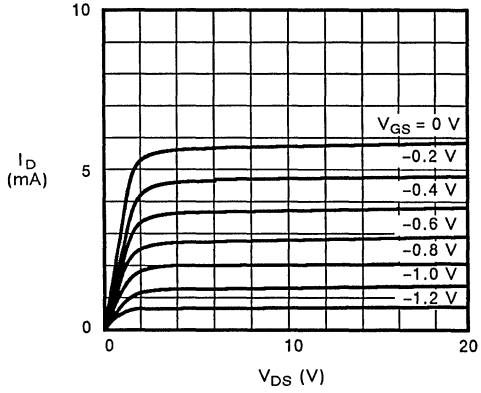
Output Characteristics ($V_{GS(OFF)}$ = -1.5 V)



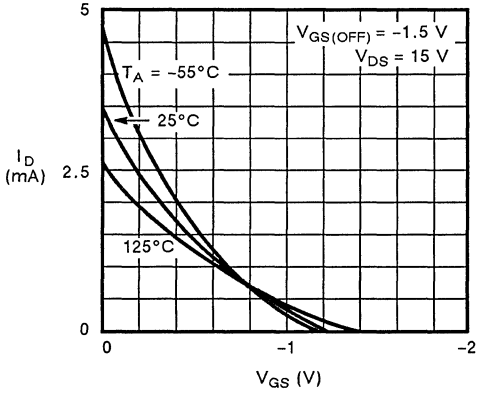
Output Characteristics ($V_{GS(OFF)}$ = -2 V)



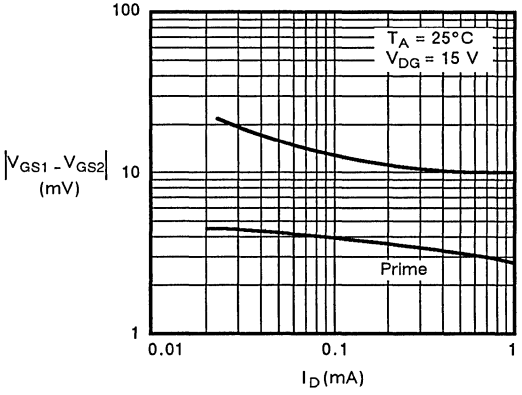
Output Characteristics ($V_{GS(OFF)}$ = -2 V)



Transfer Characteristics

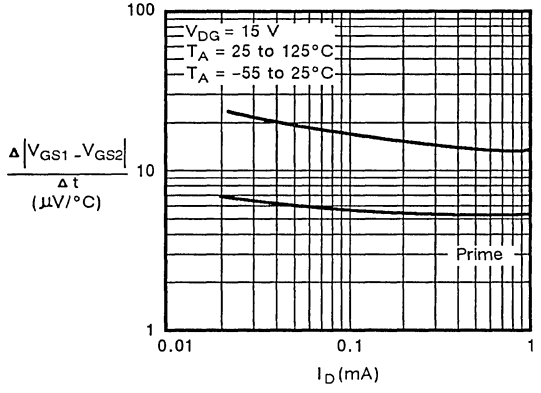


Gate-Source Differential Voltage vs. Drain Current

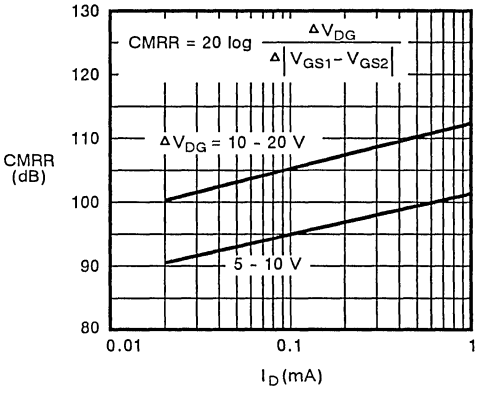


TYPICAL CHARACTERISTICS

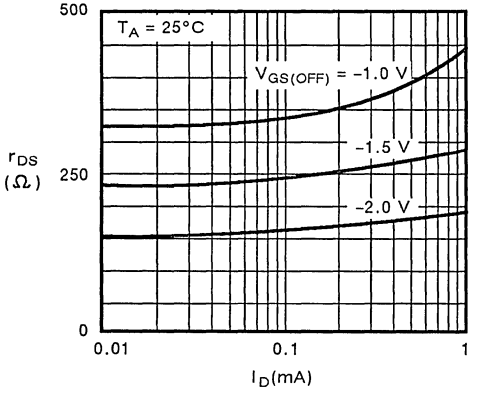
Voltage Differential with Temperature vs. Drain Current



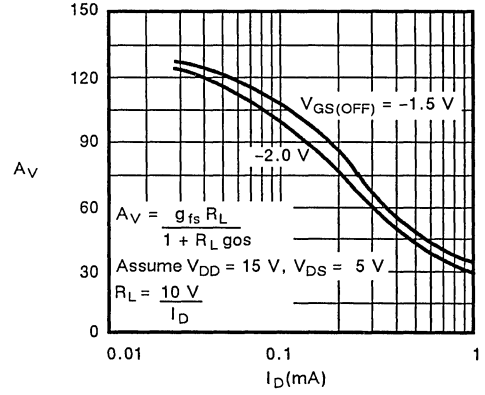
Common Mode Rejection Ratio vs. Drain Current



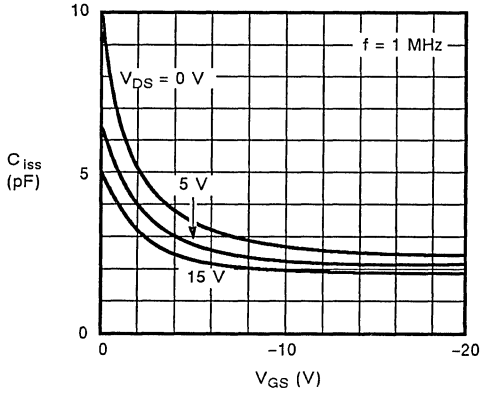
On-Resistance vs. Drain Current



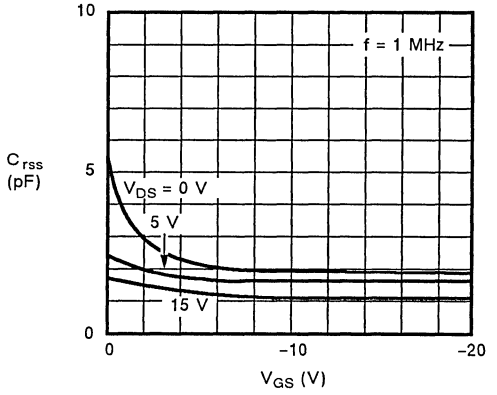
Circuit Voltage Gain vs. Drain Current



Common-Source Input Capacitance vs. Gate-Source Voltage



Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



7

Siliconix incorporated

N-Channel JFET Dual Monolithic

DESIGNED FOR:

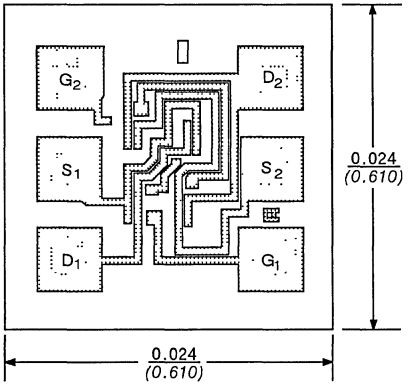
- Ultra Low Leakage FET Input Op Amps
- pH Meters
- Electrometers

FEATURES

- Ultra-High Input Impedance
- Good Voltage Gain
- Low Noise

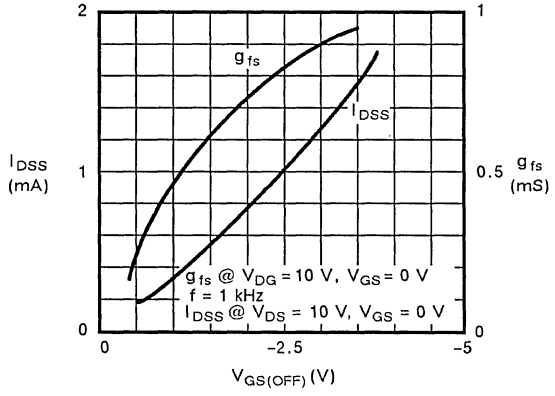
TYPE	PACKAGE	DEVICE
Dual	TO-78	• U421, U422, U423, U424, U425, U426
	Chip	• Available as above specifications for U423, U424, U425, U426

GEOMETRY DIAGRAM

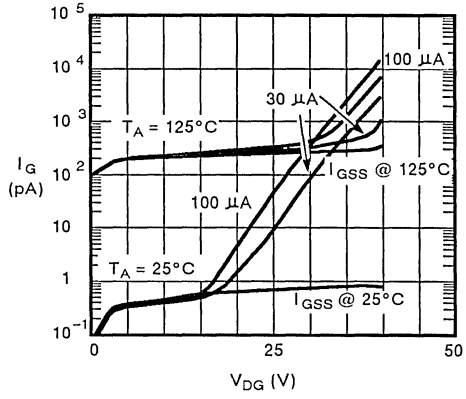


TYPICAL CHARACTERISTICS

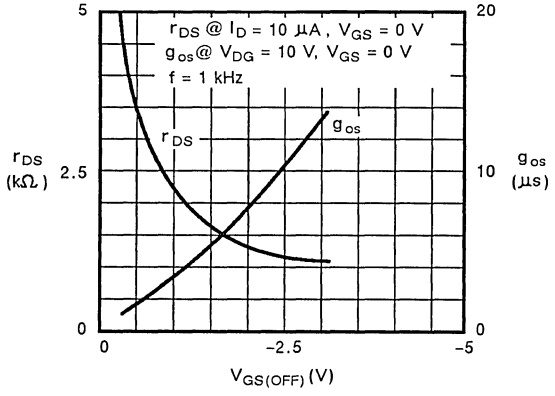
Drain Current & Transconductance vs. Gate-Source Cutoff Voltage



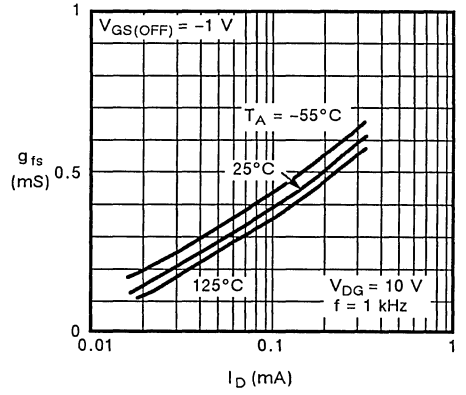
Operating Gate Current



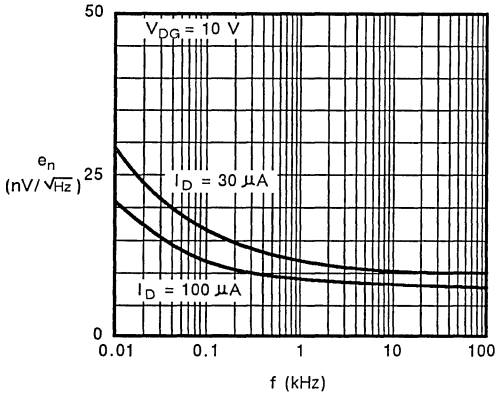
On-Resistance & Output Conductance vs. Gate-Source Cutoff Voltage



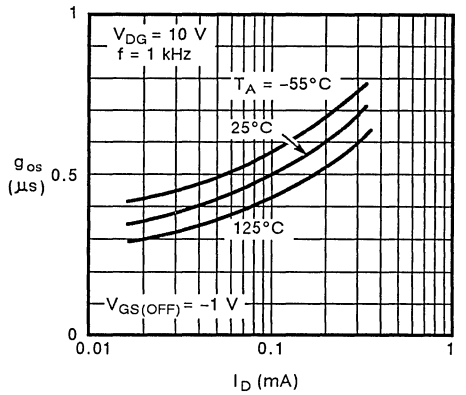
Common-Source Forward Transconductance vs. Drain Current



Equivalent Input Noise Voltage vs. Frequency



Output Conductance vs. Drain Current



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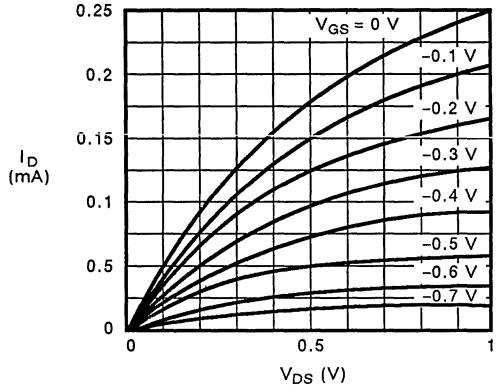
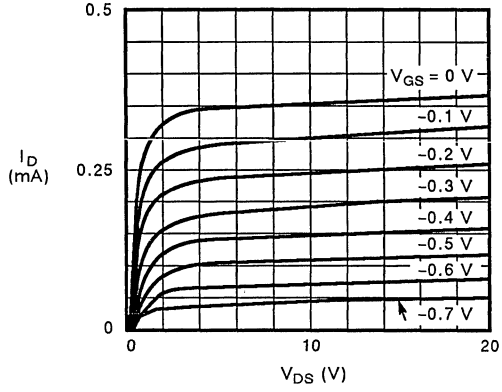
TYPICAL CHARACTERISTICS

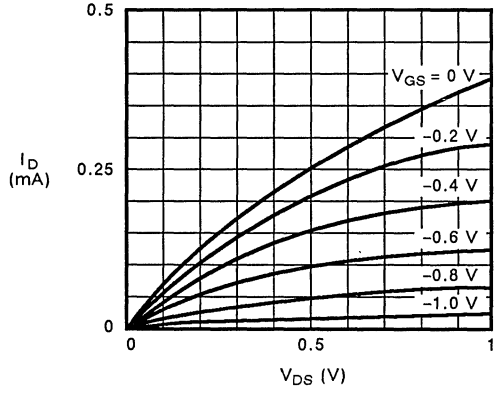
Output Characteristics ($V_{GS(OFF)}$ = -1 V)



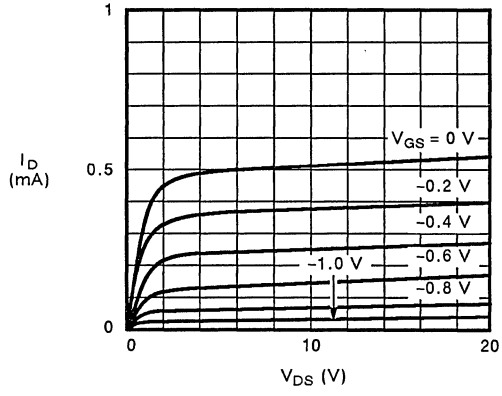
Output Characteristics ($V_{GS(OFF)}$ = -1 V)



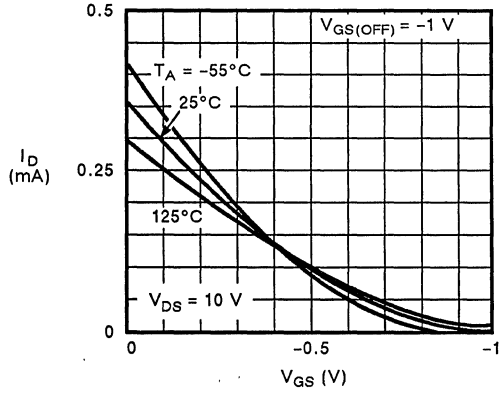
Output Characteristics ($V_{GS(OFF)}$ = -1.5 V)



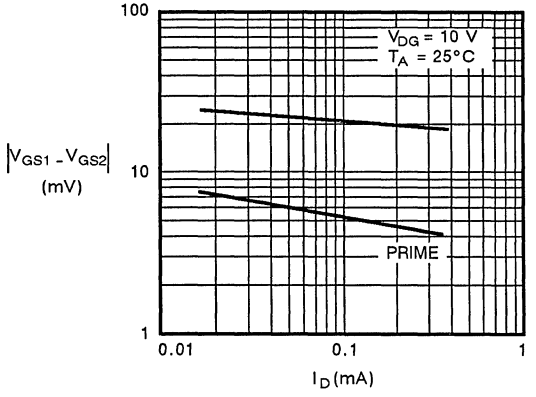
Output Characteristics ($V_{GS(OFF)}$ = -1.5 V)



Transfer Characteristics

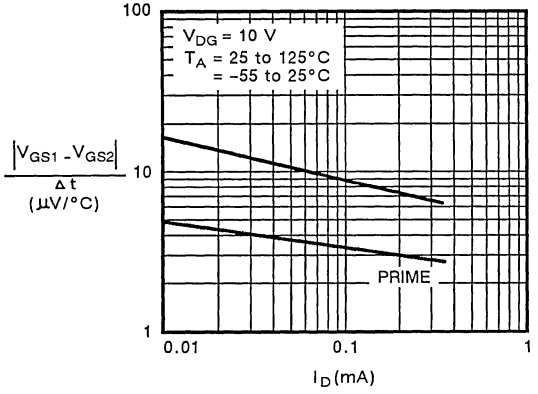


Gate-Source Differential Voltage vs. Drain Current

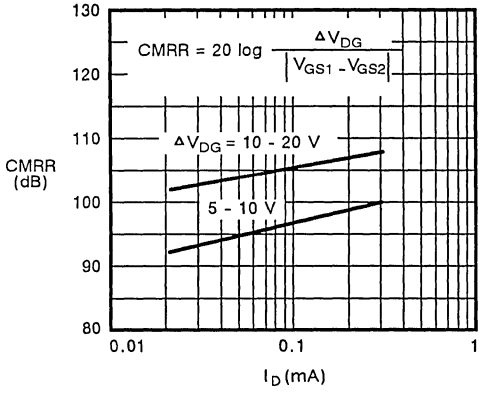


TYPICAL CHARACTERISTICS

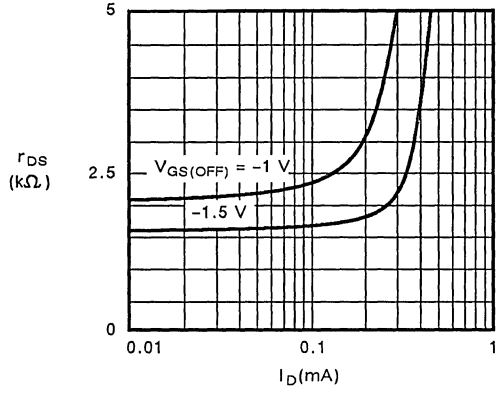
Voltage Differential with Temperature vs. Drain Current



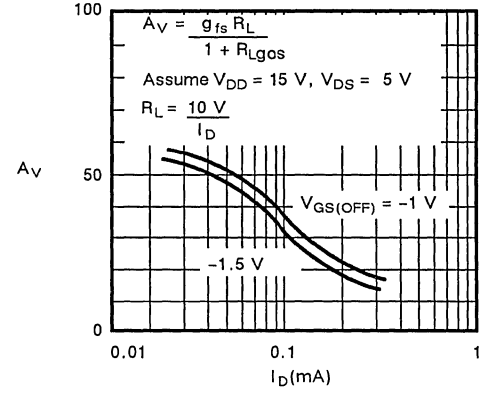
Common Mode Rejection Ratio vs. Drain Current



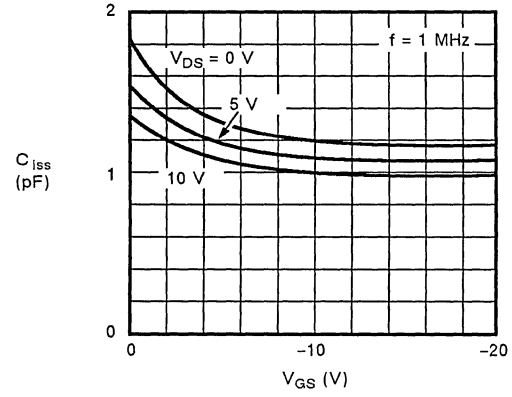
On-Resistance vs. Drain Current



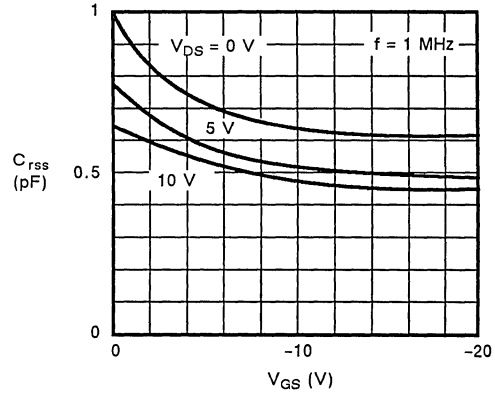
Circuit Voltage Gain vs. Drain Current



Common-Source Input Capacitance vs. Gate-Source Voltage



Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



7

Siliconix incorporated

N-Channel JFET

DESIGNED FOR:

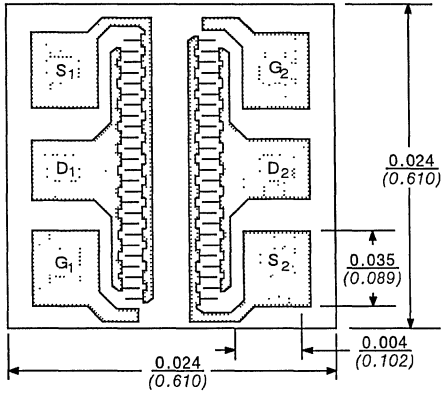
- High Frequency Amplifiers
- Mixers
- Oscillators
- Hybrid Op Amps

FEATURES

- High Gain
- Low Input Capacitance

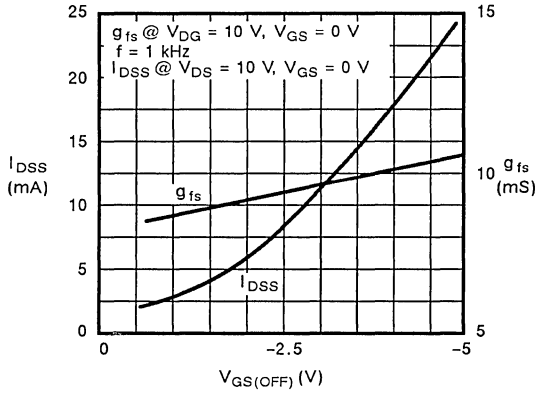
TYPE	PACKAGE	DEVICE
Dual	SOIC-8	• SST440, SST441 SST5912
	TO-71	• U440, U441
	TO-78	• 2N5911, 2N5912 U443, U444
	Chip	• Available as above specifications for 2N5912, U440, U441, U443, U444

GEOMETRY DIAGRAM

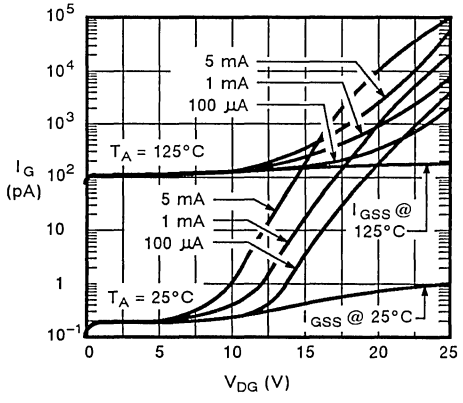


TYPICAL CHARACTERISTICS

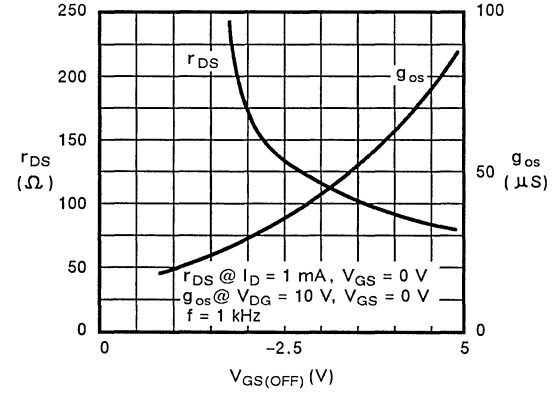
Drain Current & Transconductance vs. Gate-Source Cutoff Voltage



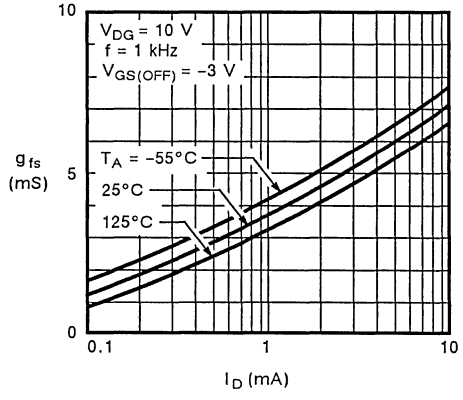
Operating Gate Current



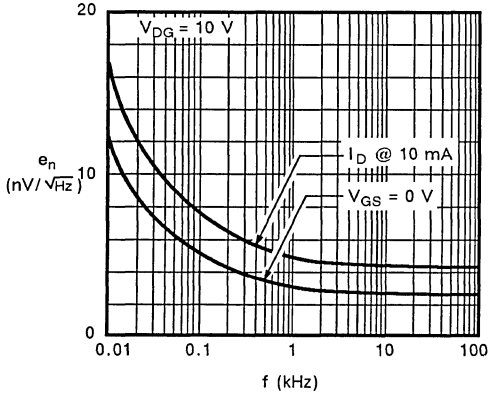
On-Resistance & Output Conductance vs. Gate-Source Cutoff Voltage



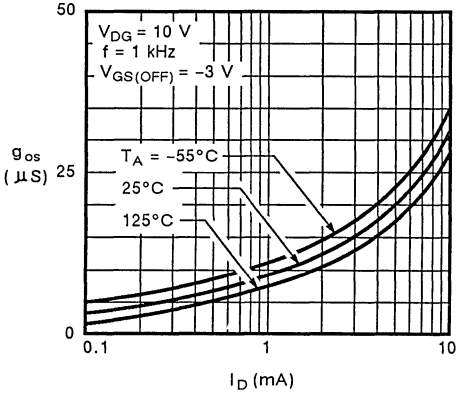
Common-Source Forward Transconductance vs. Drain Current



Equivalent Input Noise Voltage vs. Frequency



Output Conductance vs. Drain Current



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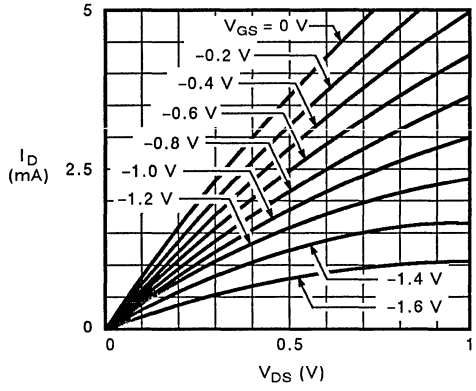
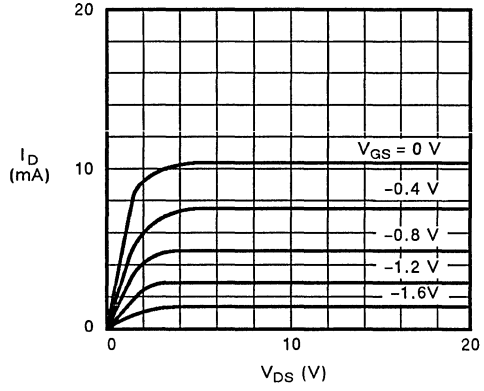
TYPICAL CHARACTERISTICS

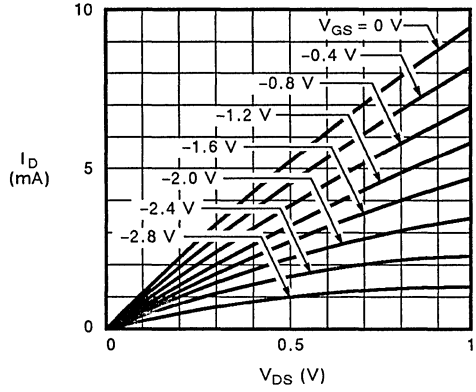
Output Characteristics ($V_{GS(OFF)}$ = -3 V)



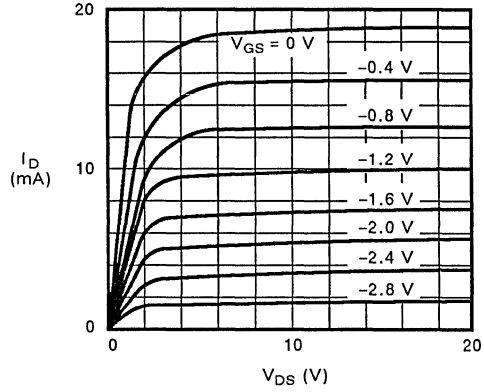
Output Characteristics ($V_{GS(OFF)}$ = -3 V)



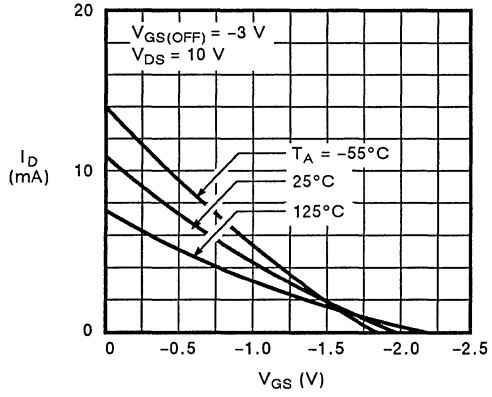
Output Characteristics ($V_{GS(OFF)}$ = -4 V)



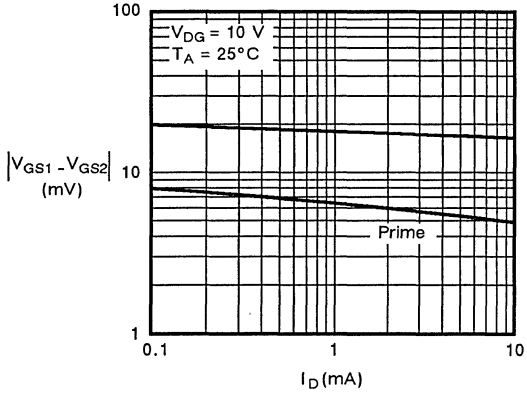
Output Characteristics ($V_{GS(OFF)}$ = -4 V)



Transfer Characteristics

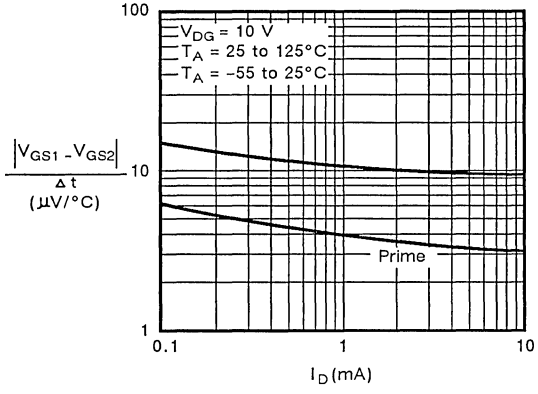


Gate-Source Differential Voltage vs. Drain Current

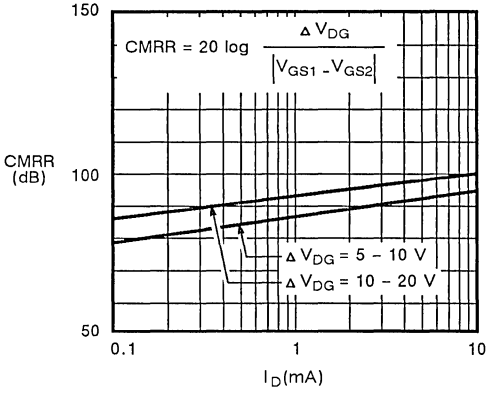


TYPICAL CHARACTERISTICS

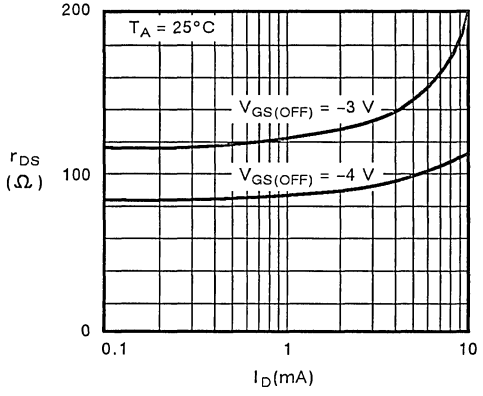
Voltage Differential with Temperature vs. Drain Current



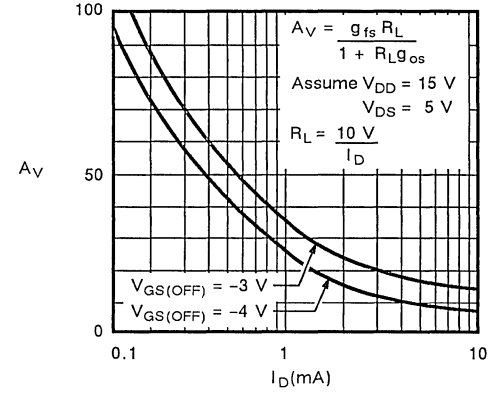
Common Mode Rejection Ratio vs. Drain Current



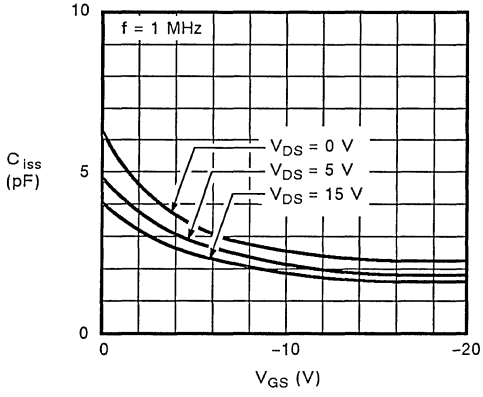
On-Resistance vs. Drain Current



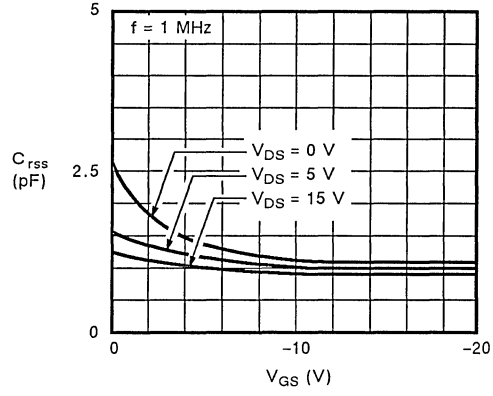
Circuit Voltage Gain vs. Drain Current



Common-Source Input Capacitance vs. Gate-Source Voltage



Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



7

Siliconix incorporated

N-Channel JFET

DESIGNED FOR:

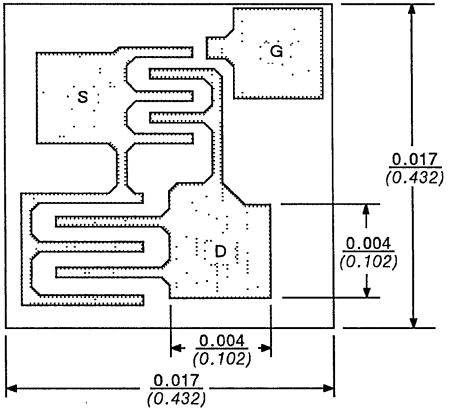
- Small Signal Amplifiers
- Voltage Controlled Resistors
- Choppers

FEATURES

- Low Noise NF < 1 dB at 1 KHz
- Operation from Low Power Supply Voltages
  $V_{GS(off)}$ < 1 V (2N4338)
- High Off-Isolation as a Switch
  $I_{D(OFF)}$ < 50 pA
- High Input Impedance

TYPE	PACKAGE	DEVICE
Single	TO-92	• J201, J202, J203, J204 PN4302, PN4303, PN4304
	SOT-23	• SST201, SST202, SST203, SST204
	TO-18	• 2N4338, 2N4339, 2N4340, 2N4341 VCR4N
	TO-72	• 2N4867, 2N4868, 2N4869, 2N4867A, 2N4868A, 2N4869A
	Chip	• Available as above specifications

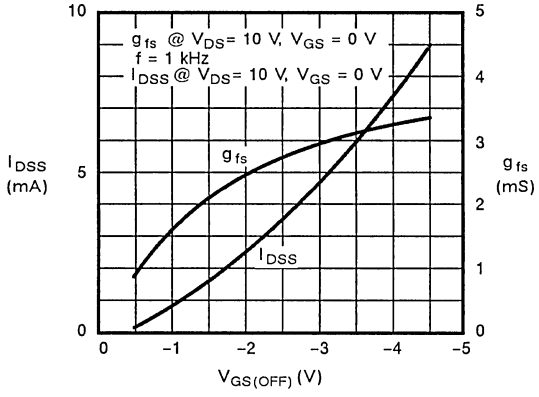
GEOMETRY DIAGRAM



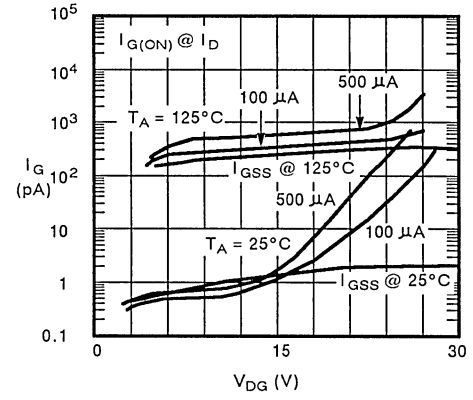
Gate also backside contact

TYPICAL CHARACTERISTICS

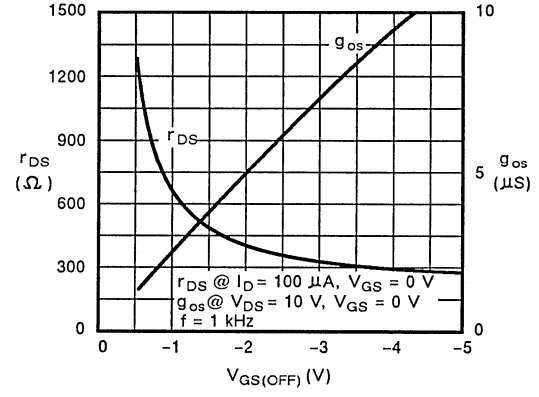
Drain Current & Transconductance vs. Gate-Source Cutoff Voltage



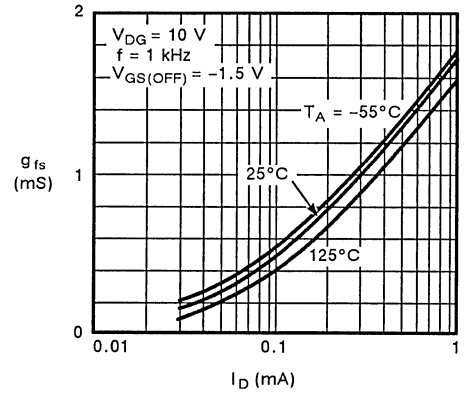
Operating Gate Current



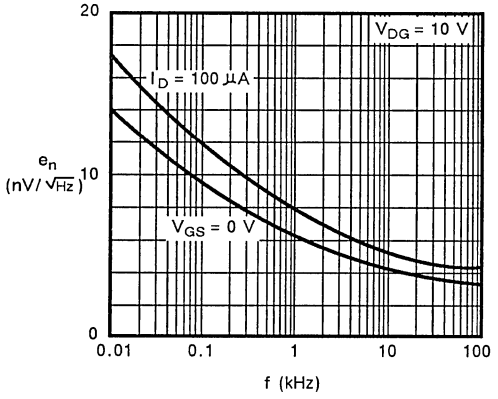
On-Resistance & Output Conductance vs. Gate-Source Cutoff Voltage



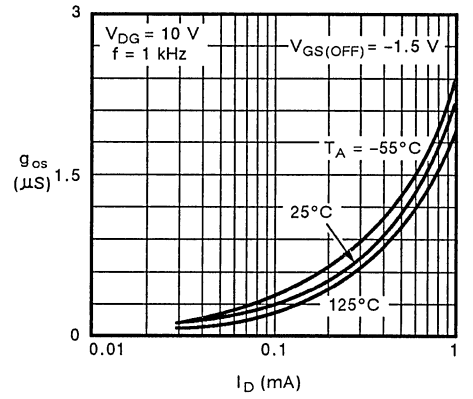
Common-Source Forward Transconductance vs. Drain Current



Equivalent Input Noise Voltage vs. Frequency



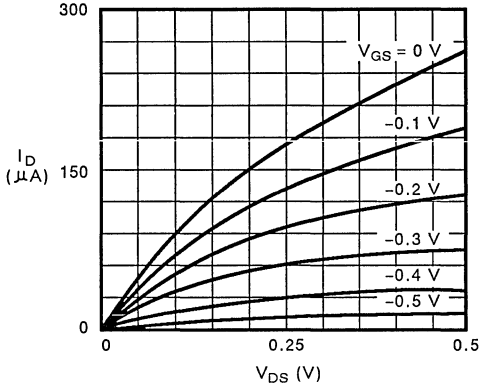
Output Conductance vs. Drain Current



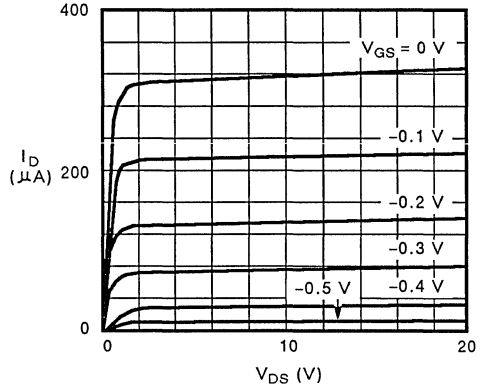
7

TYPICAL CHARACTERISTICS

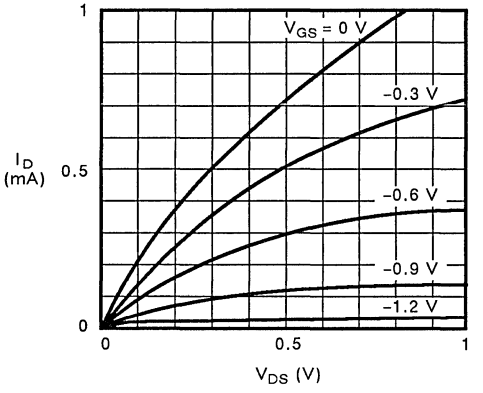
Output Characteristics ($V_{GS(OFF)}$ = -0.7 V)



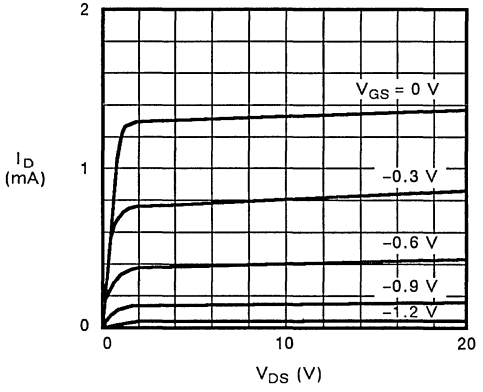
Output Characteristics ($V_{GS(OFF)}$ = -0.7 V)



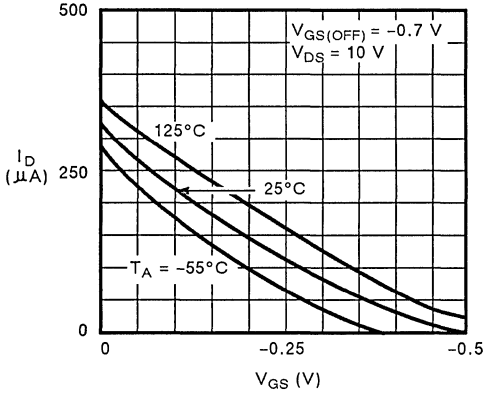
Output Characteristics ($V_{GS(OFF)}$ = -1.5 V)



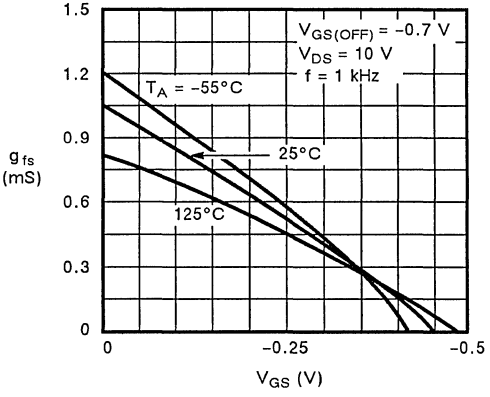
Output Characteristics ($V_{GS(OFF)}$ = -1.5 V)



Transfer Characteristics

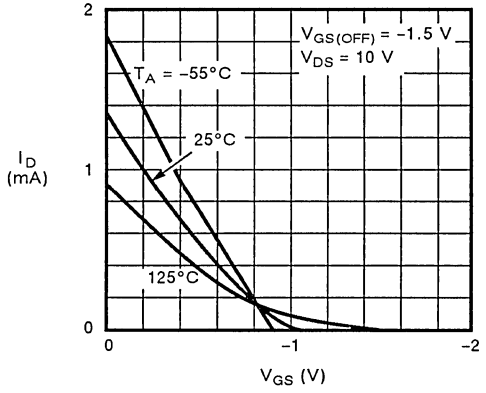


Transconductance vs. Gate-Source Voltage

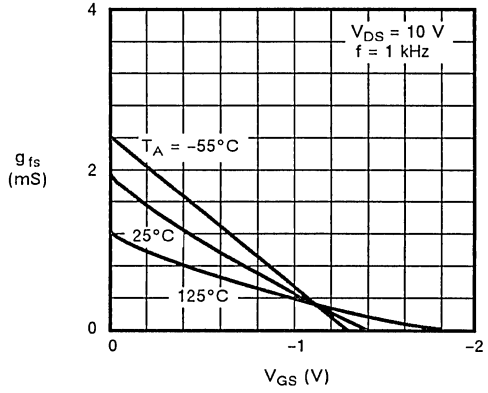


TYPICAL CHARACTERISTICS

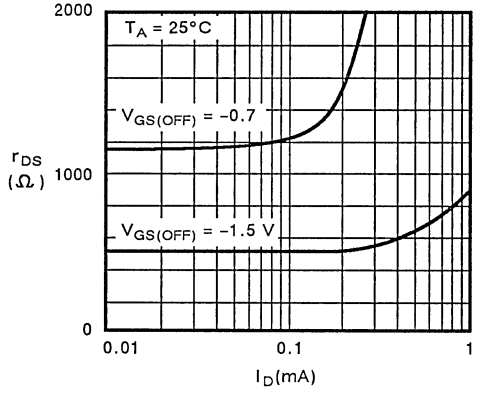
Transfer Characteristics



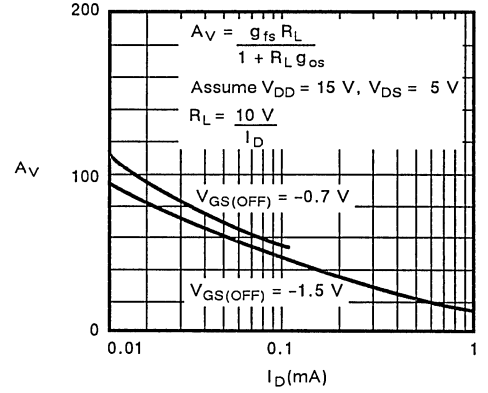
Transconductance vs. Gate-Source Voltage



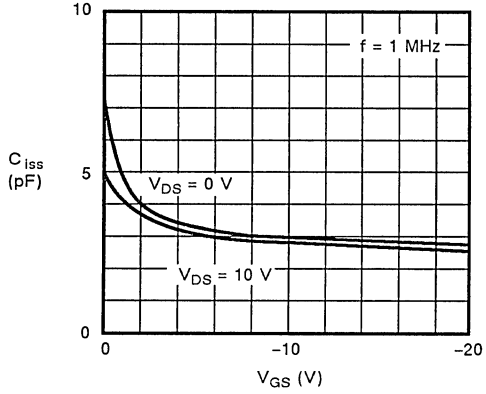
On-Resistance vs. Drain Current



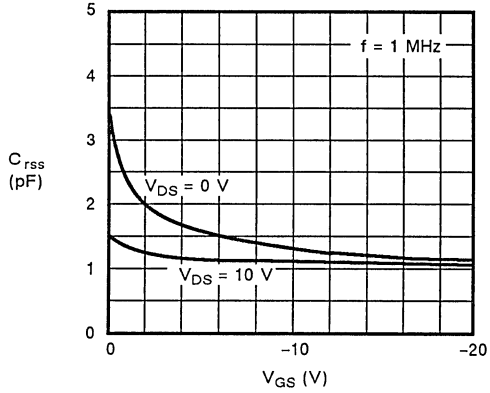
Circuit Voltage Gain vs. Drain Current



Common-Source Input Capacitance vs. Gate-Source Voltage



Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



7

N-Channel JFET

DESIGNED FOR:

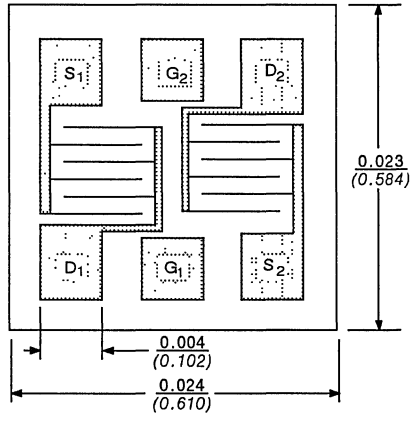
- General Purpose Amplifiers

FEATURES

- High Input Impedance

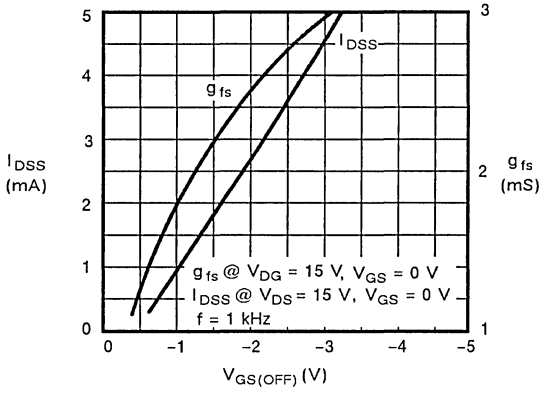
TYPE	PACKAGE	DEVICE
Dual	TO-71	• 2N3956, 2N3957, 2N3958 2N5196, 2N5197, 2N5198, 2N5199
	Chip	• Available as above specifications for 2N3956 through 2N3958, 2N5198 & 2N5199

GEOMETRY DIAGRAM

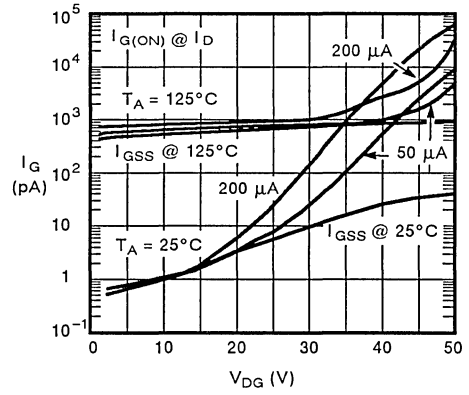


TYPICAL CHARACTERISTICS

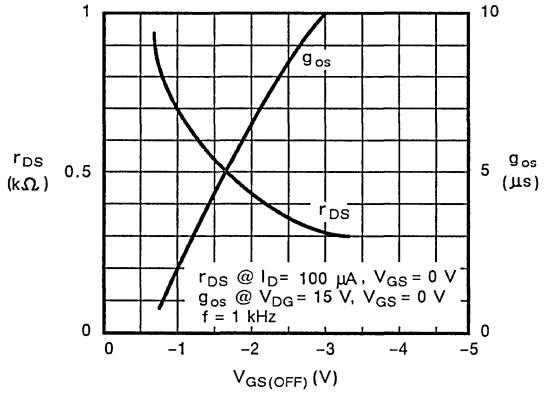
Drain Current & Transconductance vs. Gate-Source Cutoff Voltage



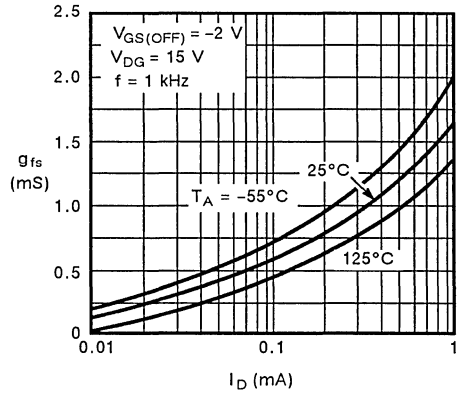
Operating Gate Current



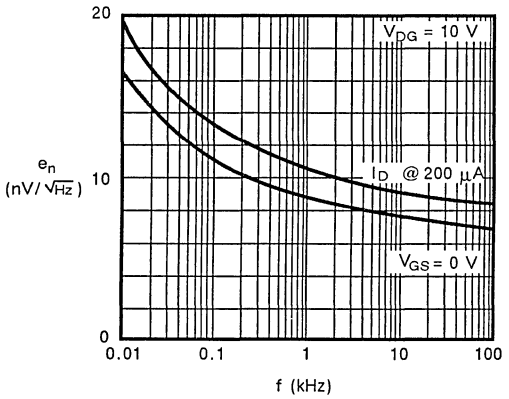
On-Resistance & Output Conductance vs. Gate-Source Cutoff Voltage



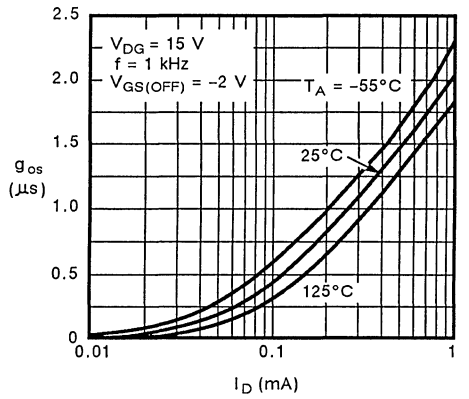
Common-Source Forward Transconductance vs. Drain Current



Equivalent Input Noise Voltage vs. Frequency



Output Conductance vs. Drain Current



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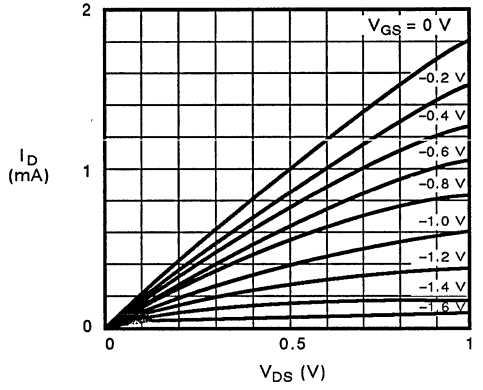
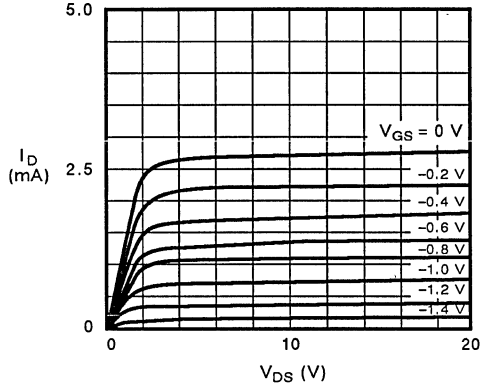
TYPICAL CHARACTERISTICS

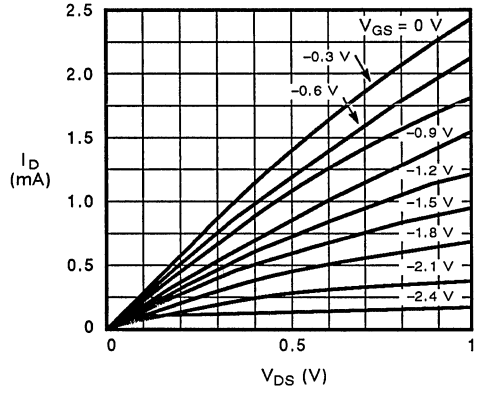
Output Characteristics ($V_{GS(OFF)}$ = −2 V)



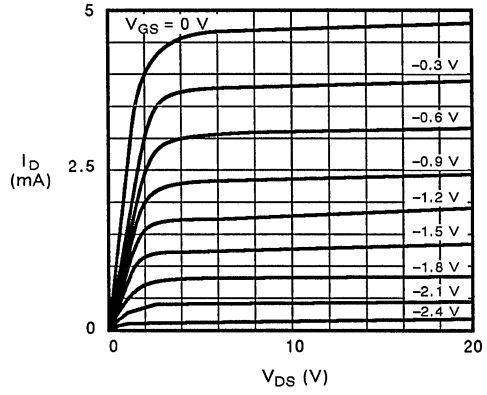
Output Characteristics ($V_{GS(OFF)}$ = −2 V)



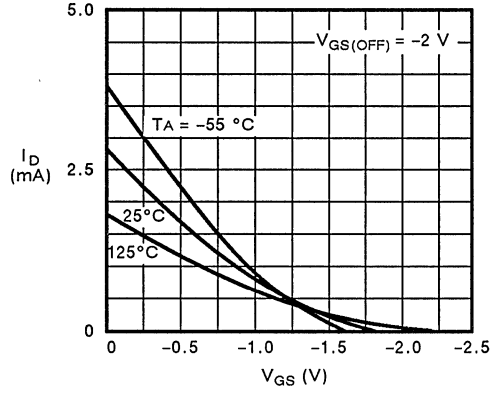
Output Characteristics ($V_{GS(OFF)}$ = −3 V)



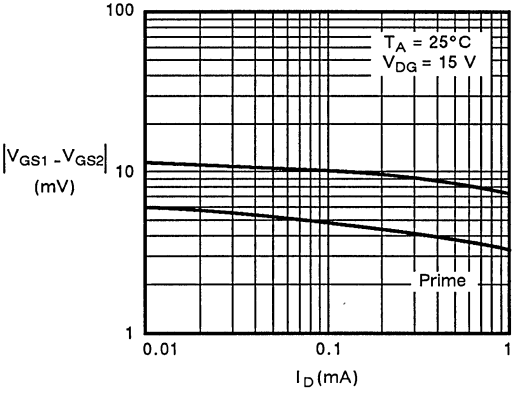
Output Characteristics ($V_{GS(OFF)}$ = −3 V)



Transfer Characteristics

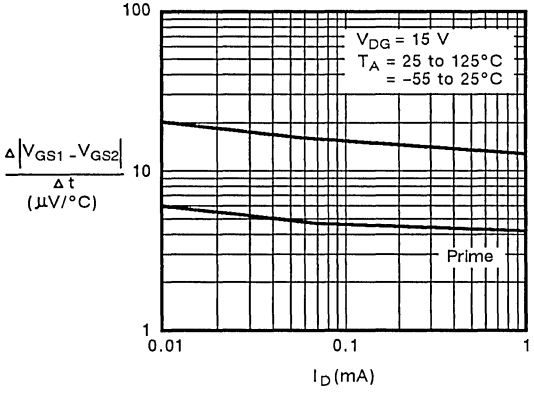


Gate-Source Differential Voltage vs. Drain Current

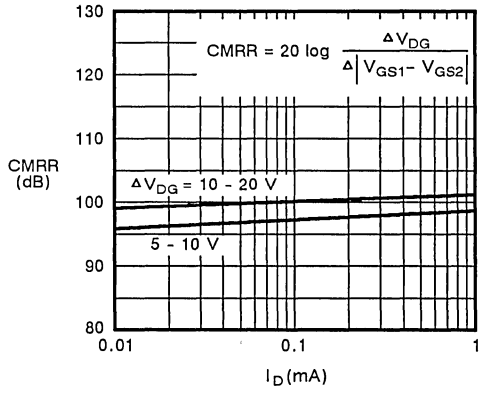


TYPICAL CHARACTERISTICS

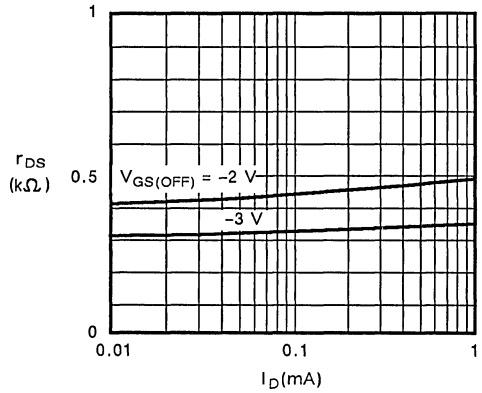
Voltage Differential with Temperature vs. Drain Current



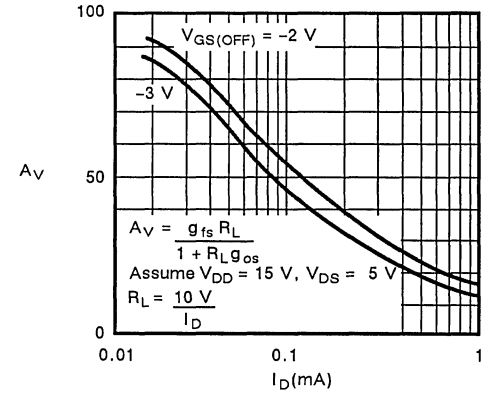
Common Mode Rejection Ratio vs. Drain Current



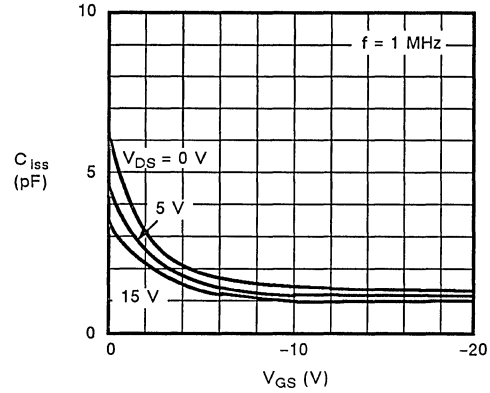
On-Resistance vs. Drain Current



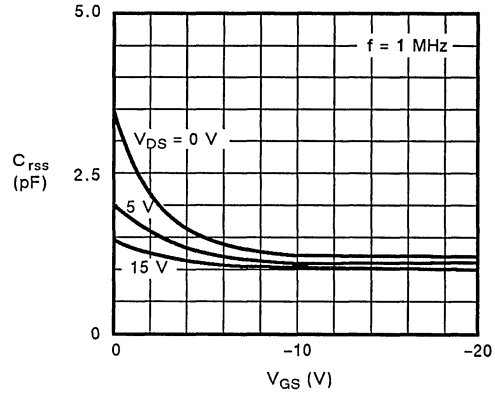
Circuit Voltage Gain vs. Drain Current



Common-Source Input Capacitance vs. Gate-Source Voltage



Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



7

Siliconix incorporated

N-Channel JFET

DESIGNED FOR:

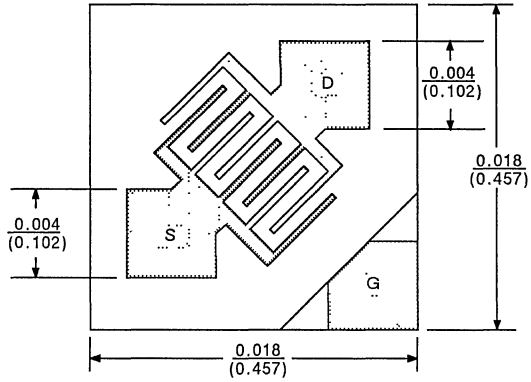
- Small Signal Amplifiers
- VHF Amplifiers
- Oscillators
- Mixers
- Switches

FEATURES

- Wide Input Dynamic Range
  High I_G Breakpoint voltage
- High Gain
- Low Insertion Loss Switches

TYPE	PACKAGE	DEVICE
Single	TO-72	• 2N4220, 2N4221, 2N4222 2N4220A, 2N4221A, 2N4222A
	Chip	• Available as above specification

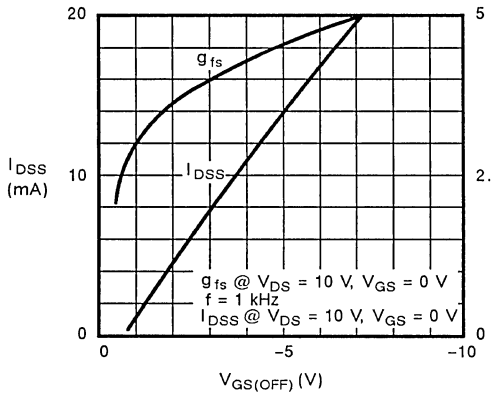
GEOMETRY DIAGRAM



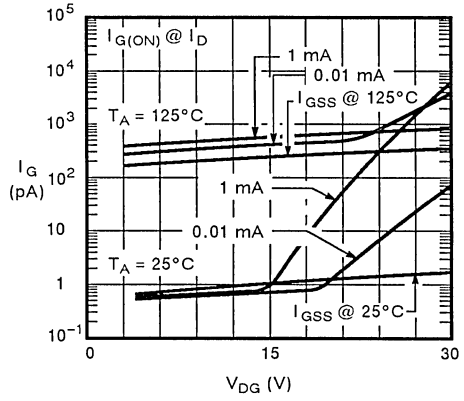
Gate also backside contact

TYPICAL CHARACTERISTICS

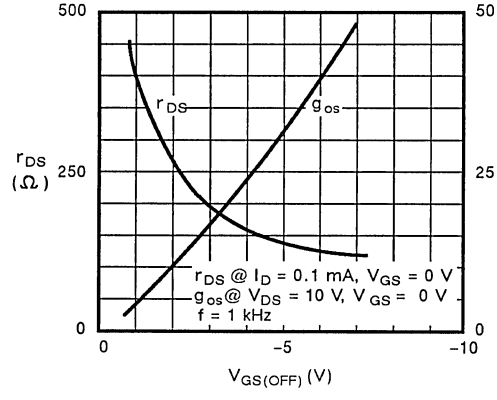
Drain Current & Transconductance vs. Gate-Source Cutoff Voltage



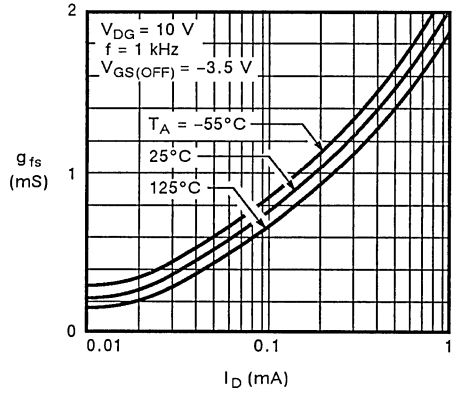
Operating Gate Current



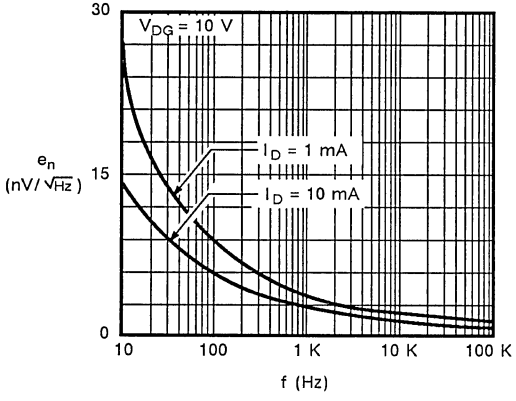
On-Resistance & Output Conductance vs. Gate-Source Cutoff Voltage



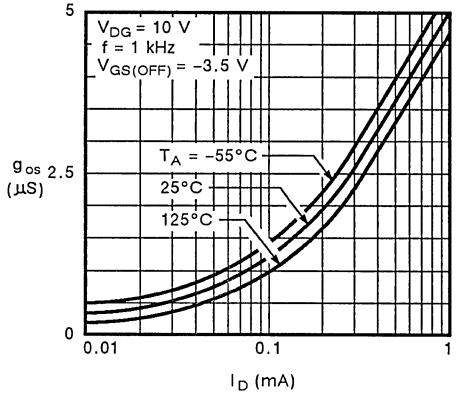
Common-Source Forward Transconductance vs. Drain Current



Equivalent Input Noise Voltage vs. Frequency



Output Conductance vs. Drain Current



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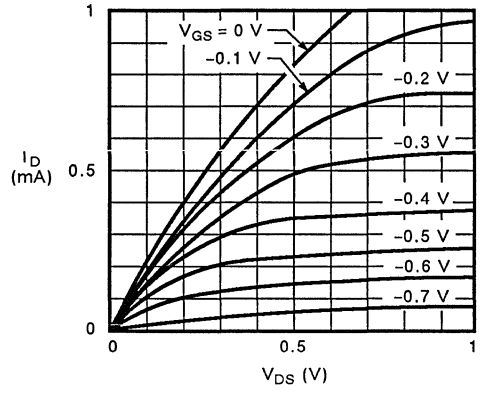
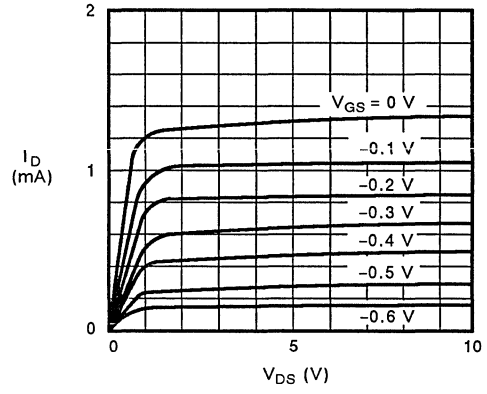
TYPICAL CHARACTERISTICS

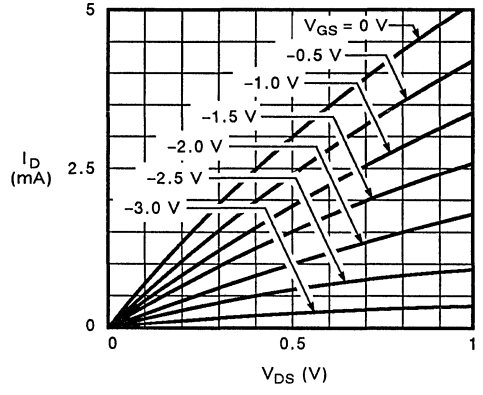
Output Characteristics ($V_{GS(OFF)}$ = -1 V)



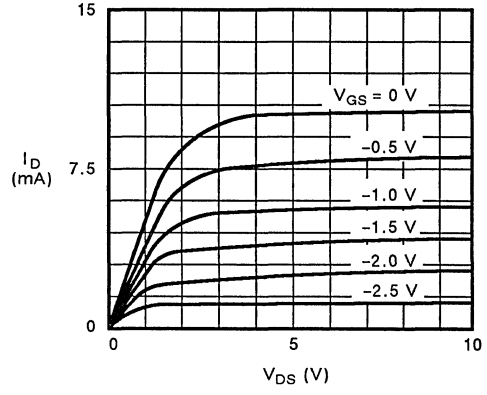
Output Characteristics ($V_{GS(OFF)}$ = -1 V)



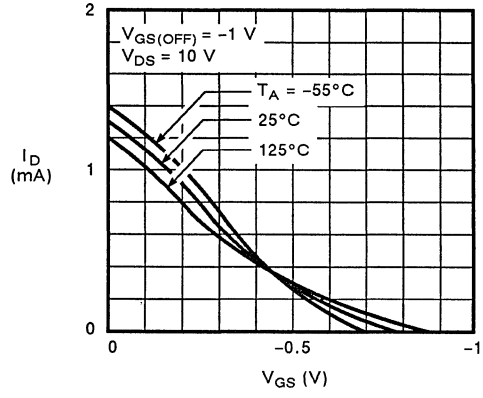
Output Characteristics ($V_{GS(OFF)}$ = -3.5 V)



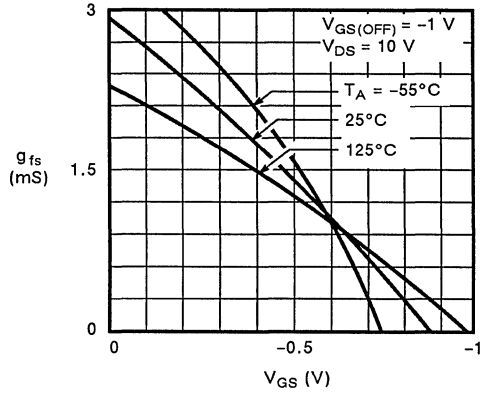
Output Characteristics ($V_{GS(OFF)}$ = -3.5 V)



Transfer Characteristics

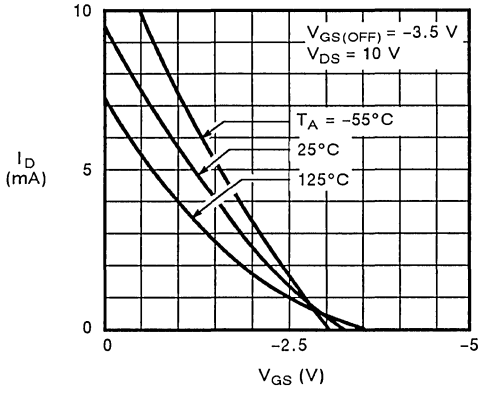


Transconductance vs. Gate-Source Voltage

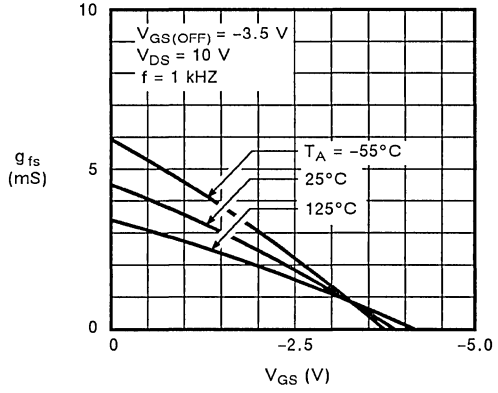


TYPICAL CHARACTERISTICS

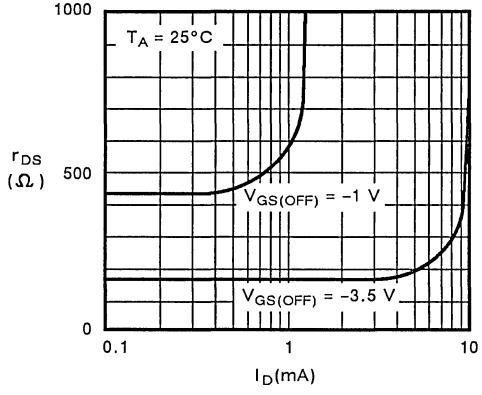
Transfer Characteristics



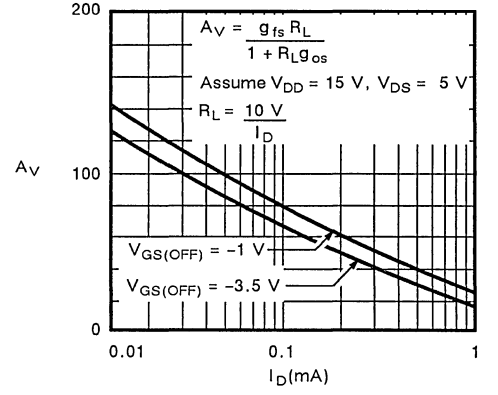
Transconductance vs. Gate-Source Voltage



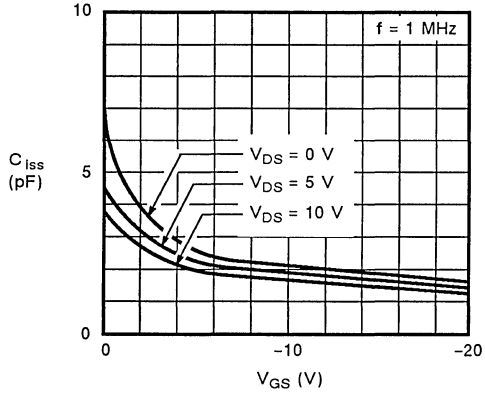
On-Resistance vs. Drain Current



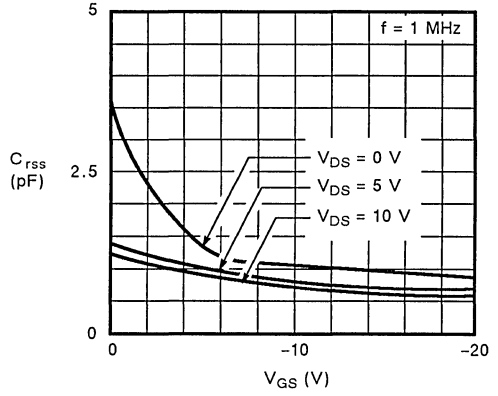
Circuit Voltage Gain vs. Drain Current



Common-Source Input Capacitance vs. Gate-Source Voltage



Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



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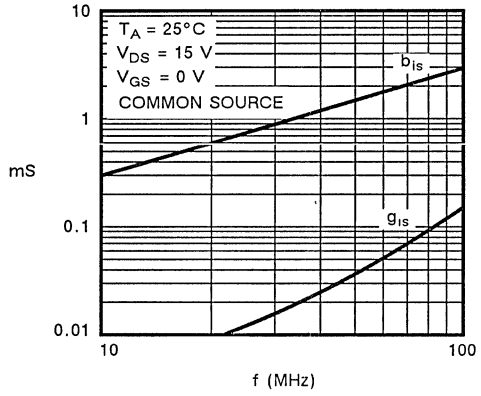
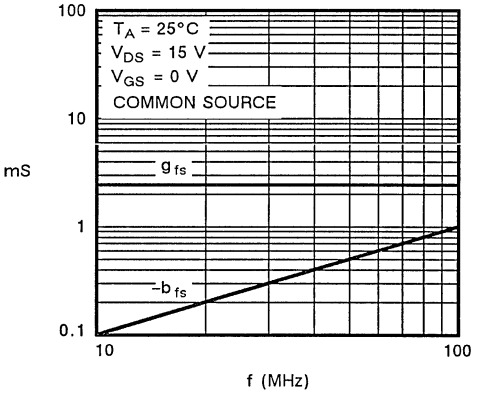
TYPICAL CHARACTERISTICS

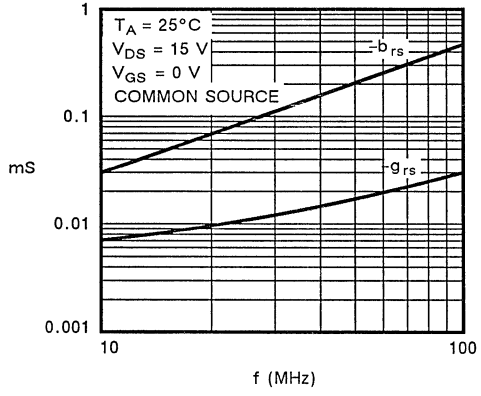
Input Admittance



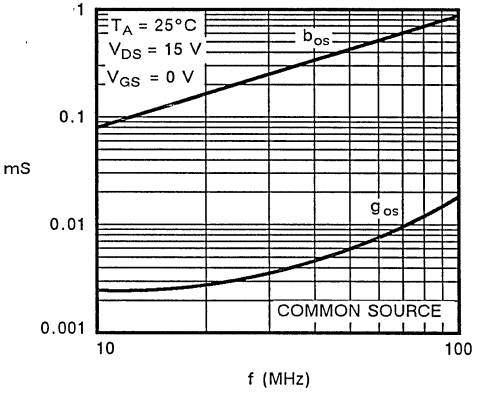
Forward Admittance



Reverse Admittance



Output Admittance



N-Channel JFET

DESIGNED FOR:

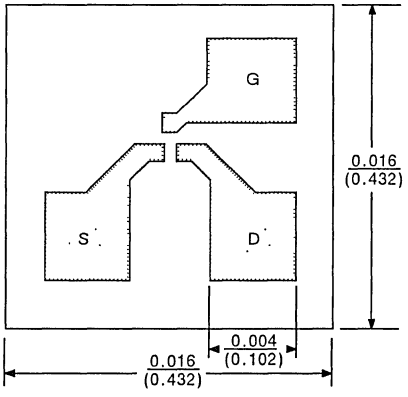
- Ultra-High Input Impedance Amplifier
  Electrometers:
  Infrared Detectors
  Smoke Detectors
  pH Meters

FEATURES

- Low Power
  I_{DSS} < 90 μA (2N4117)
- High Input Impedance
  I_G < 1 pA (2N4117A)

TYPE	PACKAGE	DEVICE
Single	TO-92	• PN4117, PN4118, PN4119 PN4117A, PN4118A, PN4119A
	TO-72	• 2N4117, 2N4118, 2N4119 2N4117A, 2N4118A, 2N4119A
	Chip	• Available as above specification

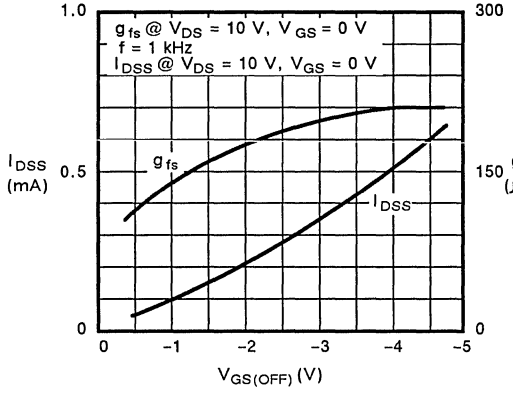
GEOMETRY DIAGRAM



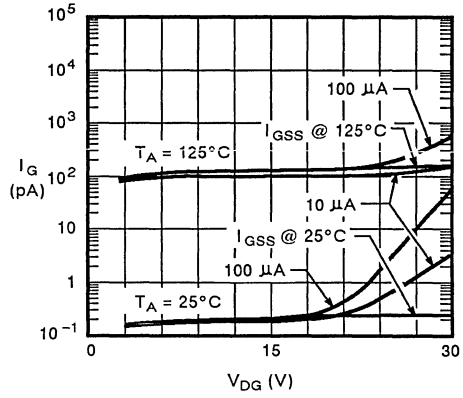
Gate also backside contact

TYPICAL CHARACTERISTICS

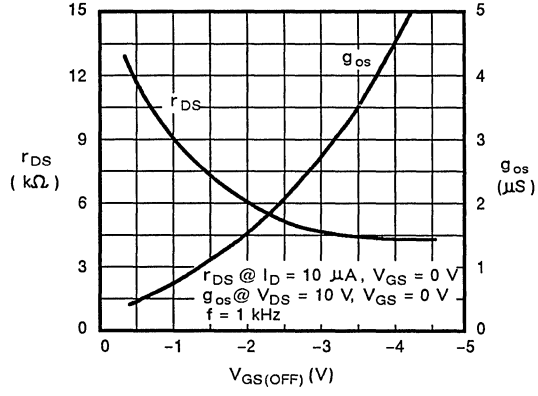
Drain Current & Transconductance vs. Gate-Source Cutoff Voltage



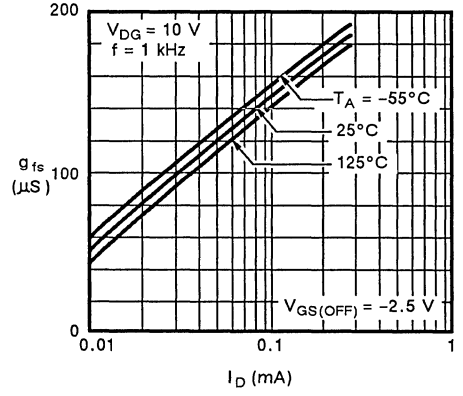
Operating Gate Current



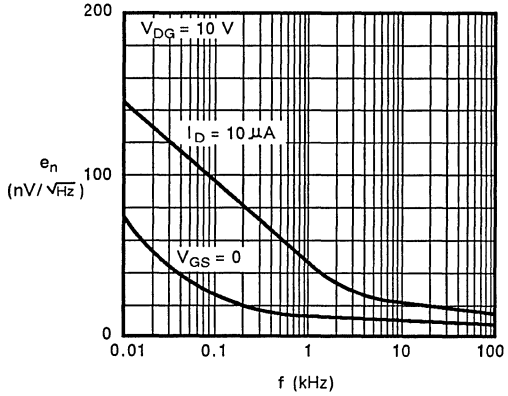
On-Resistance & Output Conductance vs. Gate-Source Cutoff Voltage



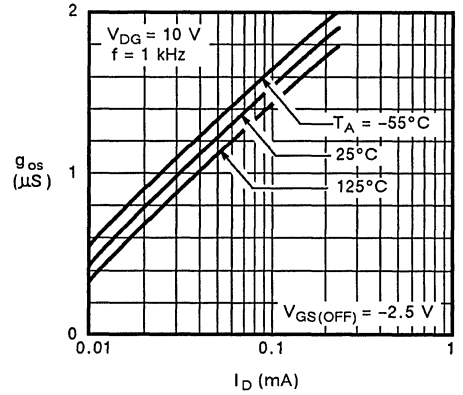
Common-Source Forward Transconductance vs. Drain Current



Equivalent Input Noise Voltage vs. Frequency

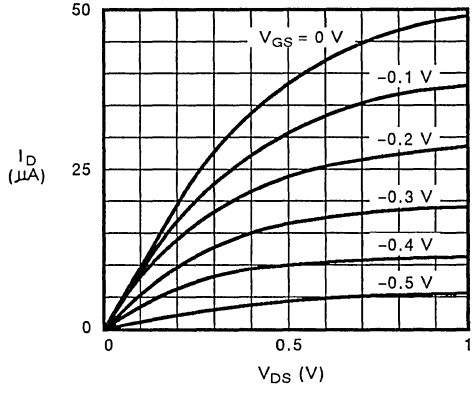


Output Conductance vs. Drain Current

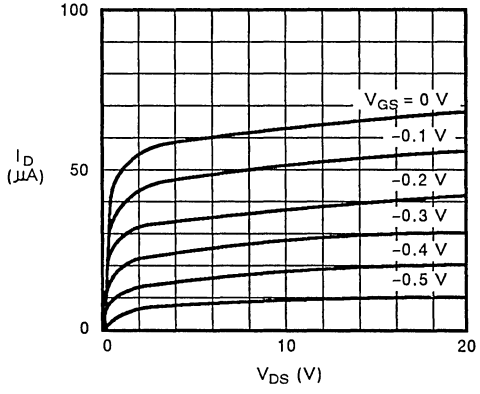


TYPICAL CHARACTERISTICS

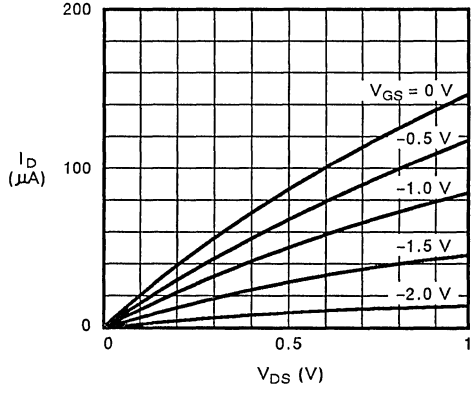
Output Characteristics ($V_{GS(OFF)}$ = -0.7 V)



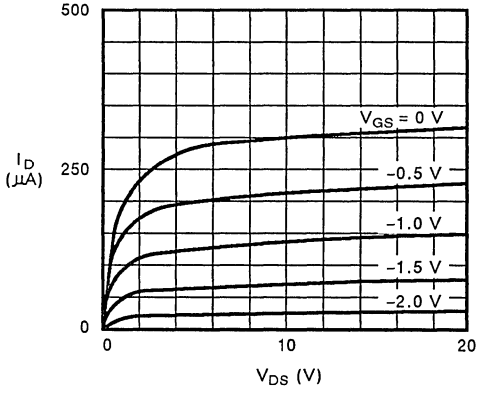
Output Characteristics ($V_{GS(OFF)}$ = -0.7 V)



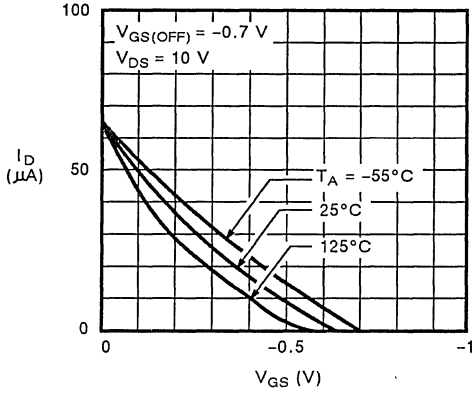
Output Characteristics ($V_{GS(OFF)}$ = -2.5 V)



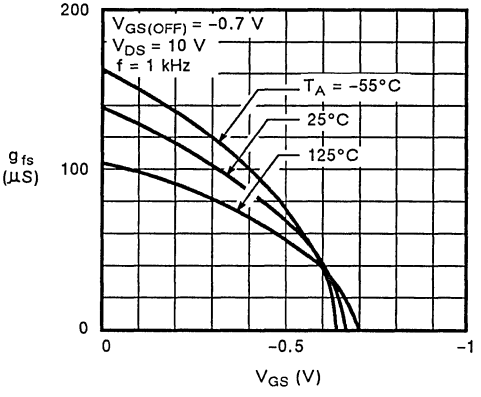
Output Characteristics ($V_{GS(OFF)}$ = -2.5 V)



Transfer Characteristics



Transconductance vs. Gate-Source Voltage



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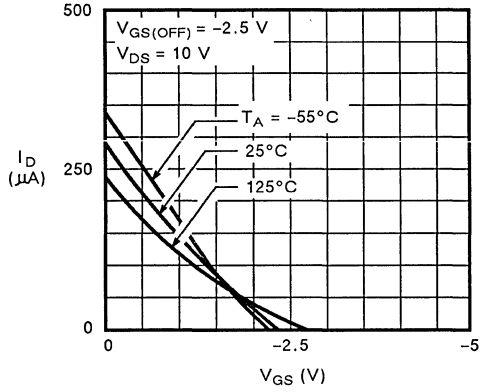
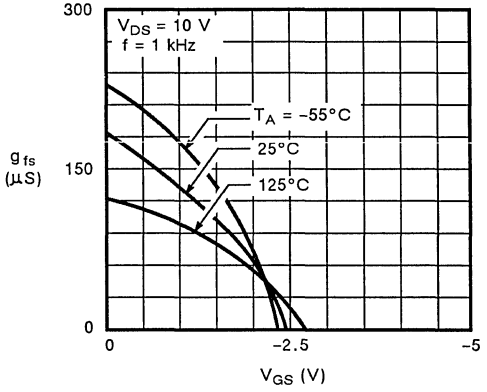
TYPICAL CHARACTERISTICS

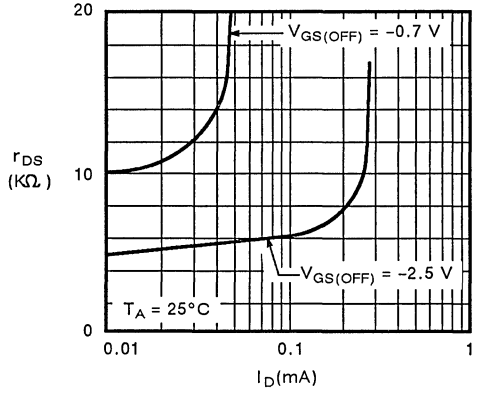
Transfer Characteristics



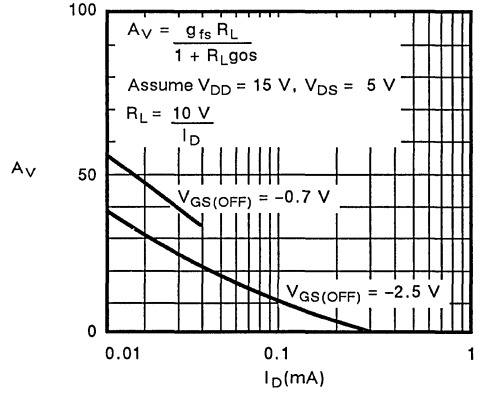
Transconductance vs. Gate-Source Voltage



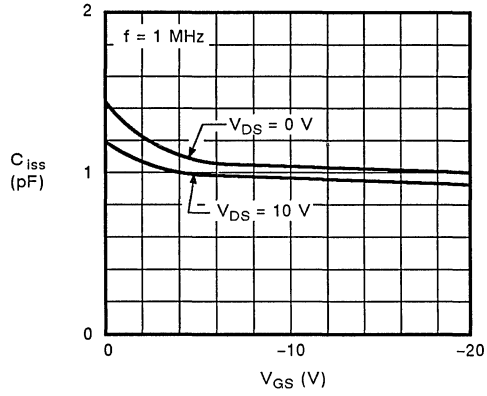
On-Resistance vs. Drain Current



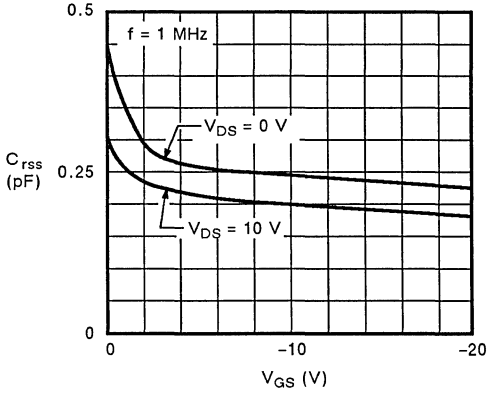
Circuit Voltage Gain vs. Drain Current



Common-Source Input Capacitance vs. Gate-Source Voltage



Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



N-Channel JFET

DESIGNED FOR:

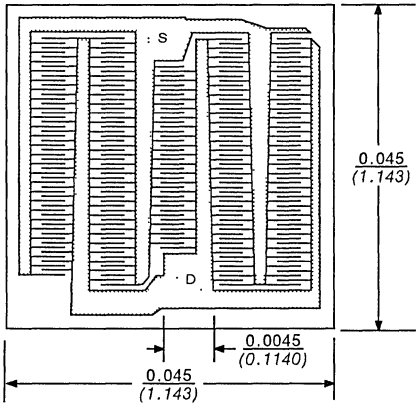
- Analog Swiches
- Commutators
- Choppers

FEATURES

- Very Low Insertion Loss
  $r_{DS(on)} < 3.0\ \Omega$ (U290)
- High Off-Isolation

TYPE	PACKAGE	DEVICE
Single	TO-92	• J105, J106, J107
	TO-52	• U290, U291
	Chip	• Available as above specifications

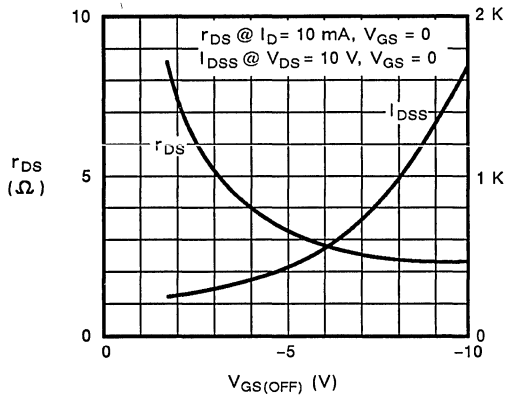
GEOMETRY DIAGRAM



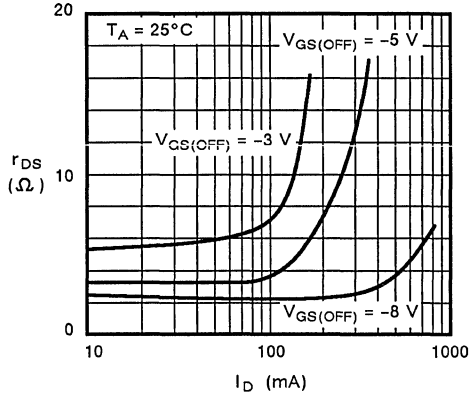
Gate is backside contact

TYPICAL CHARACTERISTICS

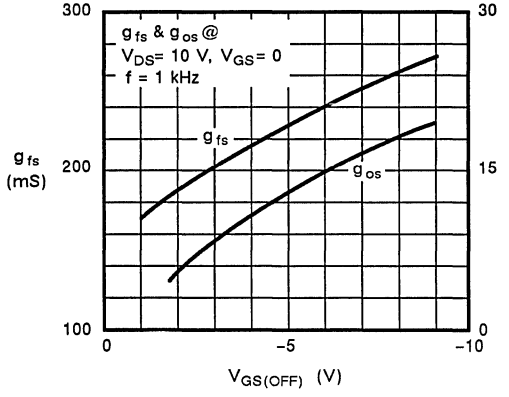
On-Resistance & Drain Current vs. Gate-Source Cutoff Voltage



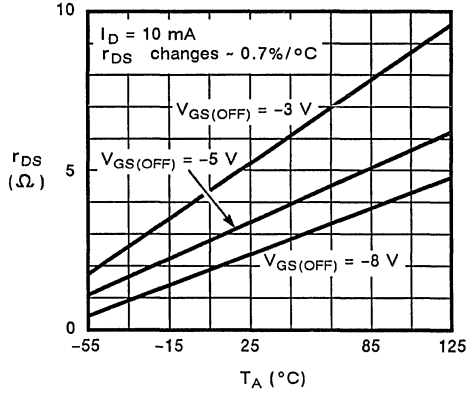
On-Resistance vs. Drain Current



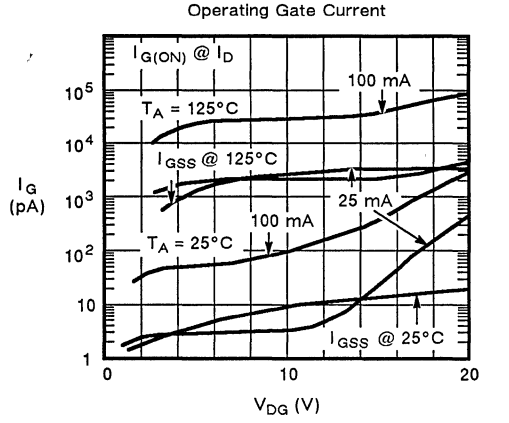
Forward Transconductance & Output Conductance vs. Gate-Source Cutoff Voltage



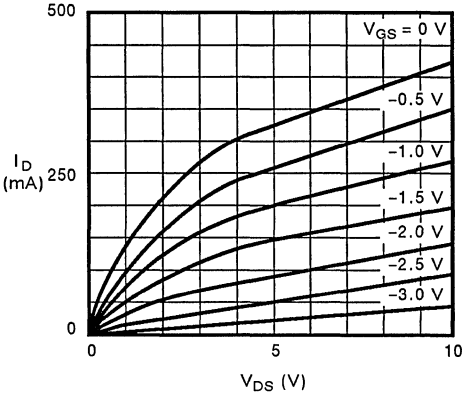
On-Resistance vs. Temperature



Operating Gate Current

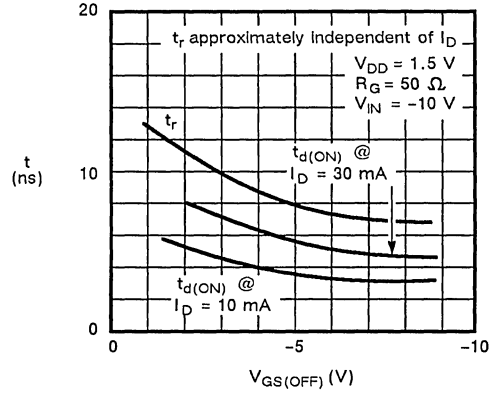


Output Characteristics ($V_{GS(OFF)}$ = -5 V)

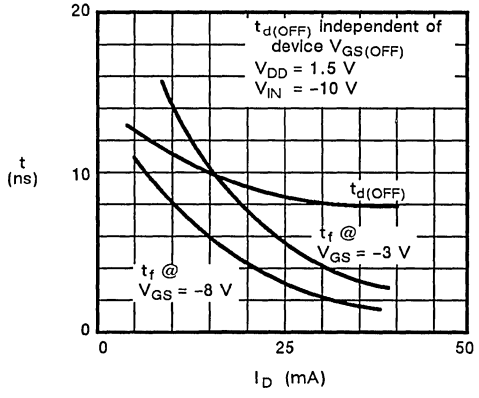


TYPICAL CHARACTERISTICS

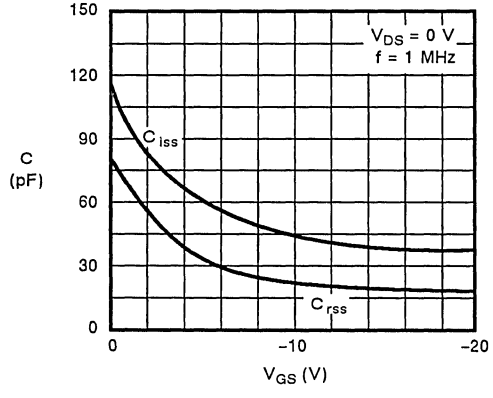
Turn-On Switching



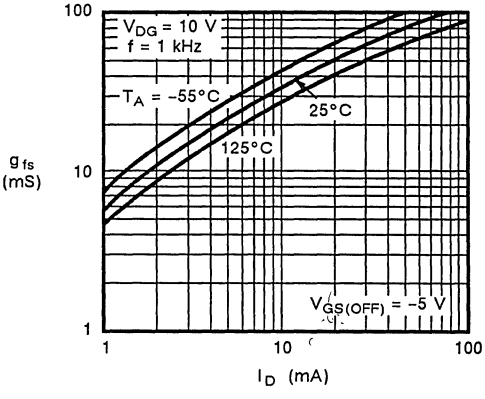
Turn-Off Switching



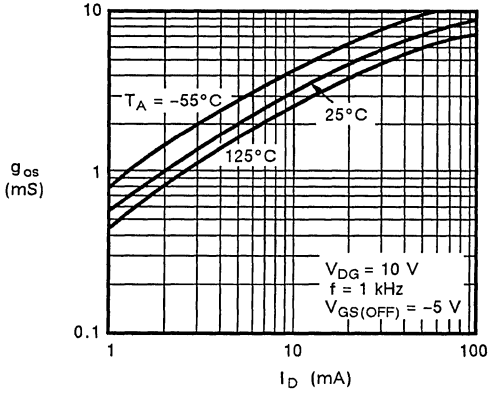
Capacitance vs. Gate-Source Voltage



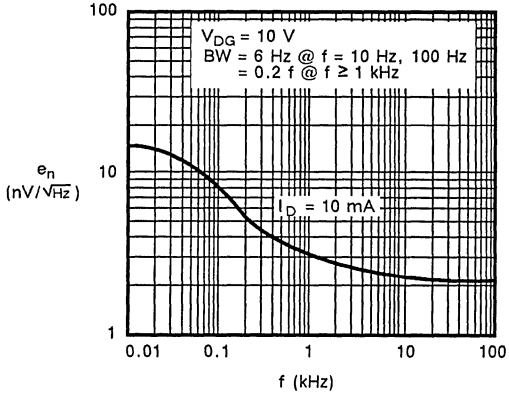
Transconductance vs. Drain Current



Output Conductance vs. Drain Current



Noise Voltage vs. Frequency



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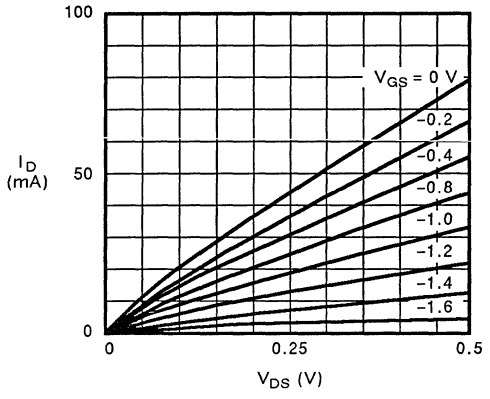
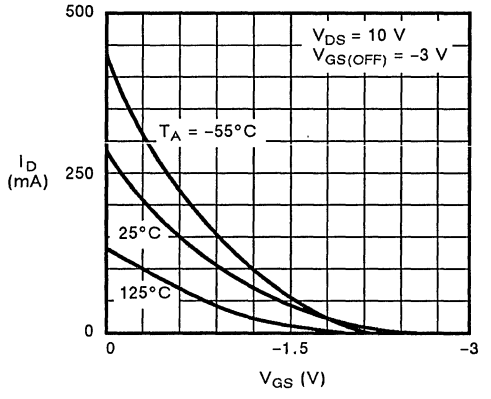
TYPICAL CHARACTERISTICS

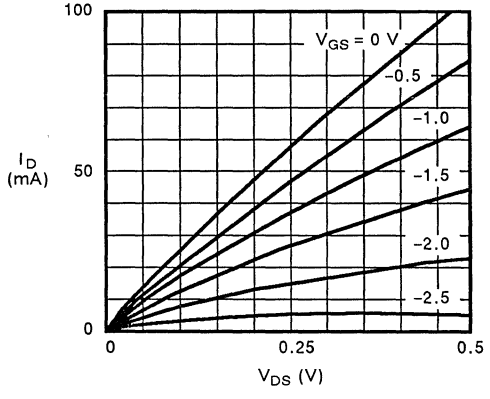
Output Characteristics ($V_{GS(OFF)}$ = -3 V)



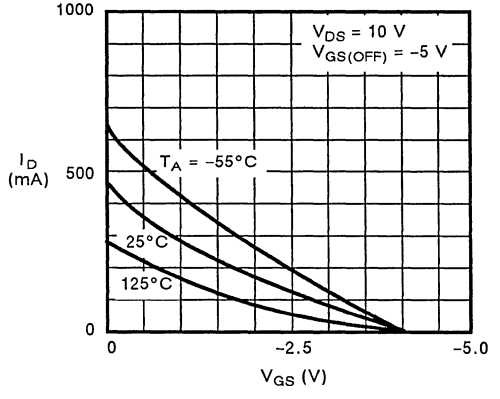
Transfer Characteristics



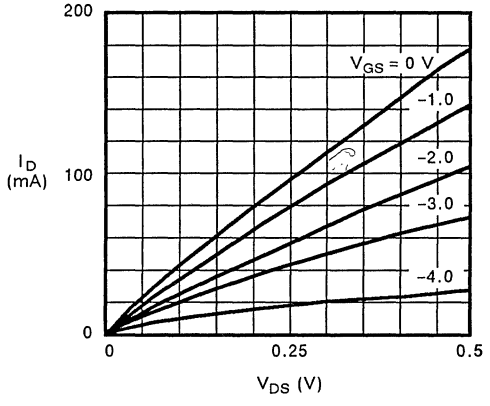
Output Characteristics ($V_{GS(OFF)}$ = -5 V)



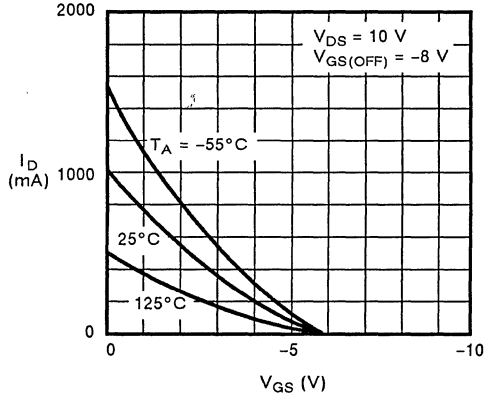
Transfer Characteristics



Output Characteristics ($V_{GS(OFF)}$ = -8 V)



Transfer Characteristics



N-Channel JFET

DESIGNED FOR:

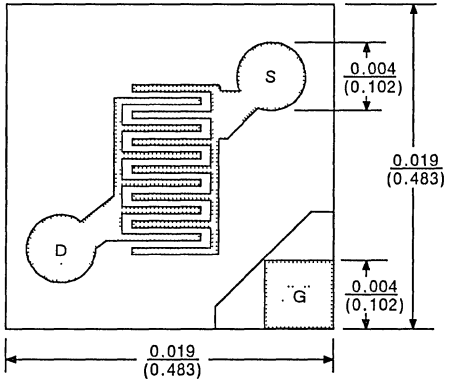
- VHF/UHF Amplifers
- Front End High Sensitivity Amplifiers
- Oscillators
- Mixers

FEATURES

- 16 dB at 100 MHz, Common Gate
- 11 dB at 450 MHz, Common Gate

TYPE	PACKAGE	DEVICE
Single	TO-92	• J308, J309, J310
	SOT-23	• SST308, SST309, SST310
	TO-52	• U308, U309, U310
Dual	TO-78	• U430, U431
	Chip	• Available as above specifications

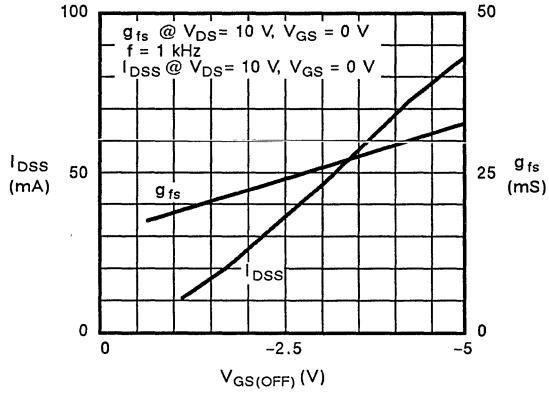
GEOMETRY DIAGRAM



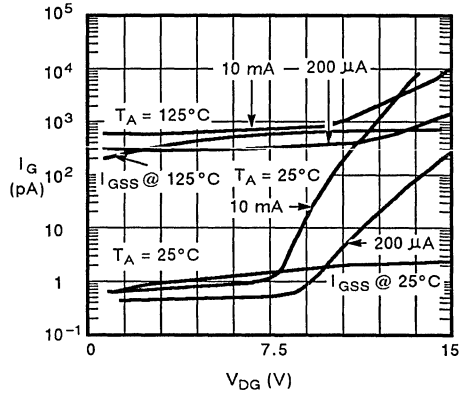
Gate also backside contact

TYPICAL CHARACTERISTICS

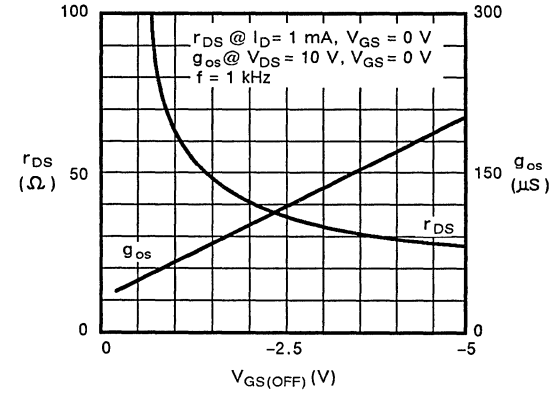
Drain Current & Transconductance vs. Gate-Source Cutoff Voltage



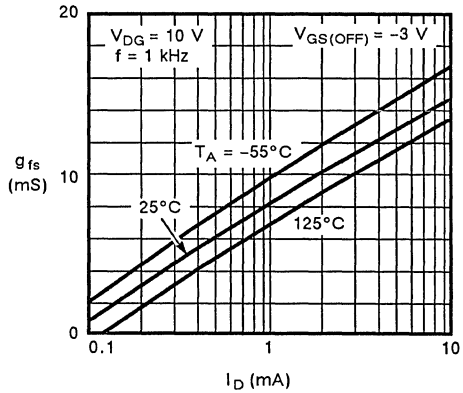
Operating Gate Current



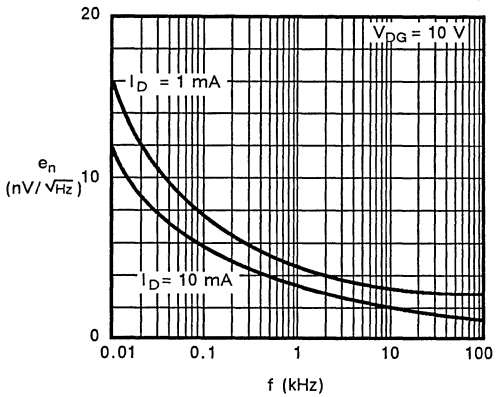
On-Resistance & Output Conductance vs. Gate-Source Cutoff Voltage



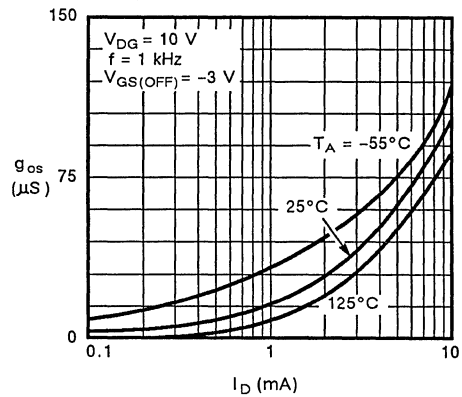
Common-Source Forward Transconductance vs. Drain Current



Equivalent Input Noise Voltage vs. Frequency

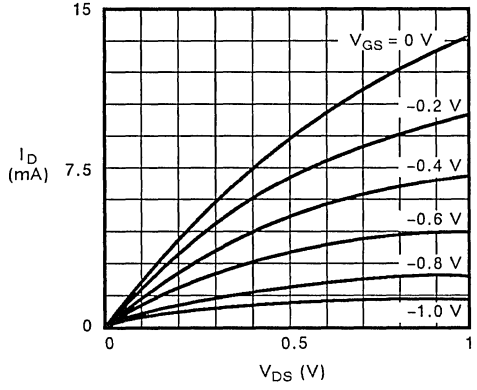


Output Conductance vs. Drain Current

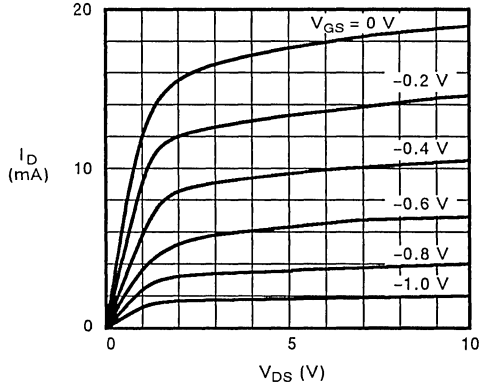


TYPICAL CHARACTERISTICS

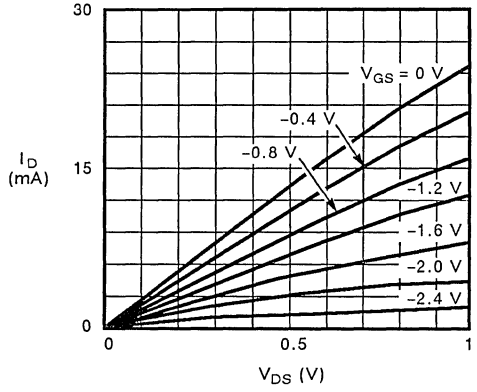
Output Characteristics ($V_{GS(OFF)}$ = -1.5 V)



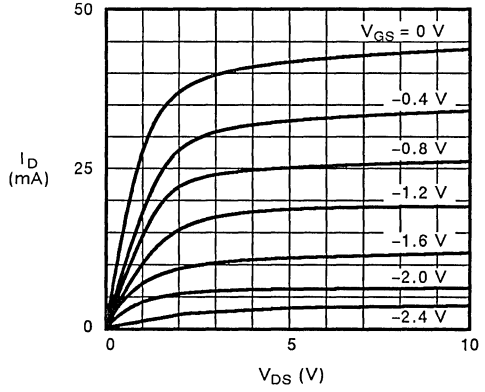
Output Characteristics ($V_{GS(OFF)}$ = -1.5 V)



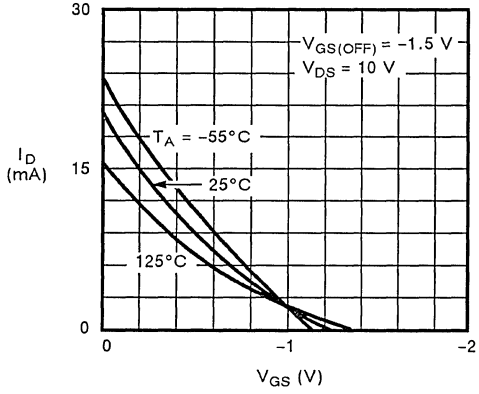
Output Characteristics ($V_{GS(OFF)}$ = -3 V)



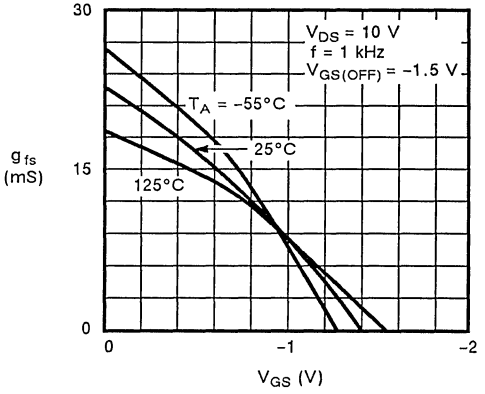
Output Characteristics ($V_{GS(OFF)}$ = -3 V)



Transfer Characteristics



Transconductance vs. Gate-Source Voltage



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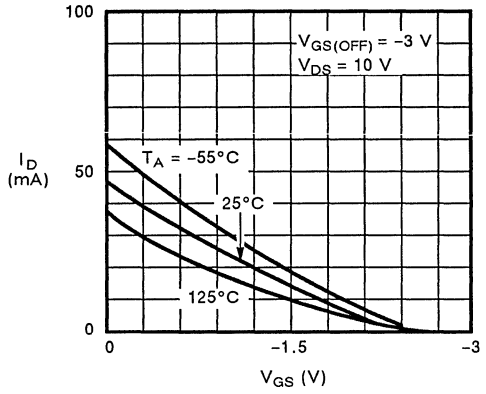
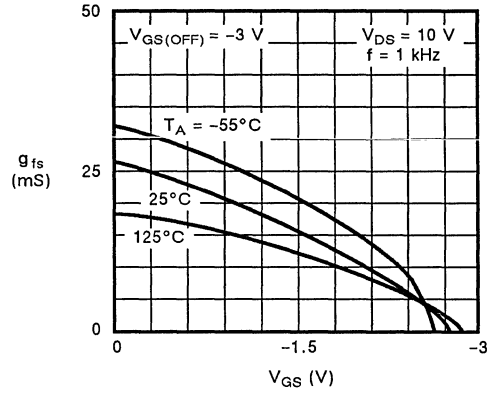
TYPICAL CHARACTERISTICS

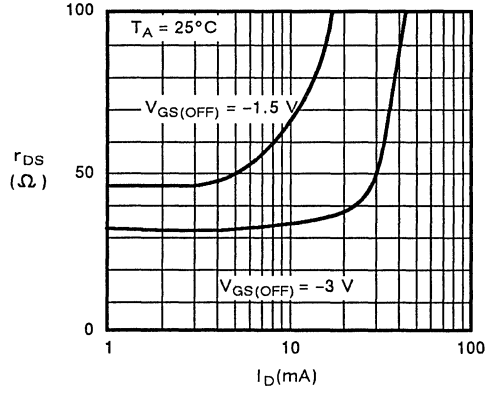
Transfer Characteristics



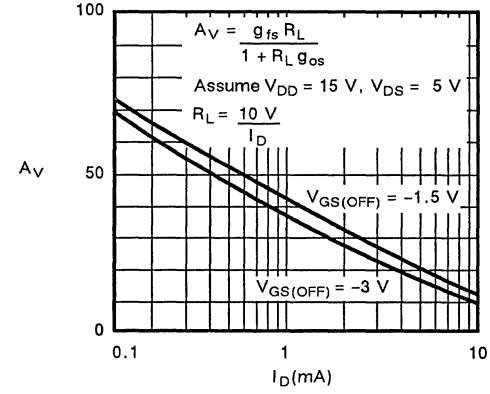
Transconductance vs. Gate-Source Voltage



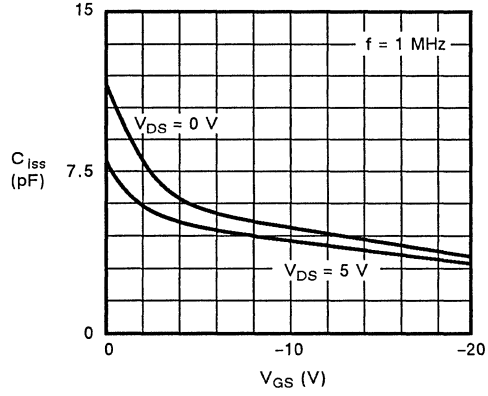
On-Resistance vs. Drain Current



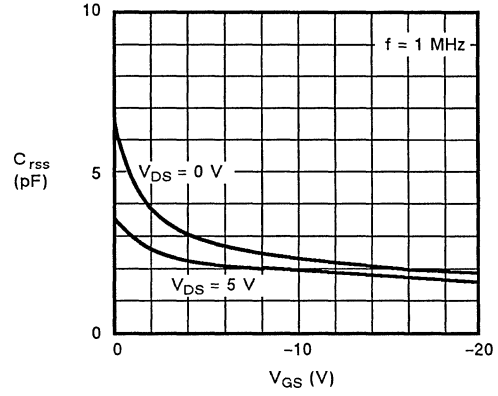
Circuit Voltage Gain vs. Drain Current



Common-Source Input Capacitance vs. Gate-Source Voltage

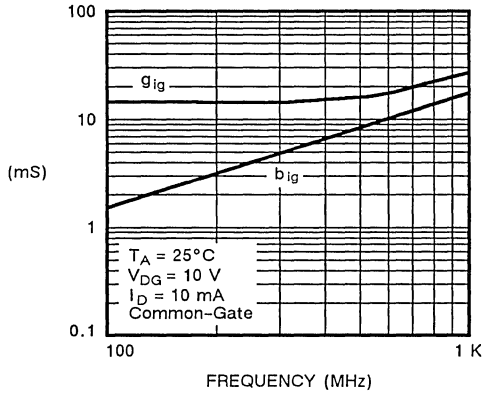


Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage

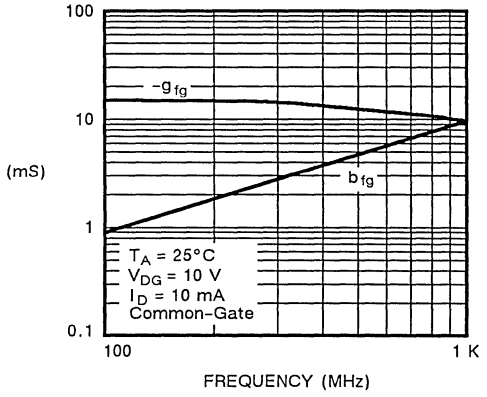


TYPICAL CHARACTERISTICS

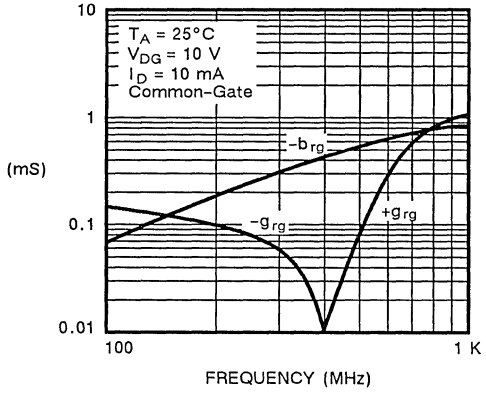
Input Admittance



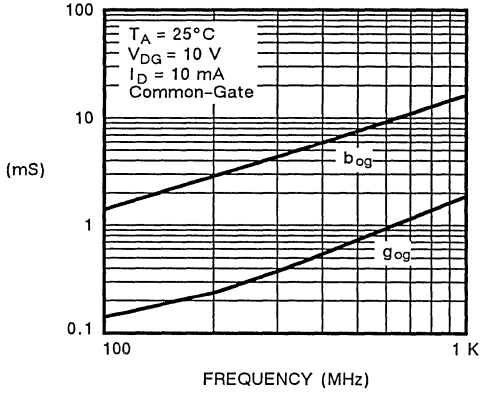
Forward Admittance



Reverse Admittance



Output Admittance



7

Siliconix incorporated

N-Channel JFET

DESIGNED FOR:

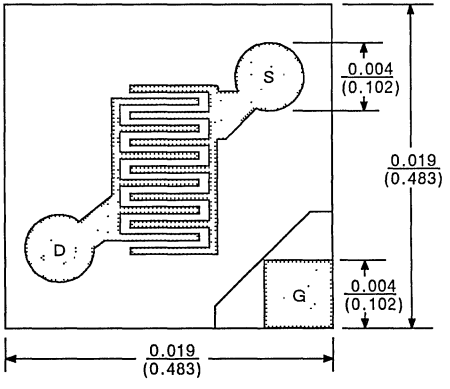
- High Frequency Amplifiers
- Mixers
- Oscillators

FEATURES

- High Power Gain
- Low Noise

TYPE	PACKAGE	DEVICE
Single	TO-92	• J210, J211, J212
	TO-71	• U440, U441
Dual	TO-78	• 2N5911, 2N5912 U443, U444
	Chip	• Available as above specifications for J210, J211, J212, U440, U441, U443, U444, and 2N5912

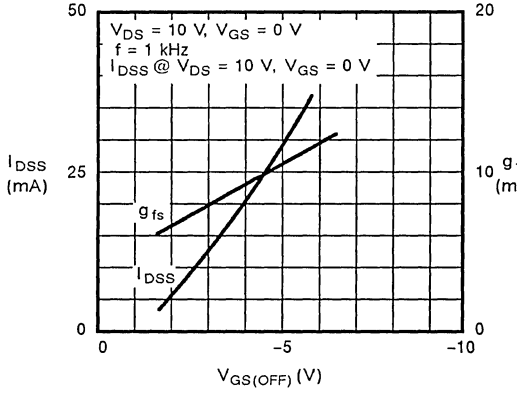
GEOMETRY DIAGRAM



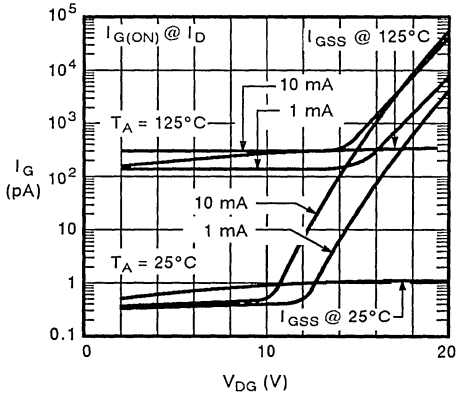
Gate also backside contact

TYPICAL CHARACTERISTICS

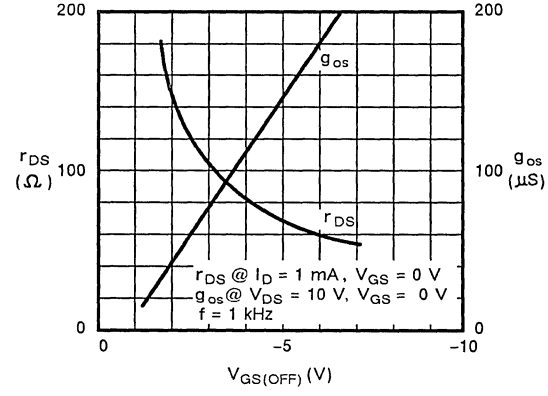
Drain Current & Transconductance vs. Gate-Source Cutoff Voltage



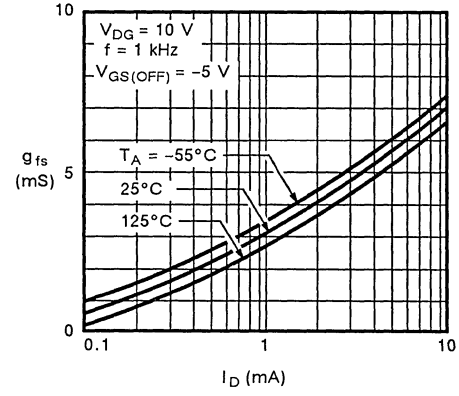
Operating Gate Current



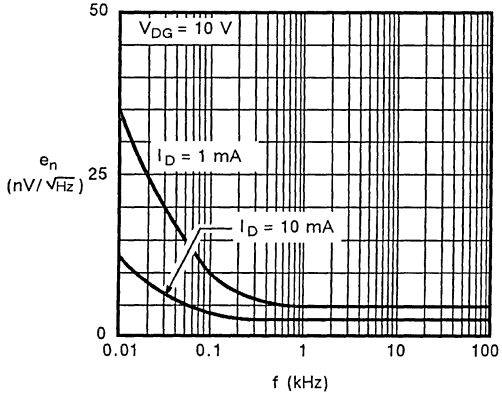
On-Resistance & Output Conductance vs. Gate-Source Cutoff Voltage



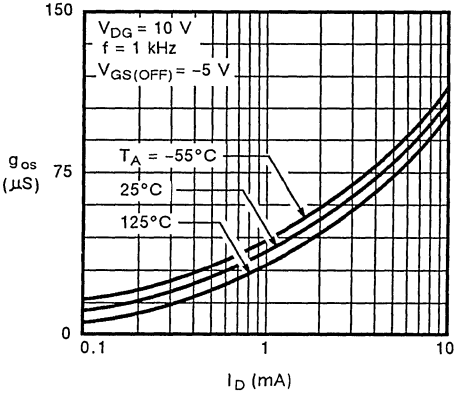
Common-Source Forward Transconductance vs. Drain Current



Equivalent Input Noise Voltage vs. Frequency



Output Conductance vs. Drain Current



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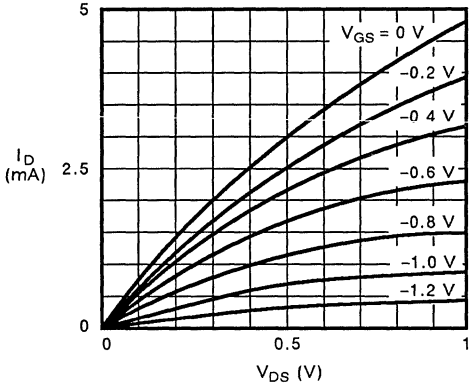
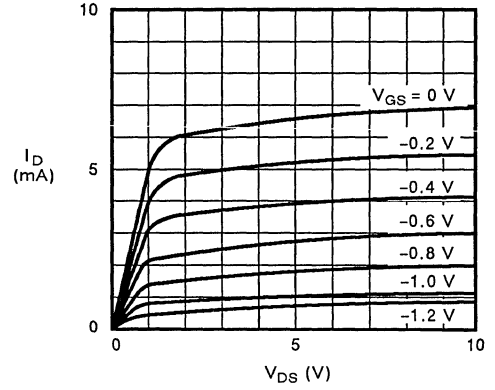
TYPICAL CHARACTERISTICS

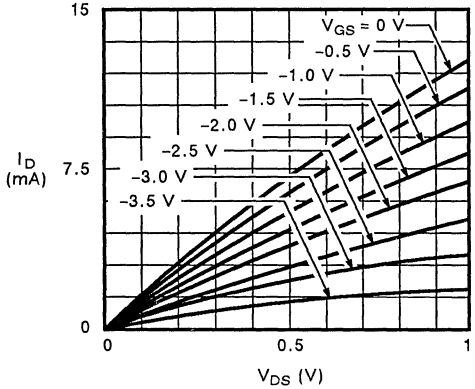
Output Characteristics ($V_{GS(OFF)}$ = -2 V)



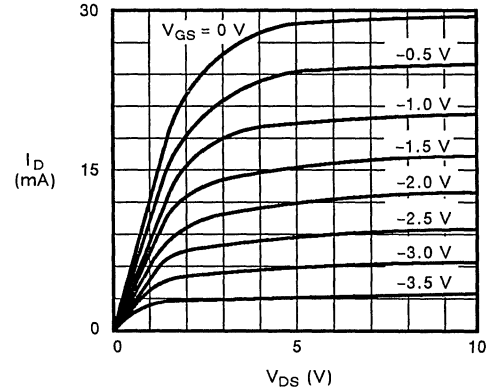
Output Characteristics ($V_{GS(OFF)}$ = -2 V)



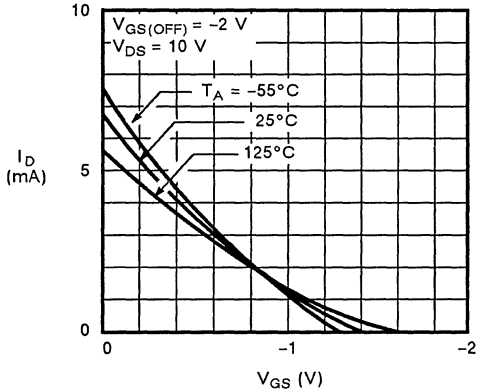
Output Characteristics ($V_{GS(OFF)}$ = -5 V)



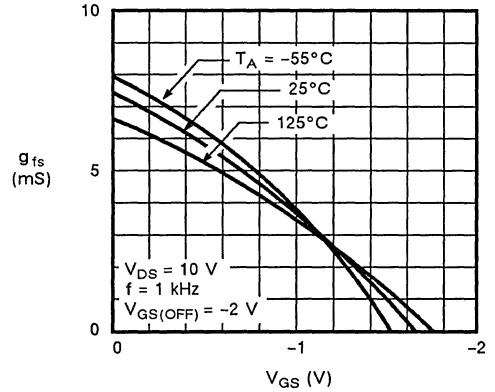
Output Characteristics ($V_{GS(OFF)}$ = -5 V)



Transfer Characteristics

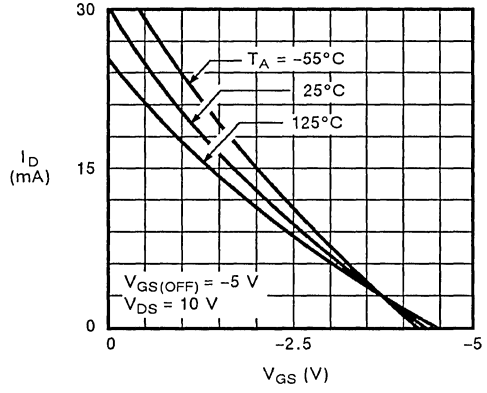


Transconductance vs. Gate-Source Voltage

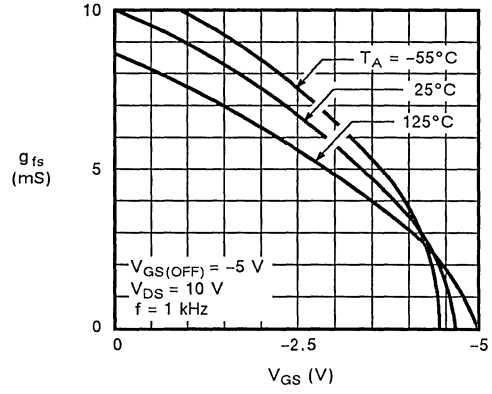


TYPICAL CHARACTERISTICS

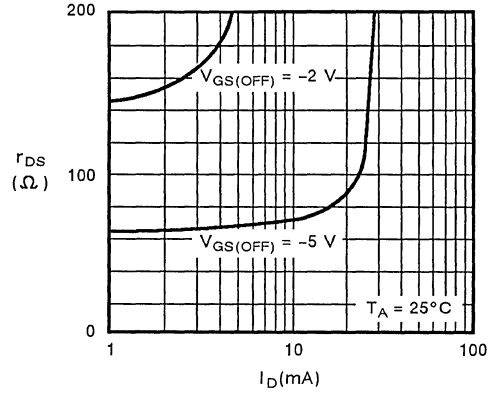
Transfer Characteristics



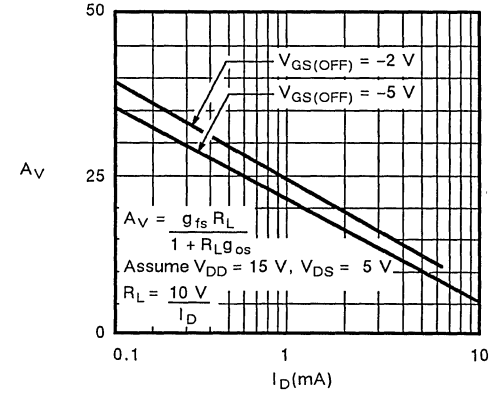
Transconductance vs. Gate-Source Voltage



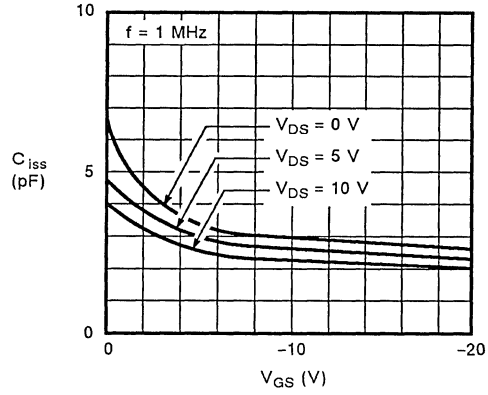
On-Resistance vs. Drain Current



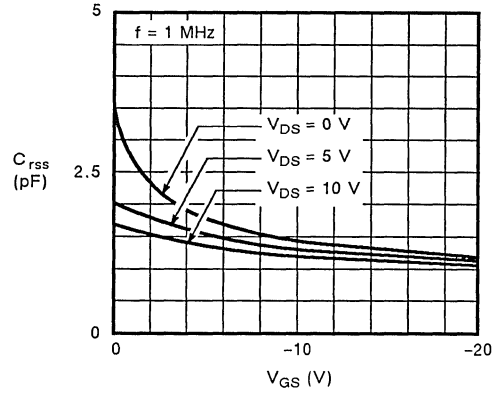
Circuit Voltage Gain vs. Drain Current



Common-Source Input Capacitance vs. Gate-Source Voltage



Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



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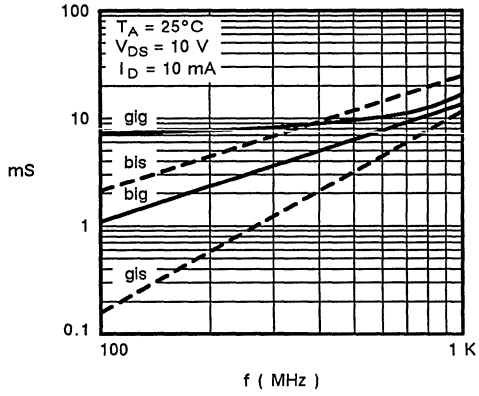
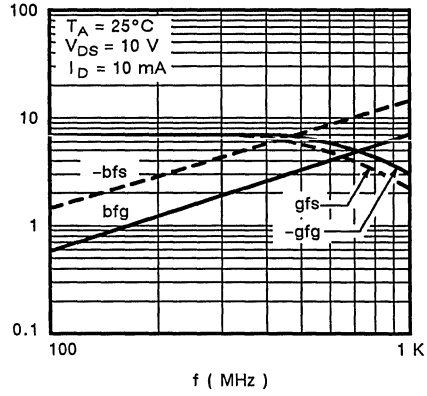
TYPICAL CHARACTERISTICS

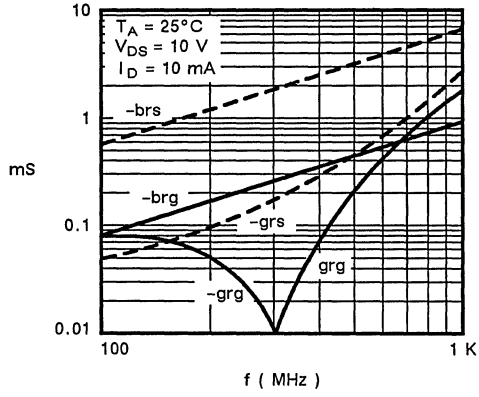
Input Admittance



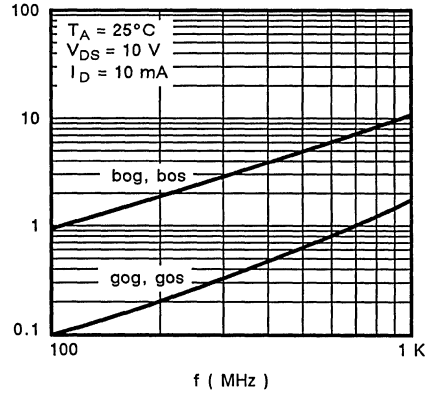
Forward Admittance



Reverse Admittance



Output Admittance



P-Channel JFET

DESIGNED FOR:

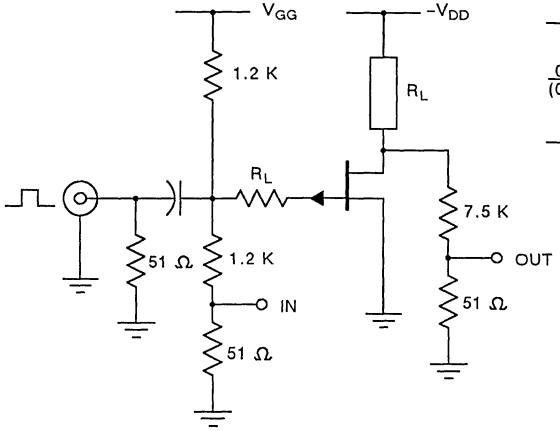
- Analog Switches
- Commutators
- Choppers
- Integrator Reset Switch

FEATURES

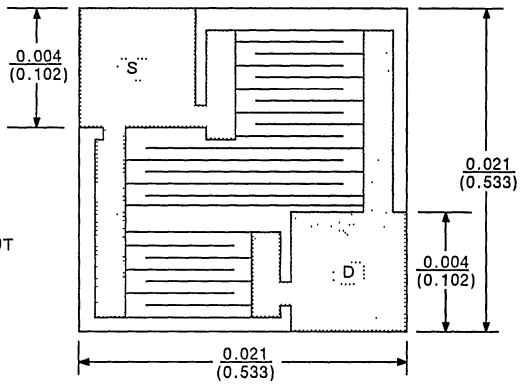
- Low Insertion Loss in Switching Systems $r_{DS(on)}$ < 75 Ω (2N5114)
- Short Sample and Hold Aperture Time C_{rss} < 7 pF
- High Off-Isolation $I_{D(OFF)}$ < 500 pA

TYPE	PACKAGE	DEVICE
Single	TO-92	• J174, J175, J176, J177 J270, J271 P1086, P1087
	SOT-23	• SST174, SST175, SST176, SST177 SST270, SST271
	TO-18	• 2N5114, 2N5115, 2N5116 (TX, TXV)
	Chip	• Available as above specifications

SWITCHING CIRCUIT



GEOMETRY DIAGRAM

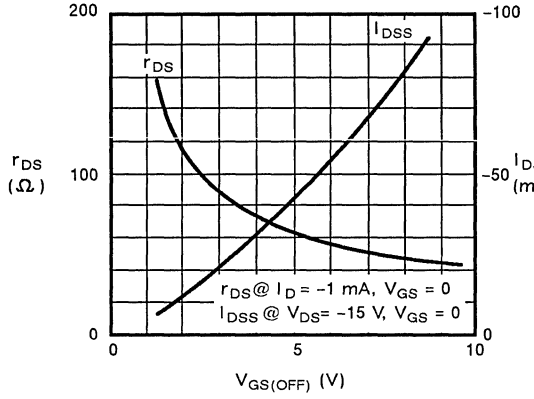


Gate backside contact

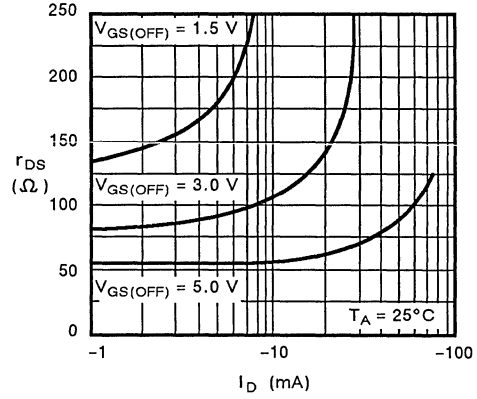
7

TYPICAL CHARACTERISTICS

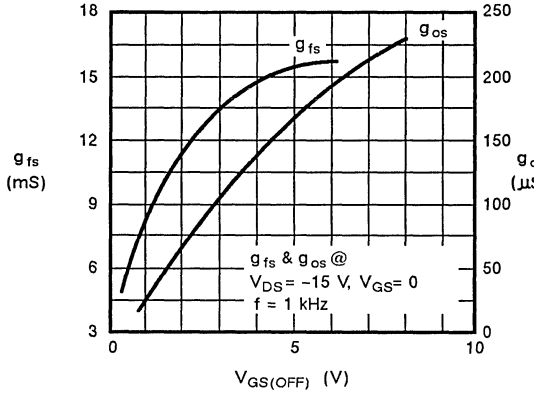
On-Resistance & Drain Current vs. Gate-Source Cutoff Voltage



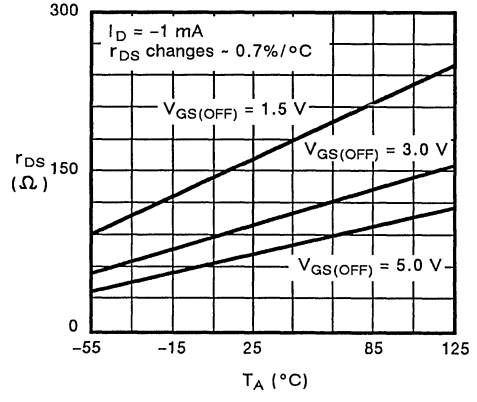
On-Resistance vs. Drain Current



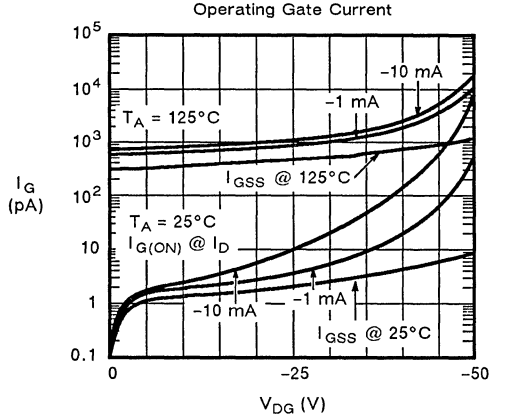
Forward Transconductance & Output Conductance vs. Gate-Source Cutoff Voltage



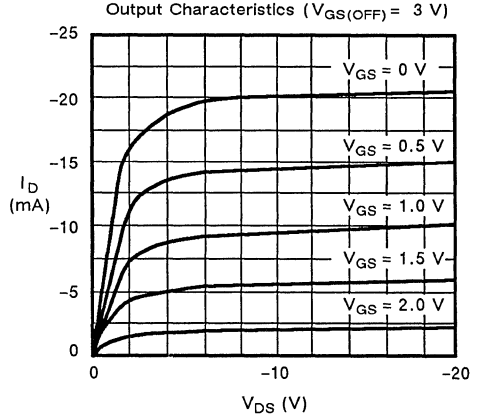
On-Resistance vs. Temperature



Operating Gate Current

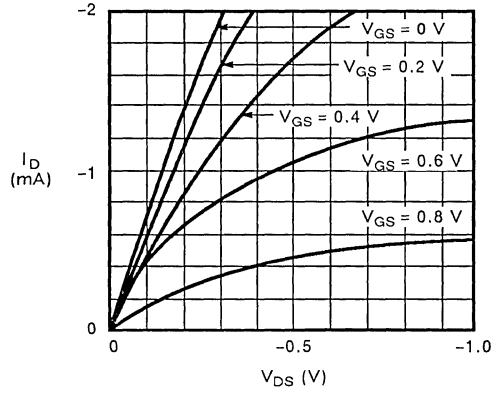


Output Characteristics ($V_{GS(OFF)}$ = 3 V)

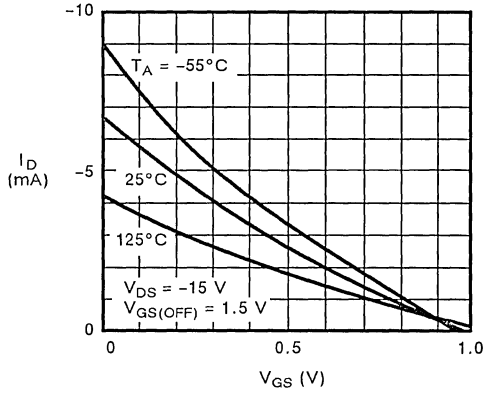


TYPICAL CHARACTERISTICS

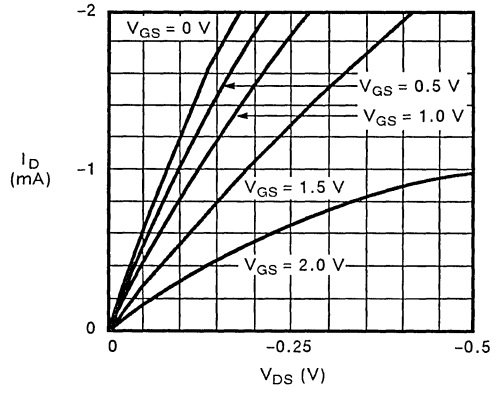
Output Characteristics ($V_{GS(OFF)}$ = 1.5 V)



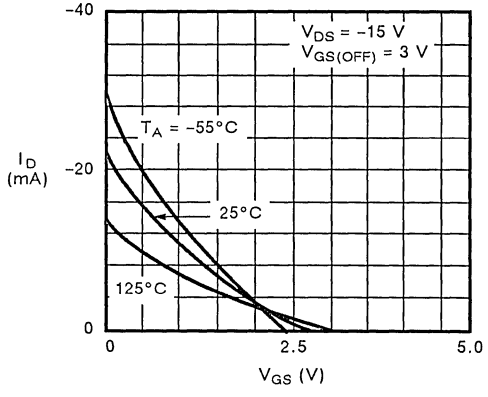
Transfer Characteristics



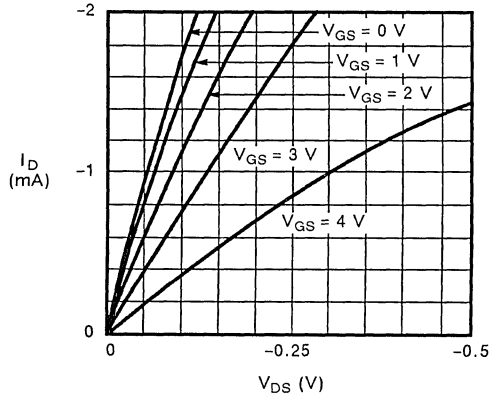
Output Characteristics ($V_{GS(OFF)}$ = 3 V)



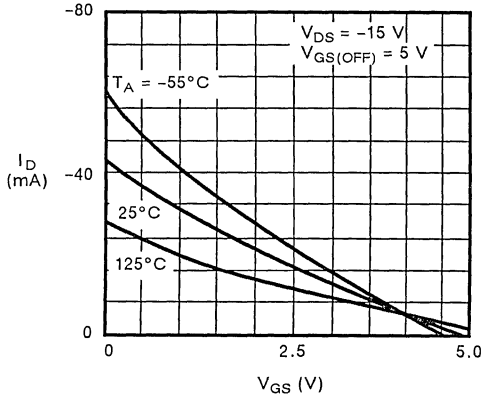
Transfer Characteristics



Output Characteristics ($V_{GS(OFF)}$ = 5 V)



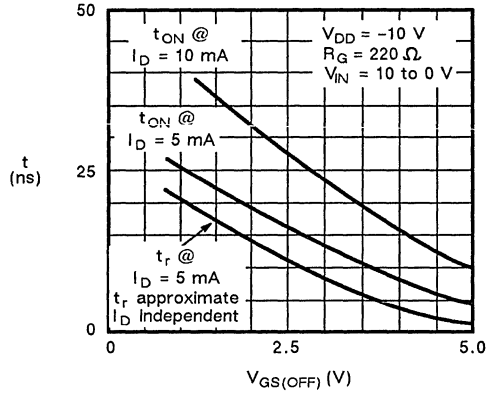
Transfer Characteristics



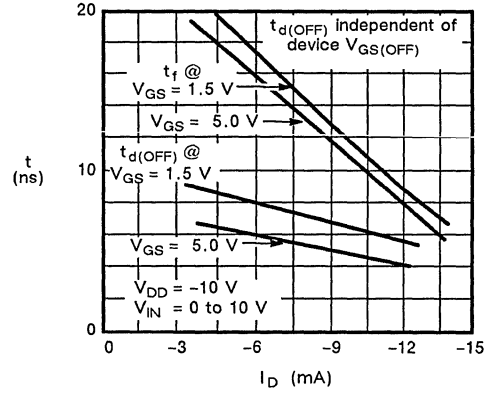
7

TYPICAL CHARACTERISTICS

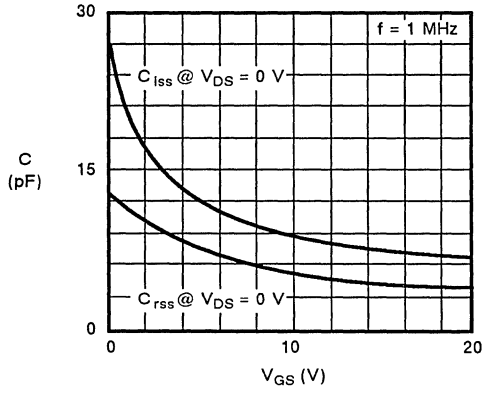
Turn-On Switching



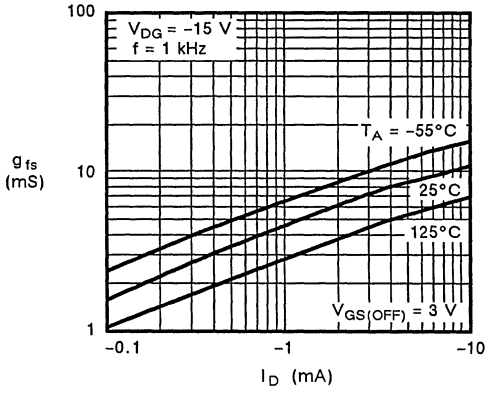
Turn-Off Switching



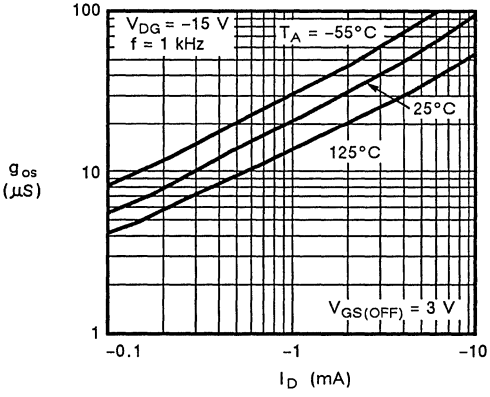
Capacitance vs. Gate-Source Voltage



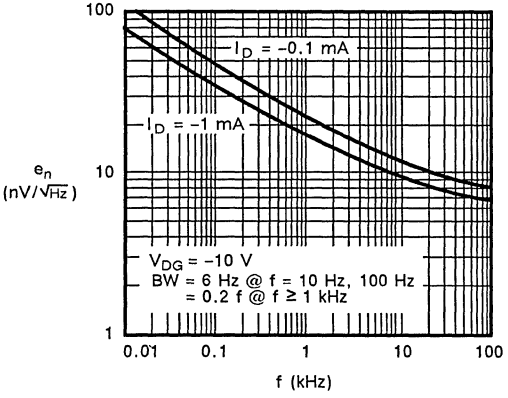
Transconductance vs. Drain Current



Output Conductance vs. Drain Current



Noise Voltage vs. Frequency



P-Channel JFET

DESIGNED FOR:

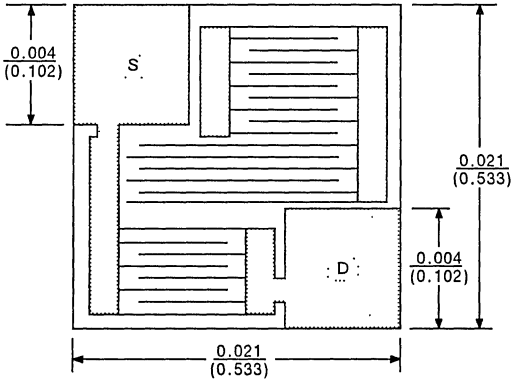
- Amplifers
- Sample and Hold
- Choppers
- Analog Switches

FEATURES

- Low $\bar{e}_n$ < 15 nV/$\sqrt{Hz}$ at 10 kHz
- Low Leakage < 10 pA at 30 V

TYPE	PACKAGE	DEVICE
Single	TO-92	• 2N5460, 2N5461, 2N5462, 2N5463, 2N5464, 2N5465
	Chip	• Available as above specifications

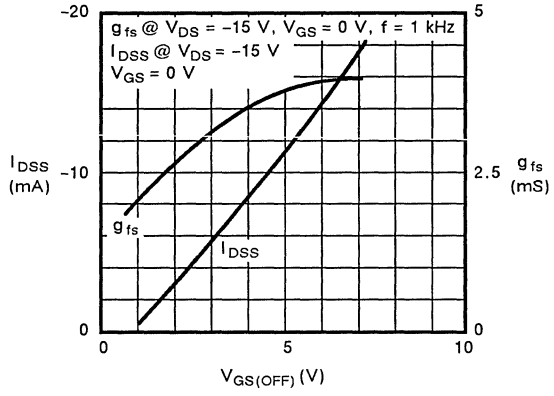
GEOMETRY DIAGRAM



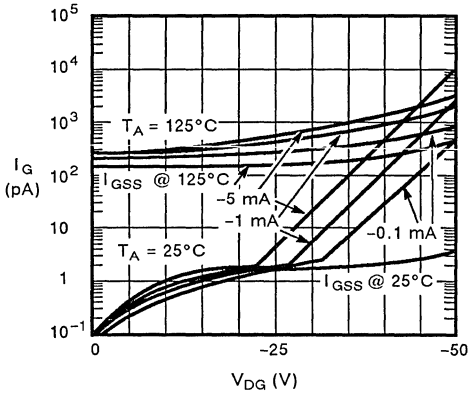
Gate backside contact

TYPICAL CHARACTERISTICS

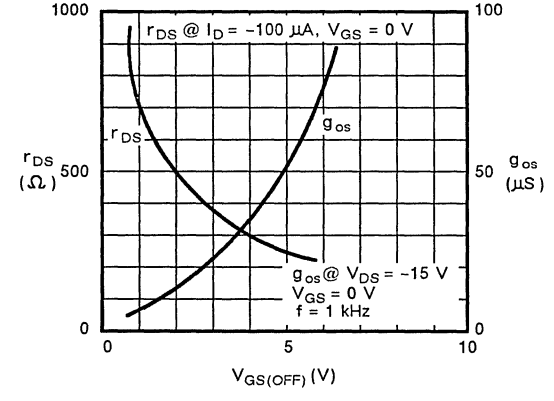
Drain Current & Transconductance vs. Gate-Source Cutoff Voltage



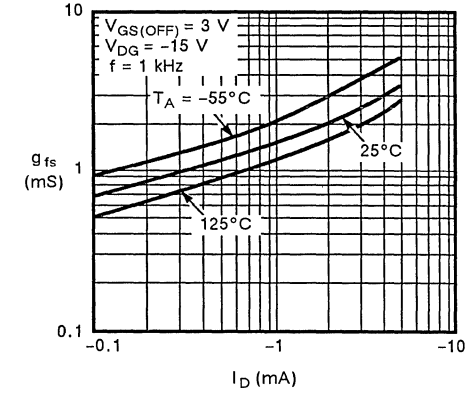
Operating Gate Current



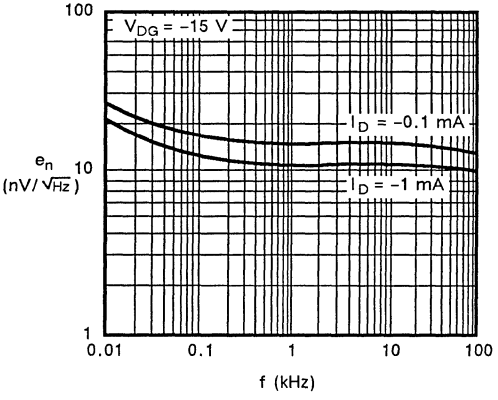
On-Resistance & Output Conductance vs. Gate-Source Cutoff Voltage



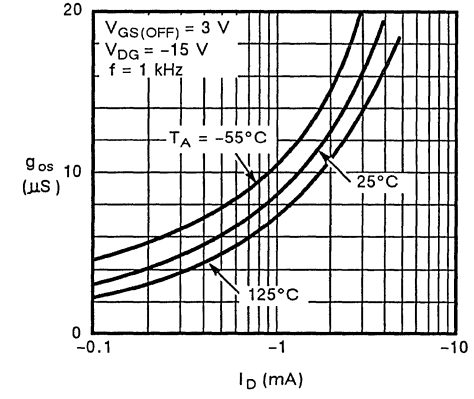
Common-Source Forward Transconductance vs. Drain Current



Equivalent Input Noise Voltage vs. Frequency

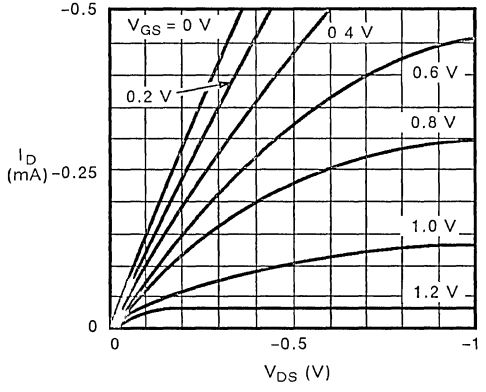


Output Conductance vs. Drain Current

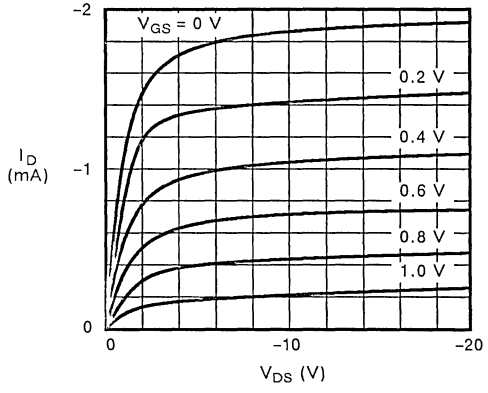


TYPICAL CHARACTERISTICS

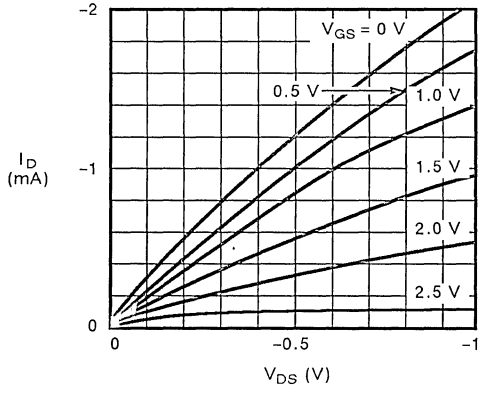
Output Characteristics ($V_{GS(OFF)}$ = 1.5 V)



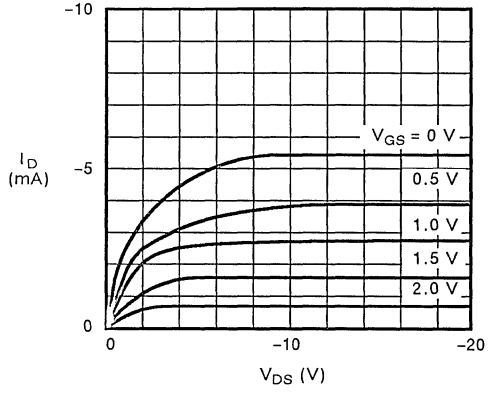
Output Characteristics ($V_{GS(OFF)}$ = 1.5 V)



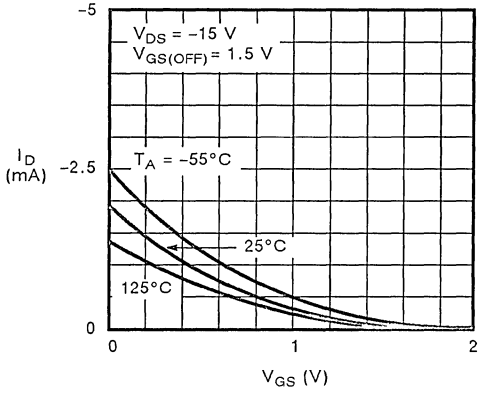
Output Characteristics ($V_{GS(OFF)}$ = 3 V)



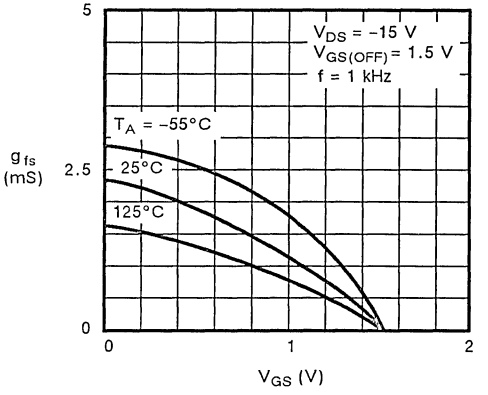
Output Characteristics ($V_{GS(OFF)}$ = 3 V)



Transfer Characteristics



Transconductance vs. Gate-Source Voltage



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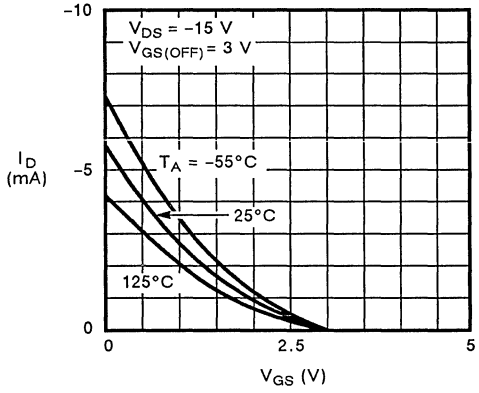
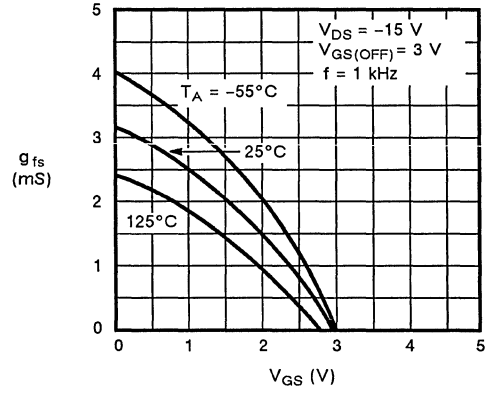
TYPICAL CHARACTERISTICS

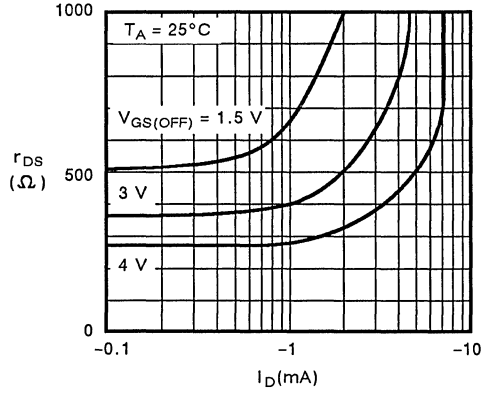
Transfer Characteristics



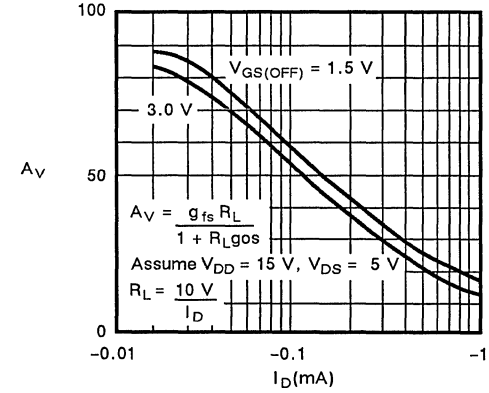
Transconductance vs. Gate-Source Voltage



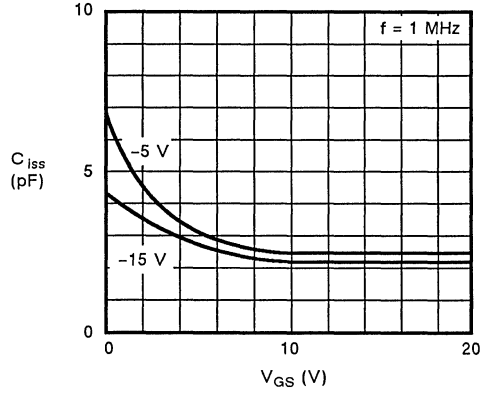
On-Resistance vs. Drain Current



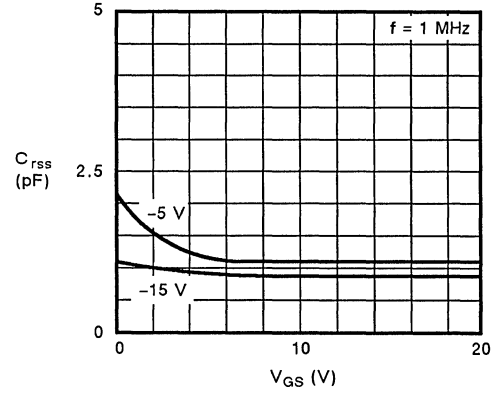
Circuit Voltage Gain vs. Drain Current



Common-Source Input Capacitance vs. Gate-Source Voltage



Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



VDDQ20

N-Channel Depletion-Mode MOSFET

DESIGNED FOR:

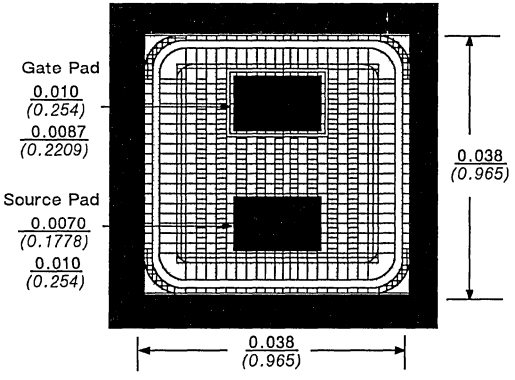
- Switching
- Amplification

FEATURES

- High Breakdown Voltage > 200 V
- Low $r_{DS(on)}$ < 3 Ω

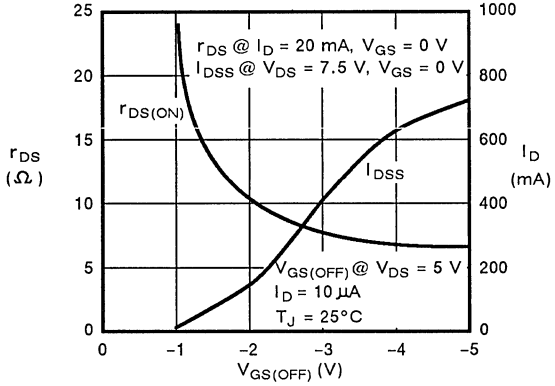
TYPE	PACKAGE	DEVICE
Single	TO-206AC	• ND2012E, ND2020E
	TO-92	• ND2012L, ND2020L
	Chip	• Available as above specifications

GEOMETRY DIAGRAM

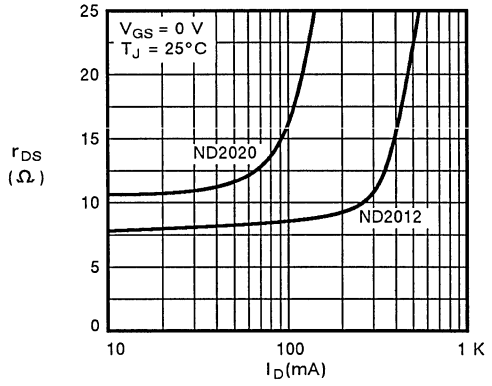


TYPICAL CHARACTERISTICS

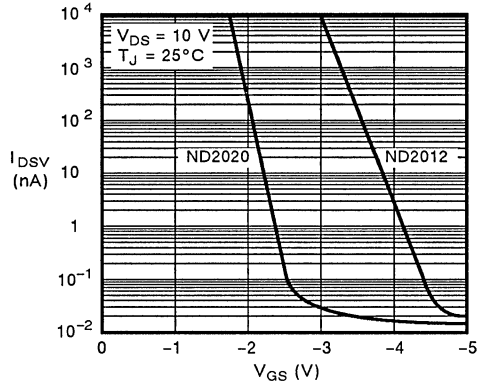
On-Resistance & Drain Current vs. Gate-Source Cutoff Voltage



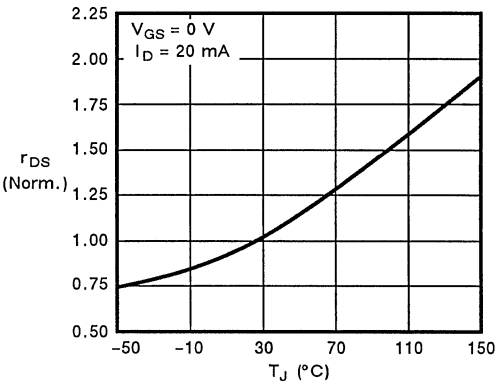
On-Resistance vs. Drain Current



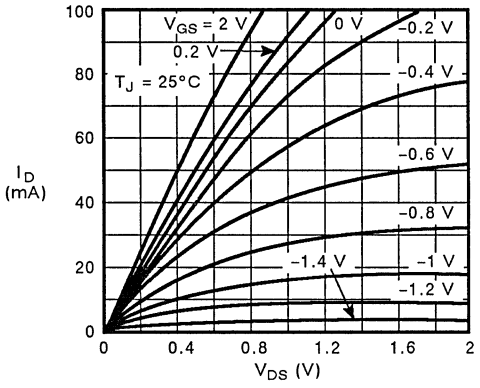
Body-Drain Leakage Current



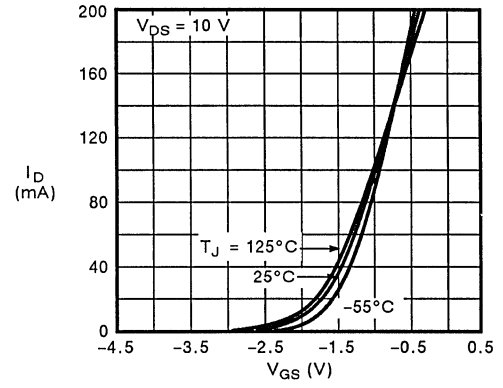
On-Resistance vs. Junction Temperature



Output Characteristics (ND2020)

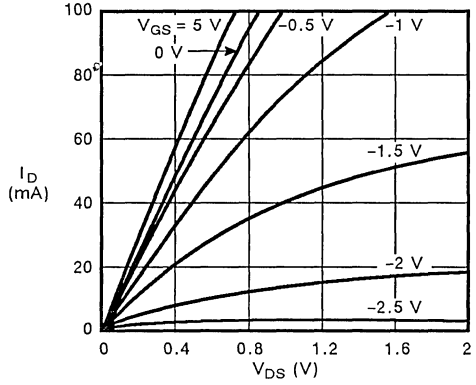


Transfer Characteristics (ND2020)

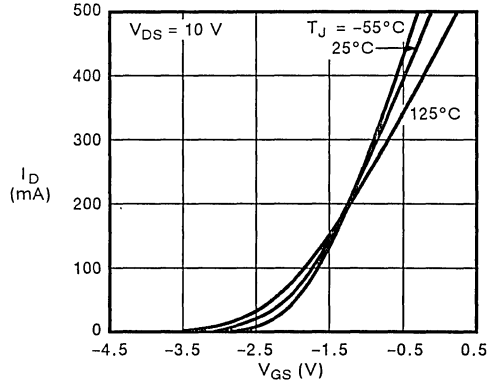


TYPICAL CHARACTERISTICS

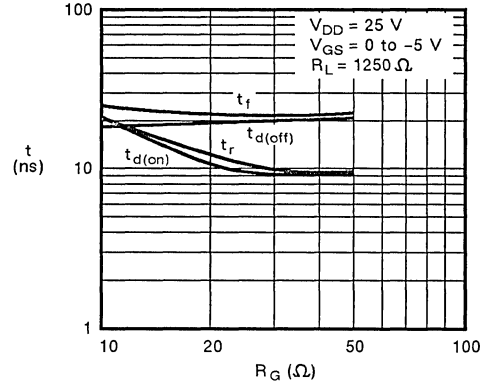
Output Characteristics (ND2012)



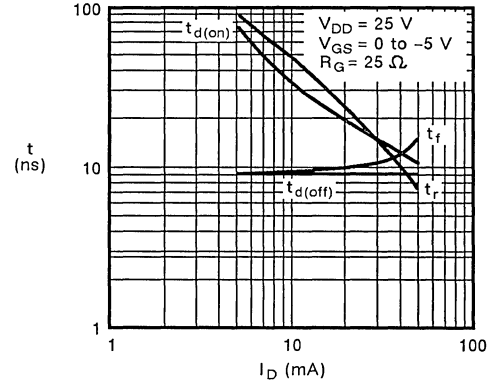
Transfer Characteristics (ND2012)



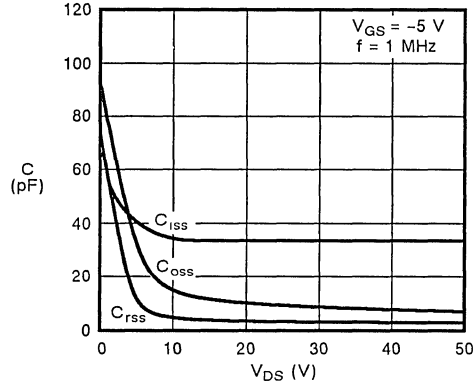
Effects of Drive Resistance



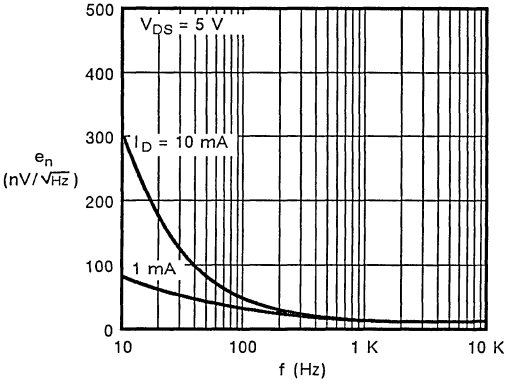
Effects on Load Conditions



Capacitance



Equivalent Input Noise Voltage vs. Frequency



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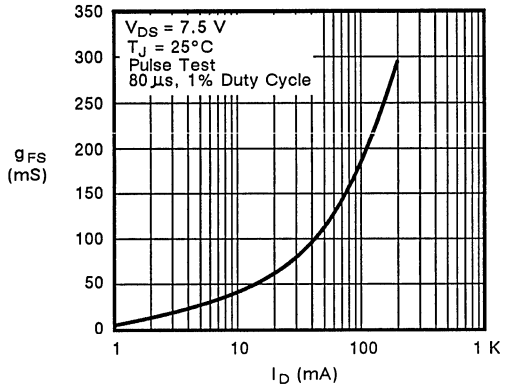
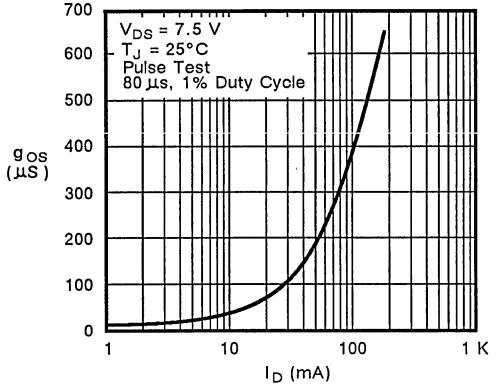
TYPICAL CHARACTERISTICS

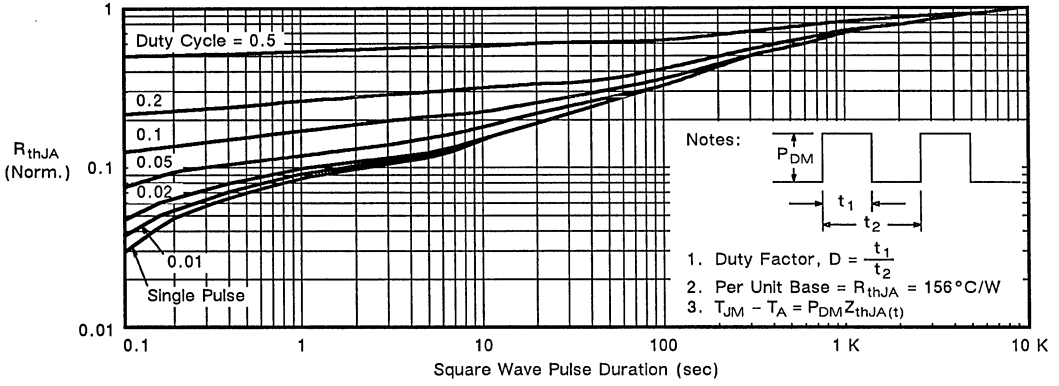
Forward Transconductance vs. Drain Current



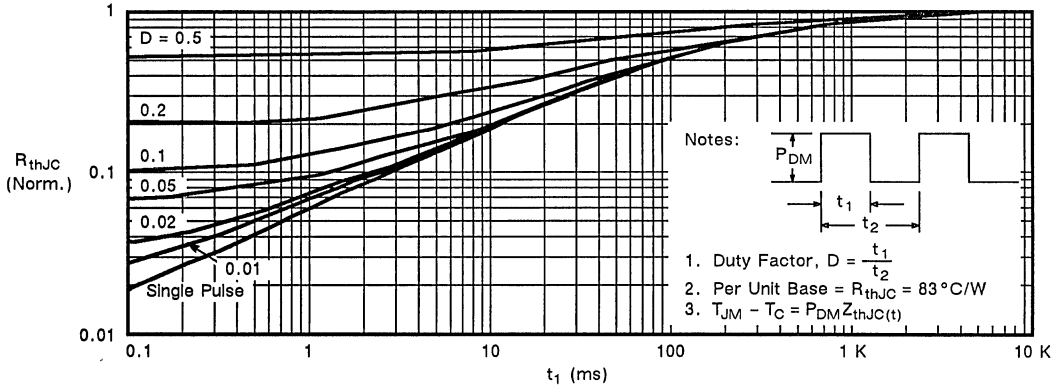
Output Conductance vs. Drain Current



Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



Transient Thermal Response (TO-206AC)



N-Channel Depletion-Mode MOSFET

DESIGNED FOR:

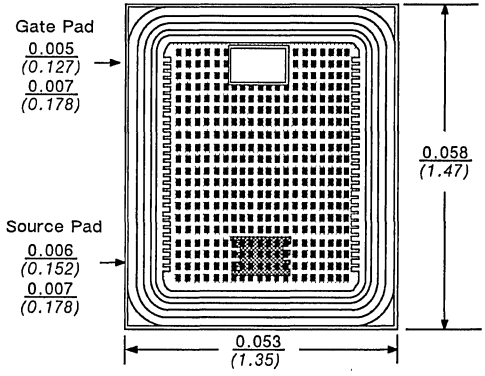
- Switching
- Amplification

FEATURES

- High Breakdown > 240 V
- Low $r_{DS(on)}$ < 10 Ω

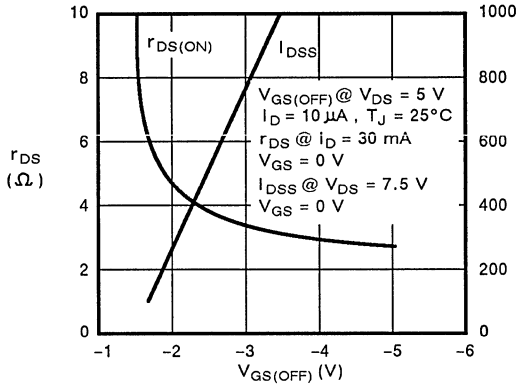
TYPE	PACKAGE	DEVICE
Single	TO-205AD	• ND2406B, ND2410B
	TO-92	• ND2406L, ND2410L
	Chip	• Available as above specifications

GEOMETRY DIAGRAM

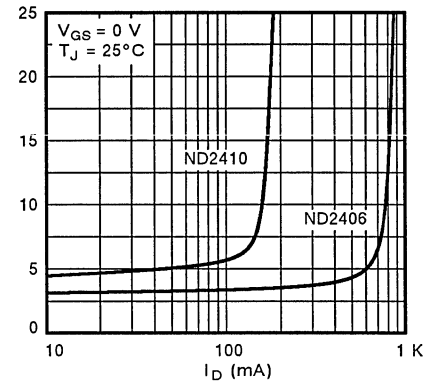


TYPICAL CHARACTERISTICS

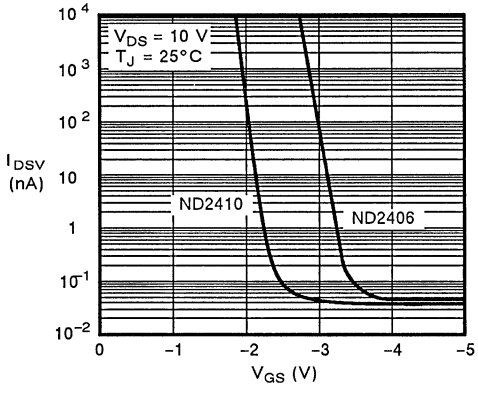
On-Resistance & Drain Current vs. Gate-Source Cutoff Voltage



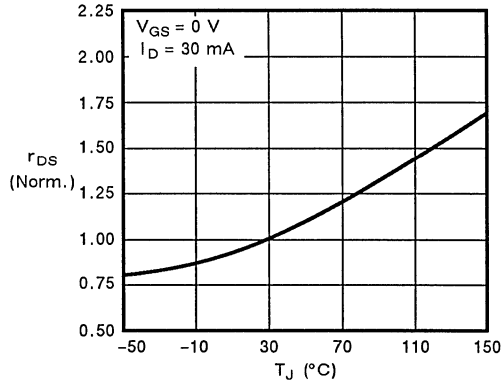
On-Resistance vs. Drain Current



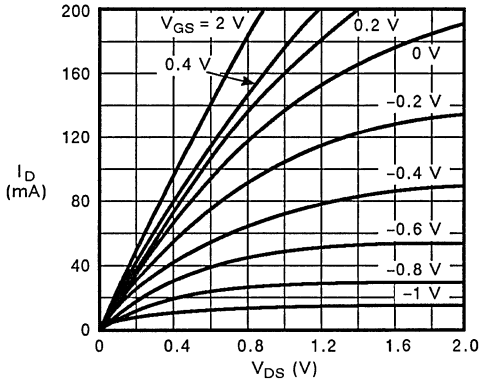
Body-Drain Leakage Current



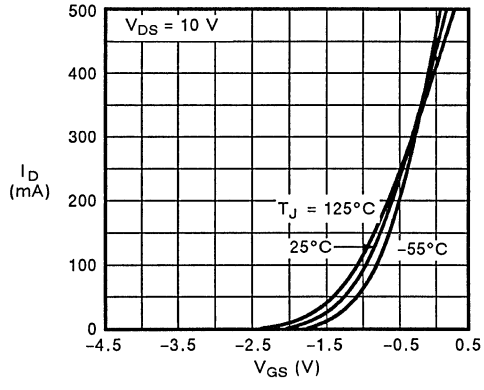
On-Resistance vs. Junction Temperature



Output Characteristics (ND2410)

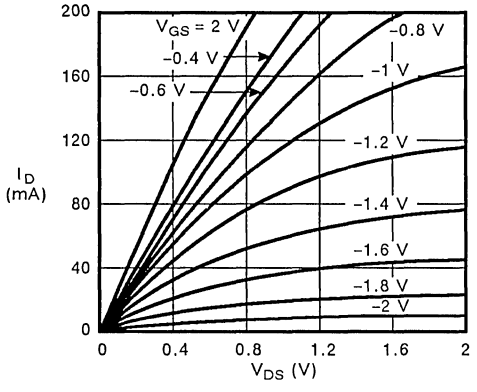


Transfer Characteristics (ND2410)

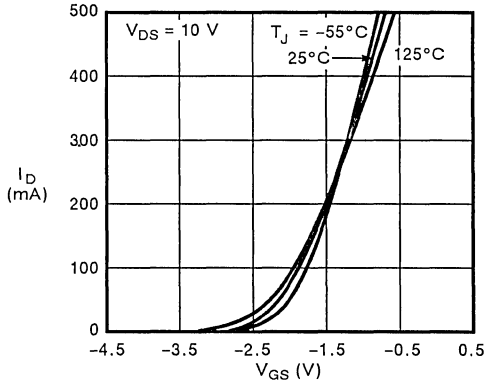


TYPICAL CHARACTERISTICS

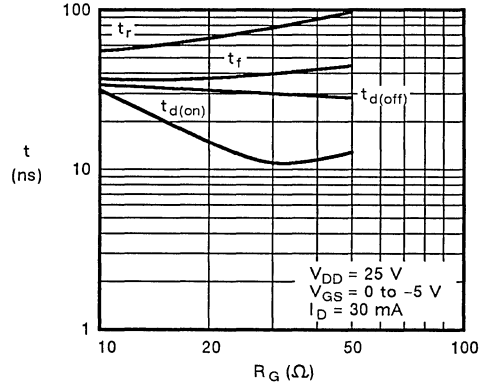
Output Characteristics (ND2406)



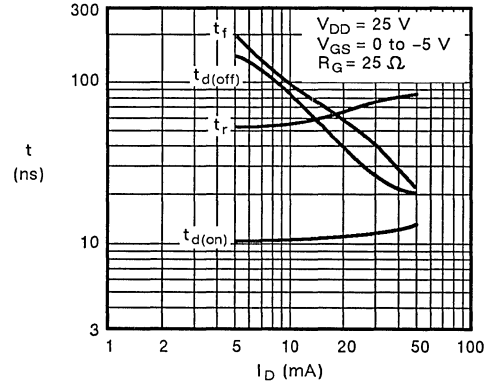
Transfer Characteristics (ND2406)



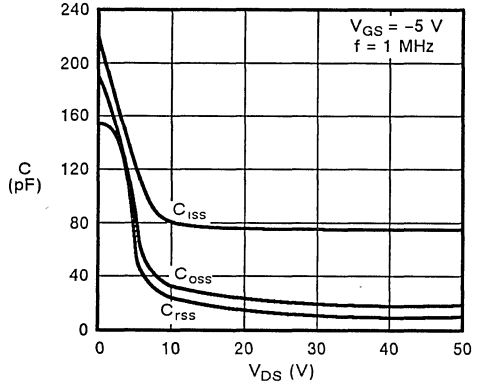
Effects of Drive Resistance



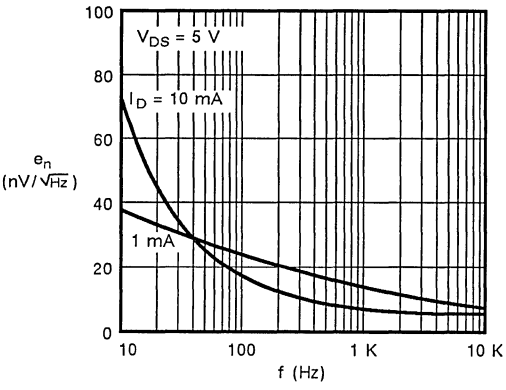
Effects on Load Conditions



Capacitance



Equivalent Input Noise Voltage vs. Frequency



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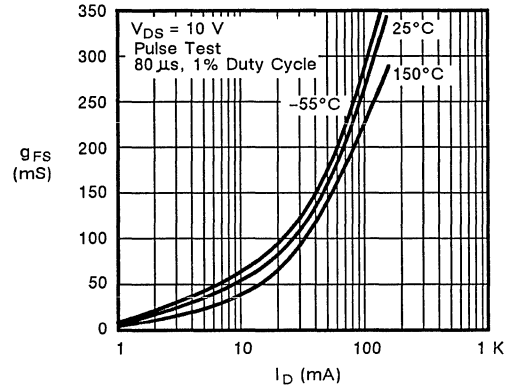
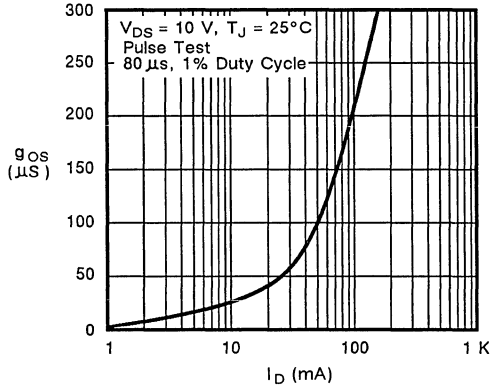
TYPICAL CHARACTERISTICS

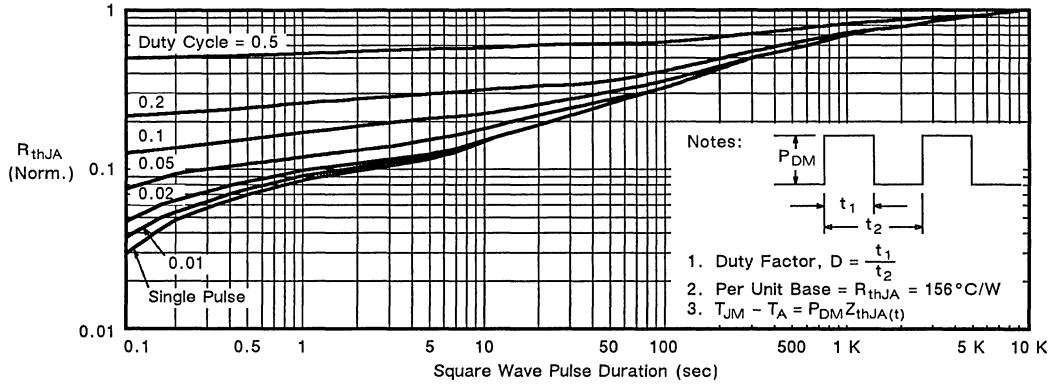
Transconductance



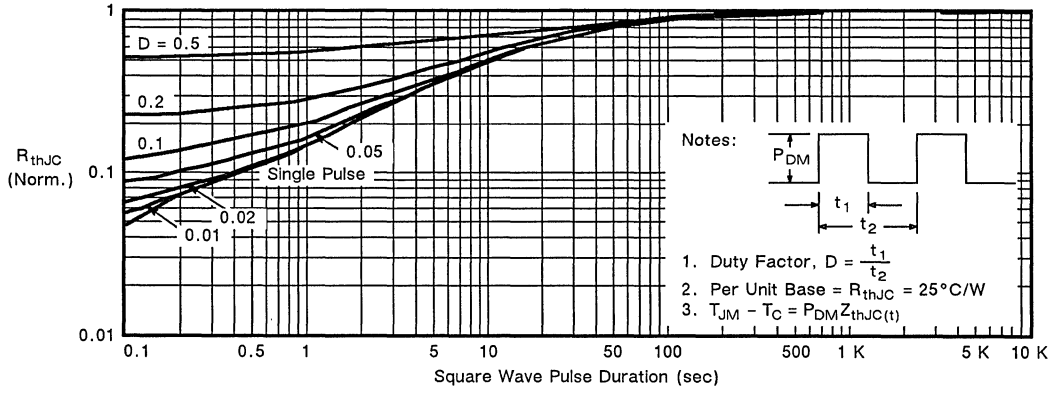
Output Conductance vs. Drain Current



Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



Transient Thermal Response (TO-205AD)



N-Channel Enhancement-Mode MOSFET

DESIGNED FOR:

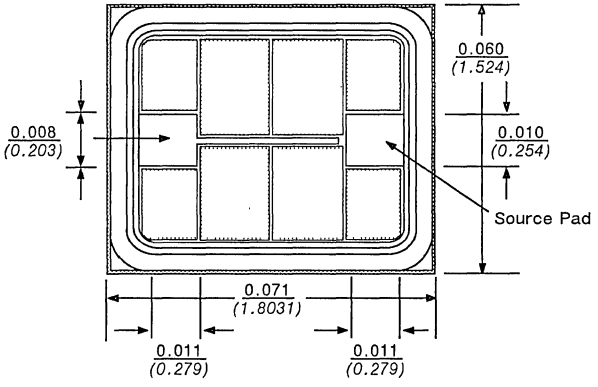
- Switching
- Amplification

FEATURES

- High Breakdown > 240 V
- Low $r_{DS(on)}$ < 6 Ω

TYPE	PACKAGE	DEVICE
Single	TO-205AD	• VN1706B, VN2406B
	TO-220	• VN1706D, VN2406D
	TO-92	• VN1706L, VN2406L
	TO-237	• VN1706M, VN1710M, VN2406M
	Chip	• Available as above specifications

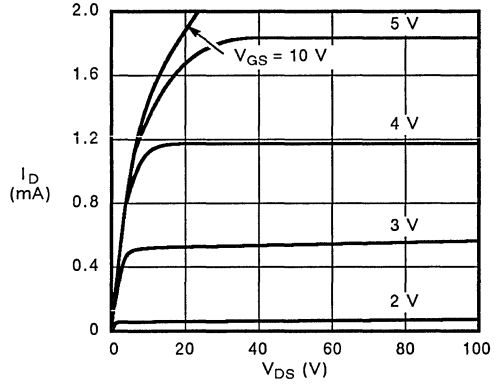
GEOMETRY DIAGRAM



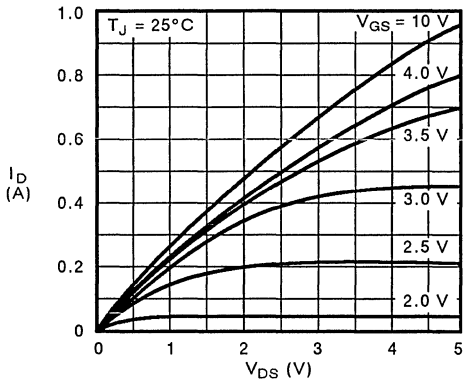
7

TYPICAL CHARACTERISTICS

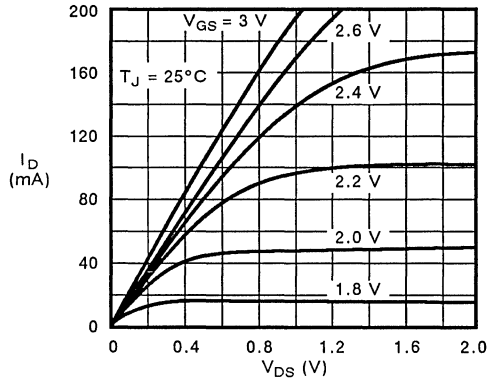
Output Characteristics



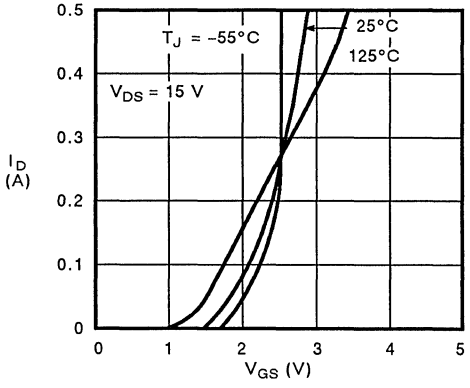
Ohmic Region Characteristics



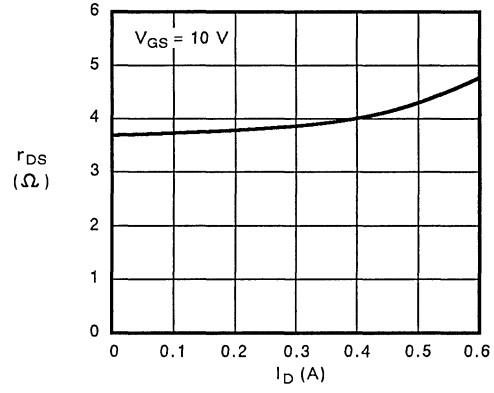
Output Characteristics for Low Gate Drive



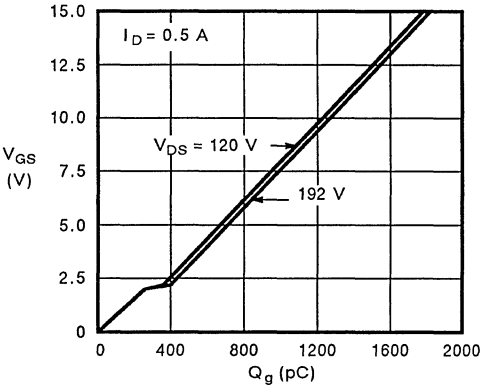
Transfer Characteristics



On-Resistance

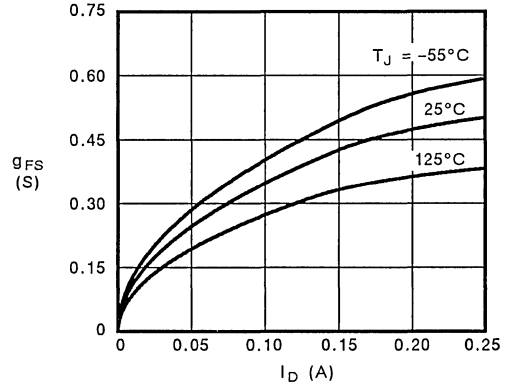


Gate Charge

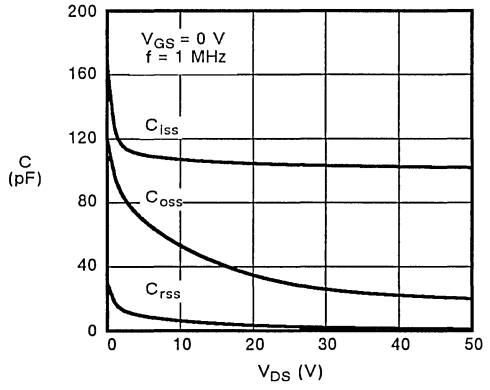


TYPICAL CHARACTERISTICS

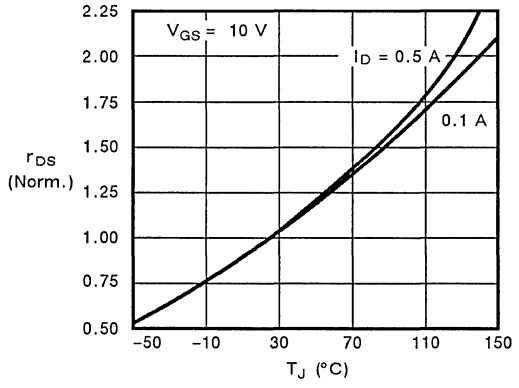
Transconductance



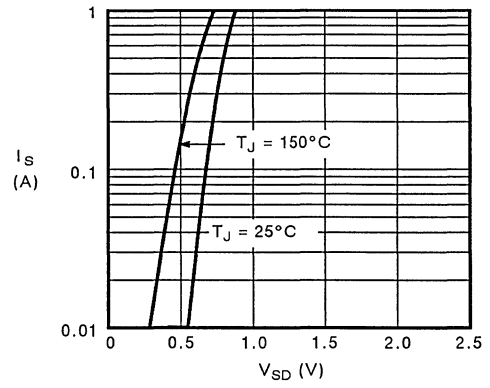
Capacitance



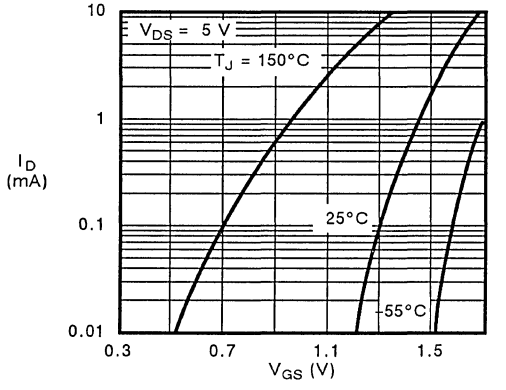
On-Resistance vs. Junction Temperature



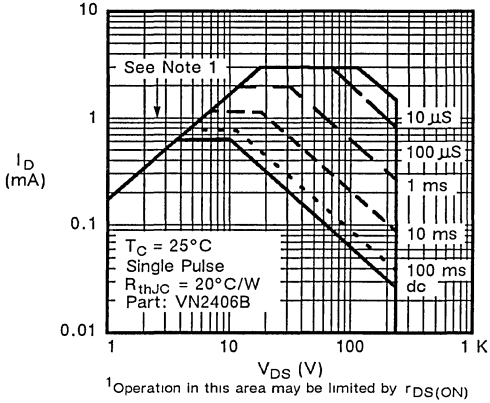
Source-Drain Diode Forward Voltage



Threshold Region



Safe Operating Area

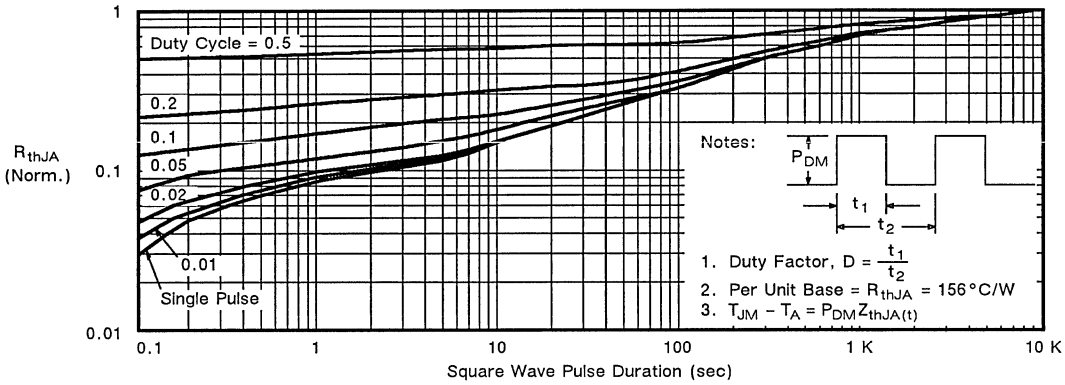


[1]Operation in this area may be limited by $r_{DS(ON)}$

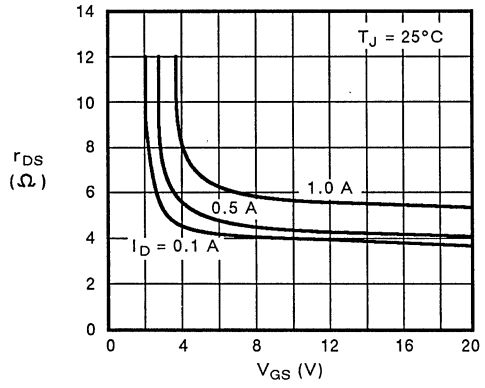
7

TYPICAL CHARACTERISTICS

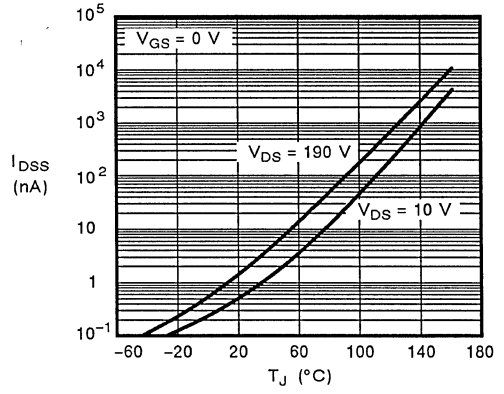
Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



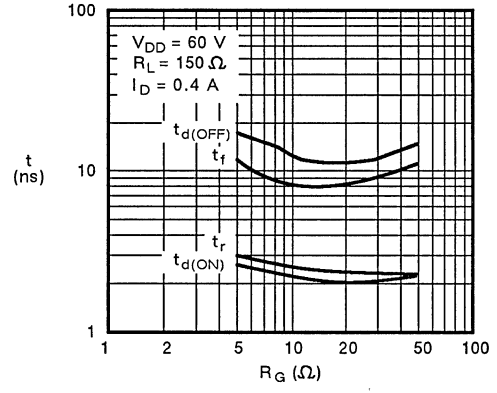
On-Resistance vs. Gate to Source Voltage



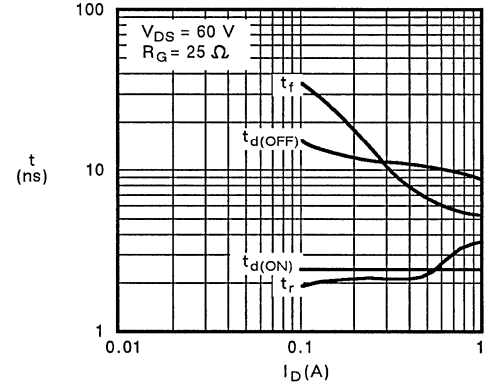
Off State Current



Drive Resistance Effects on Switching

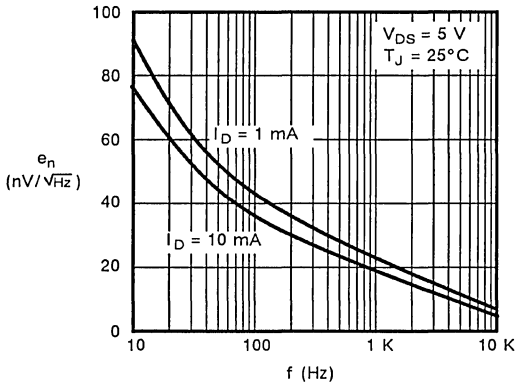


Load Condition Effects on Switching

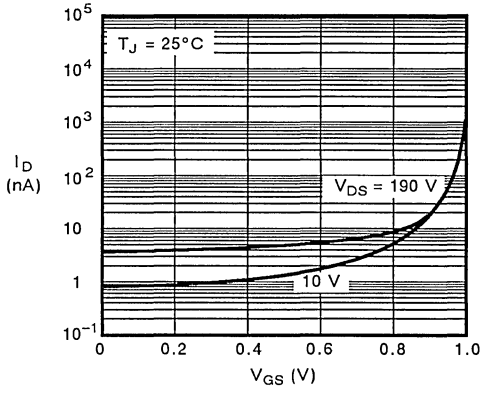


TYPICAL CHARACTERISTICS

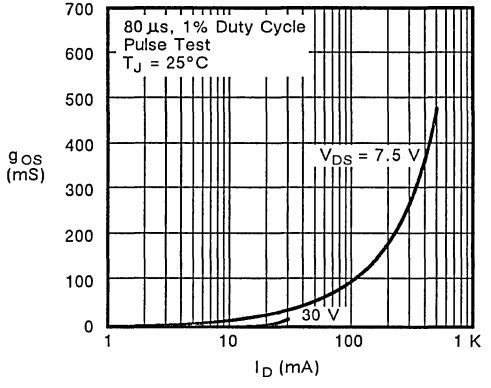
Equivalent Input Noise Voltage vs. Frequency



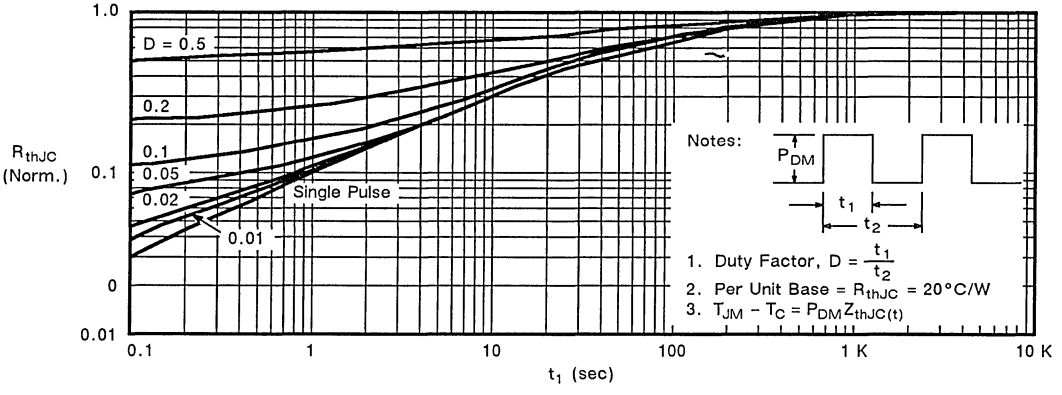
Body Drain Leakage Current



Output Conductance vs. Drain Current



Transient Thermal Response (TO-205AD)



7

Siliconix incorporated

N-Channel Enhancement-Mode MOSFET

DESIGNED FOR:

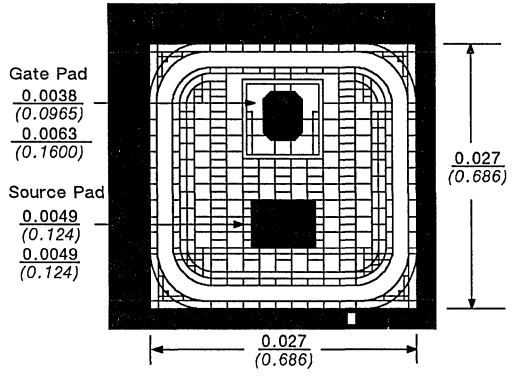
- Switching
- Amplification

FEATURES

- High Breakdown > 240 V
- Available in Surface Mount SOT-23

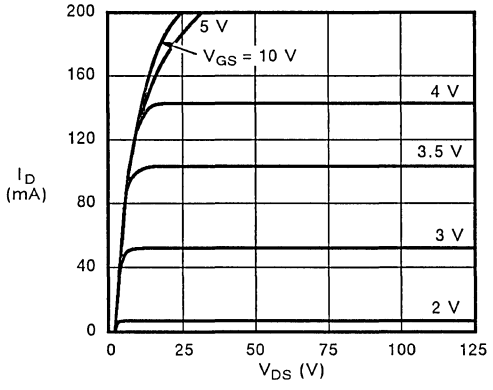
TYPE	PACKAGE	DEVICE
Single	To-92	• 2N7007
	SOT-23	• 2N7001
	Chip	• Available as above specifications

GEOMETRY DIAGRAM

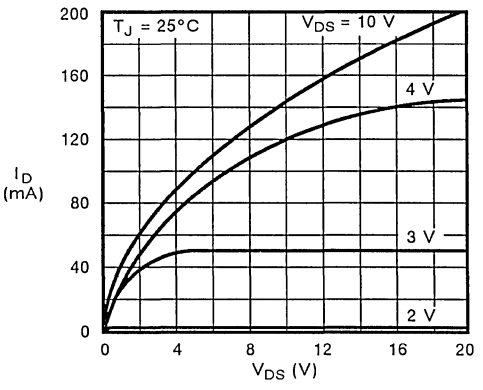


TYPICAL CHARACTERISTICS

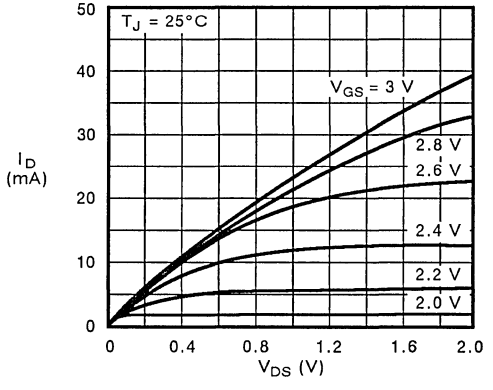
Output Characteristics



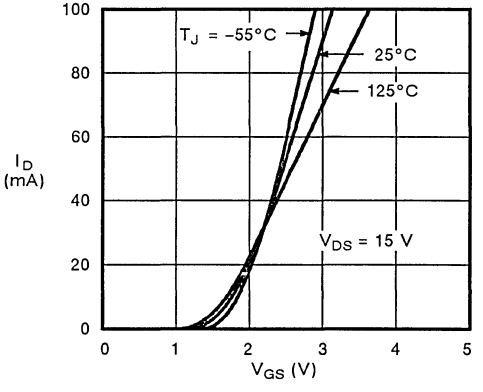
Ohmic Region Characteristics



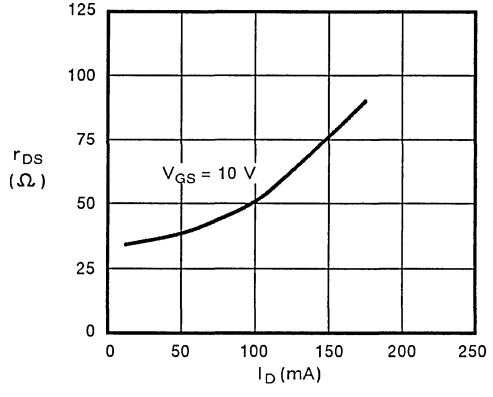
Output Characteristics for Low Gate Drive



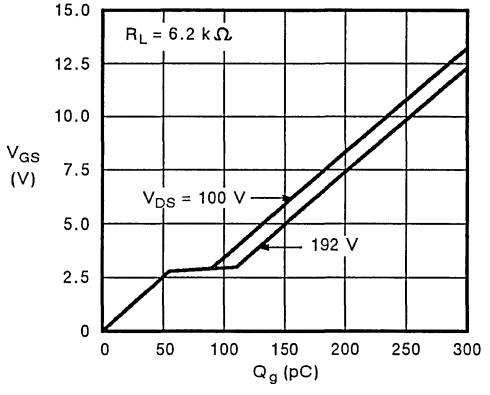
Transfer Characteristics



On-Resistance



Gate Charge



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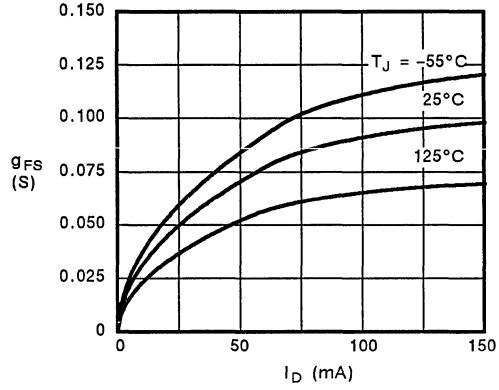
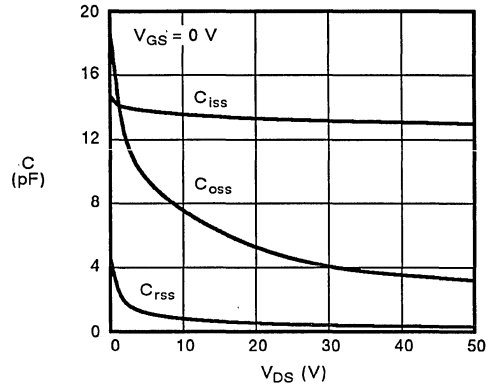
TYPICAL CHARACTERISTICS

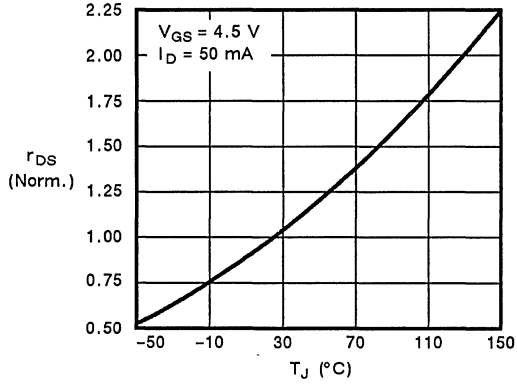
Transconductance



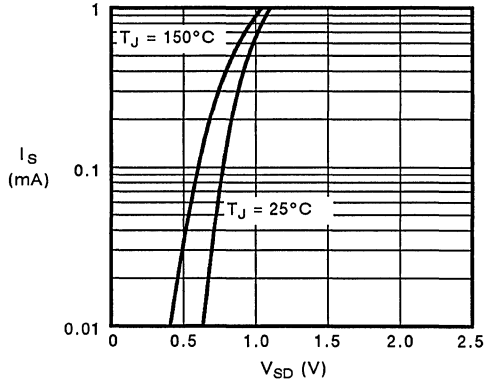
Capacitance



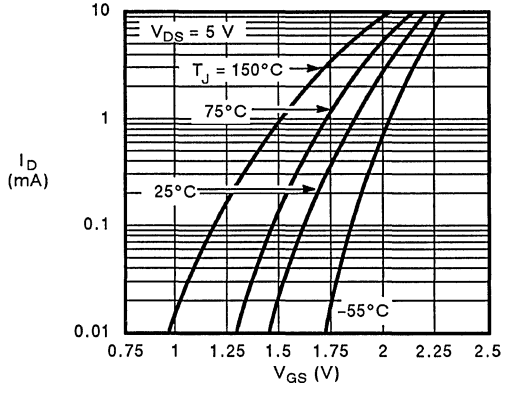
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

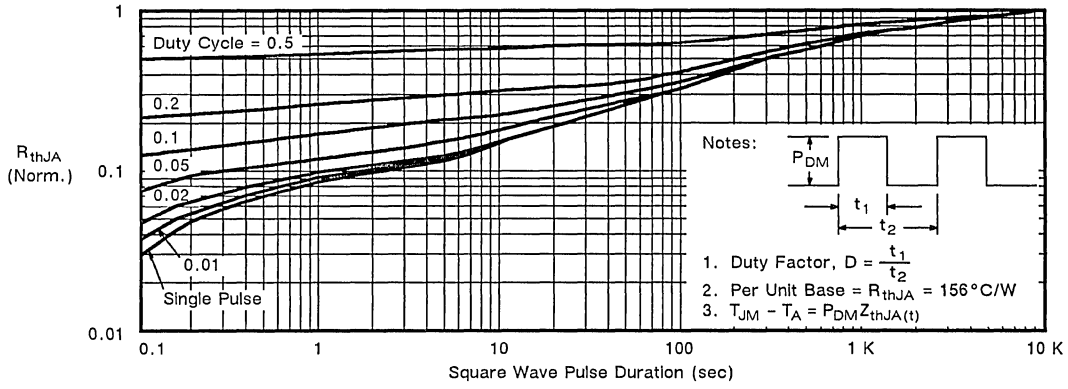


Threshold Region

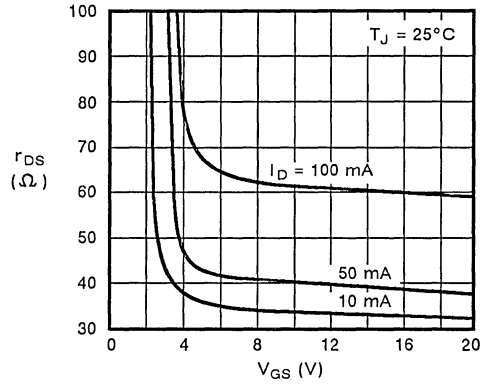


TYPICAL CHARACTERISTICS

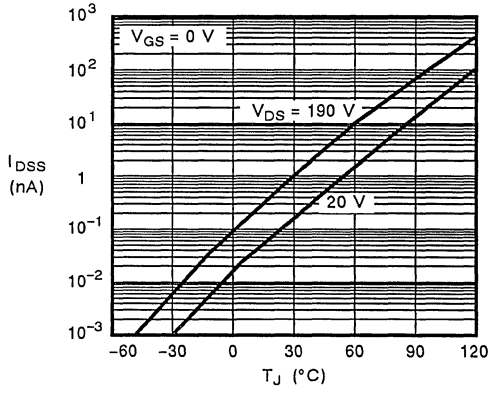
Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



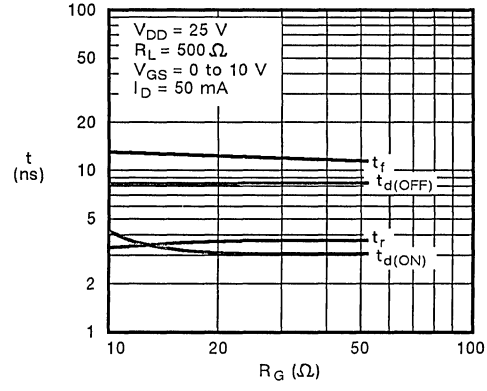
On-Resistance vs. Gate to Source Voltage



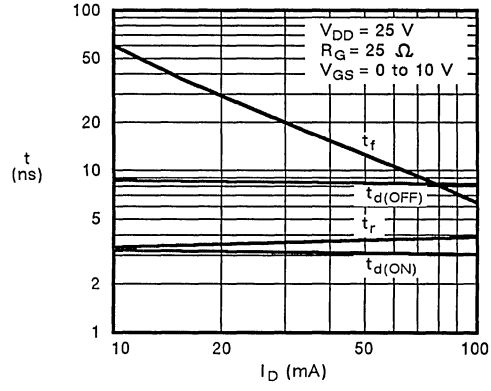
Off State Current



Drive Resistance Effects on Switching



Load Condition Effects on Switching



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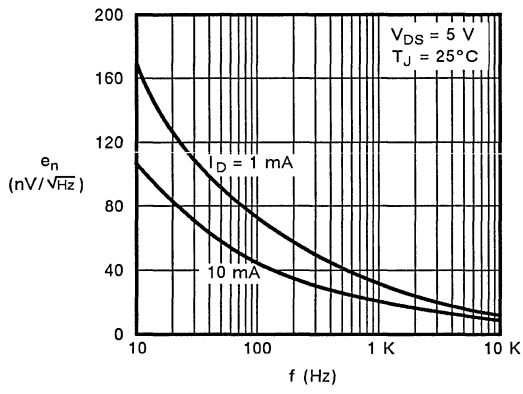
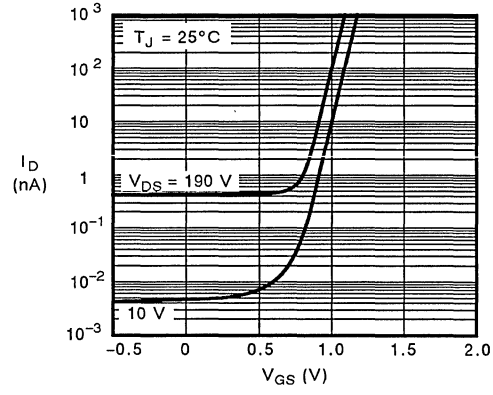
TYPICAL CHARACTERISTICS

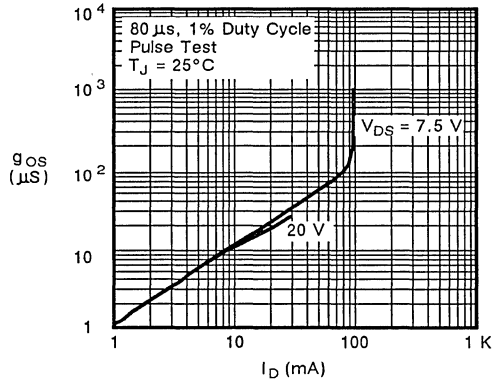
Equivalent Input Noise Voltage vs. Frequency



Body Drain Leakage Current



Output Conductance vs. Drain Current



N-Channel Enhancement-Mode MOSFET

DESIGNED FOR:

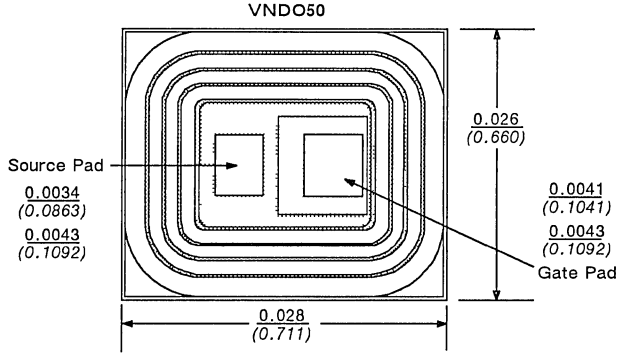
- Switching
- Spike Protection

FEATURES

- High Breakdown 450 V
- Available in Surface Mount Package SOT-23

TYPE	PACKAGE	DEVICE
Single	TO-92	• VN45350L VN50300L
	SOT-23	• VN45350T VN50300T
	Chip	• Available as above specifications

GEOMETRY DIAGRAM



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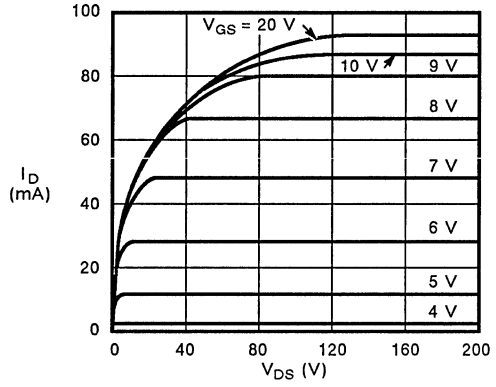
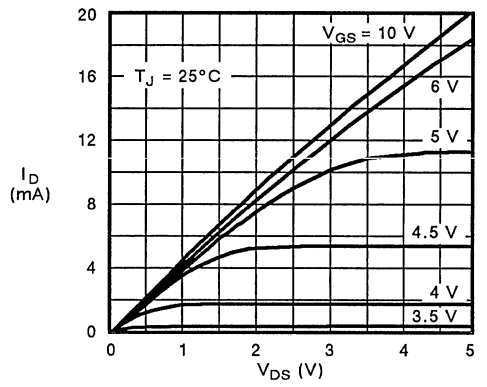
TYPICAL CHARACTERISTICS

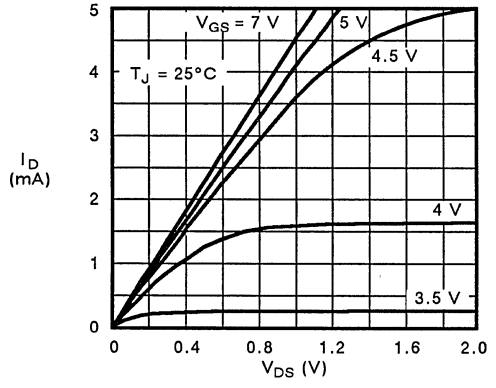
Output Characteristics



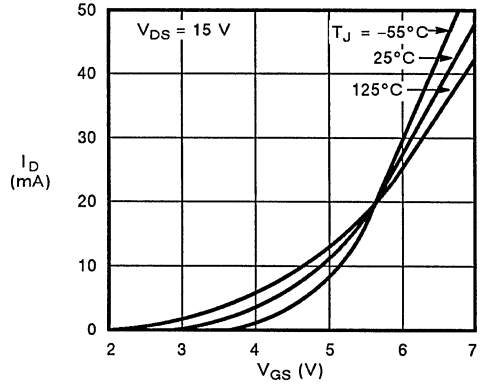
Ohmic Region Characteristics



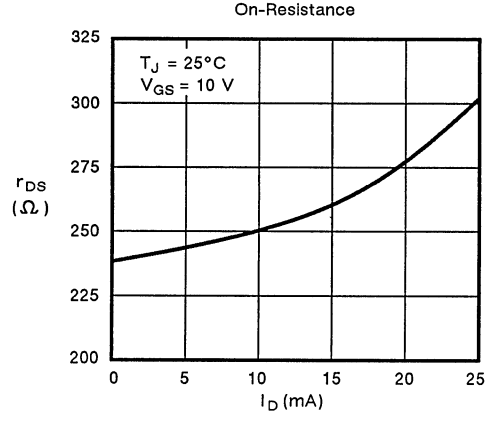
Output Characteristics for Low Gate Drive



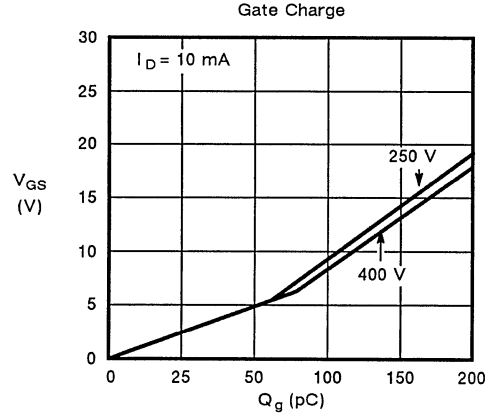
Transfer Characteristics



On-Resistance

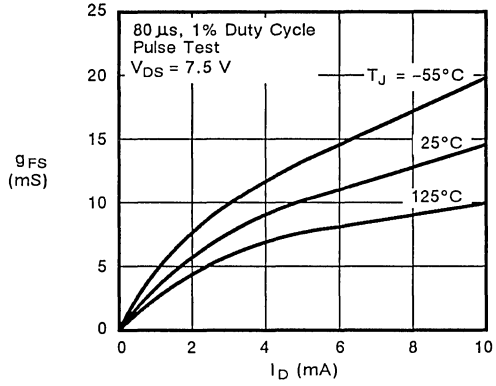


Gate Charge

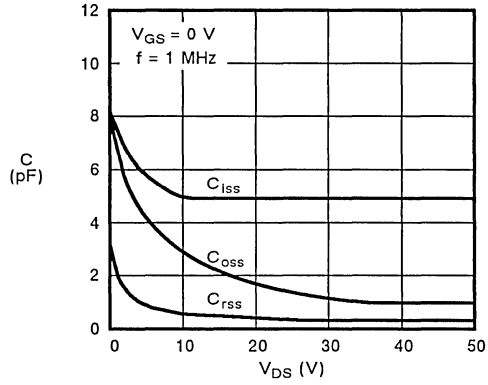


TYPICAL CHARACTERISTICS

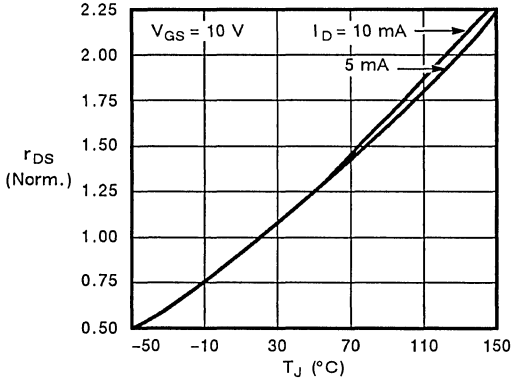
Transconductance



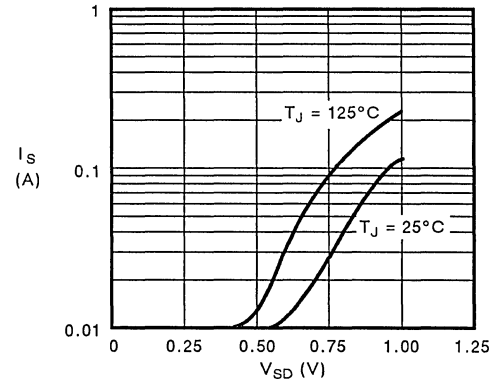
Capacitance



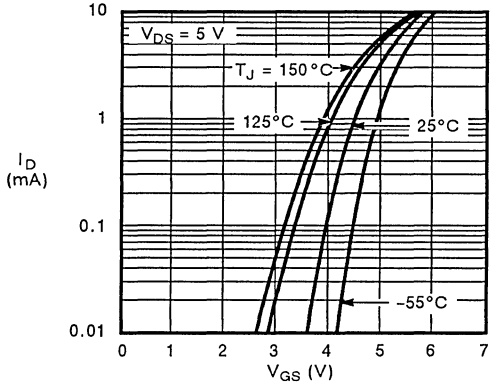
On-Resistance vs. Junction Temperature



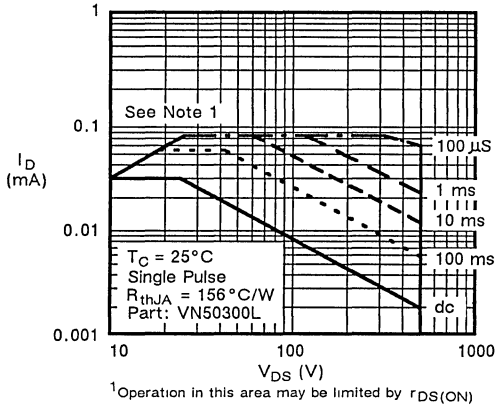
Source-Drain Diode Forward Voltage



Threshold Region



Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(ON)}$

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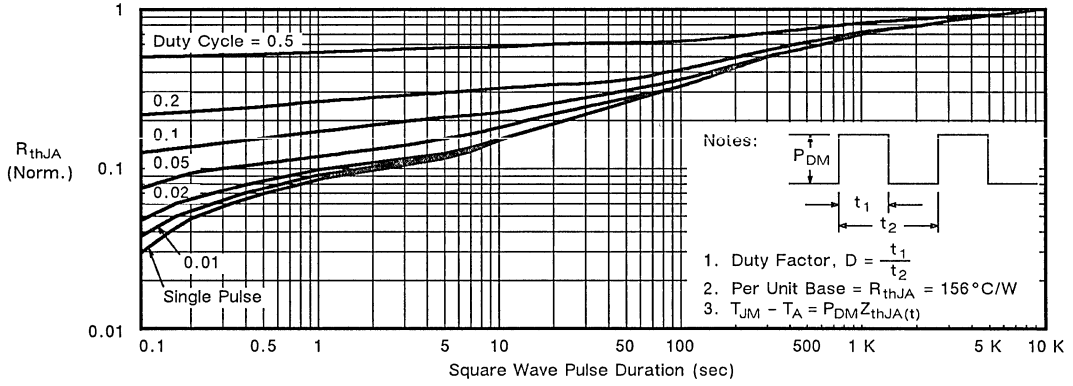
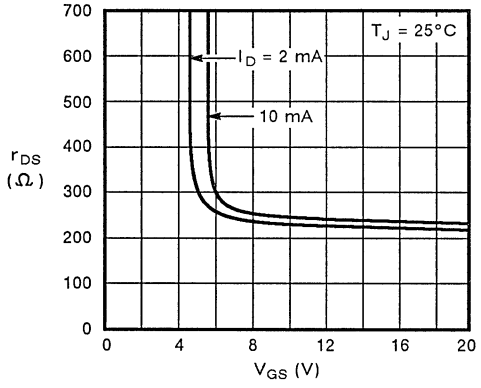
TYPICAL CHARACTERISTICS

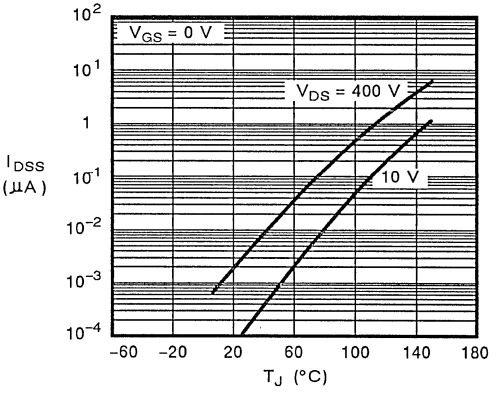
Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



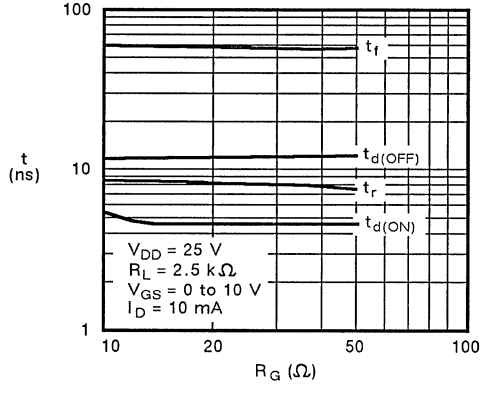
On-Resistance vs. Gate to Source Voltage



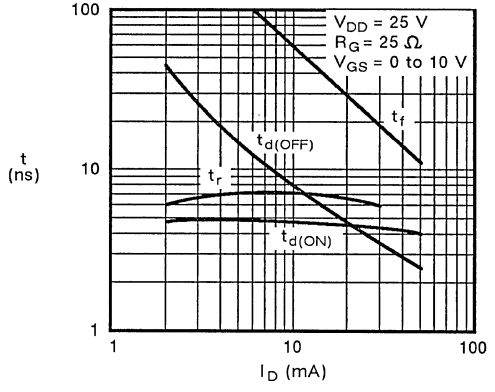
Off State Current



Drive Resistance Effects on Switching

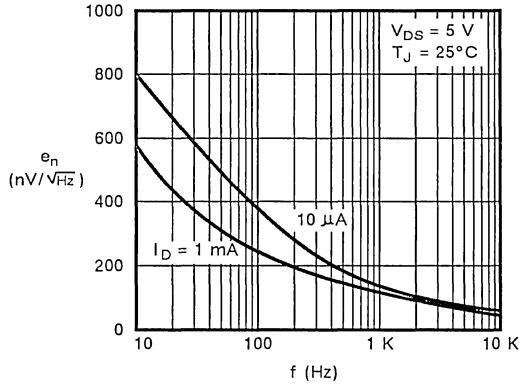


Load Condition Effects on Switching

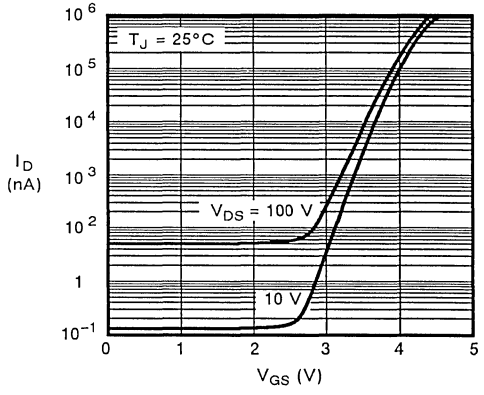


TYPICAL CHARACTERISTICS

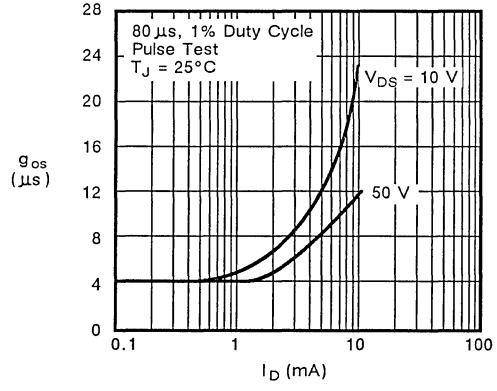
Equivalent Input Noise Voltage vs. Frequency



Body Drain Leakage Current



Output Conductance vs. Drain Current



7

VNDP06

Siliconix incorporated

N-Channel Enhancement-Mode MOSFET

DESIGNED FOR:

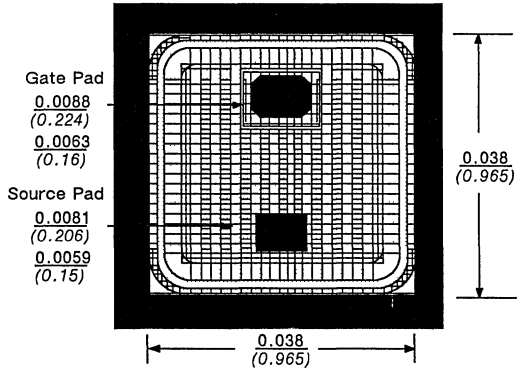
- Switching
- Amplification

FEATURES

- Protection Diode
- Low $r_{DS(on)} < 10\ \Omega$

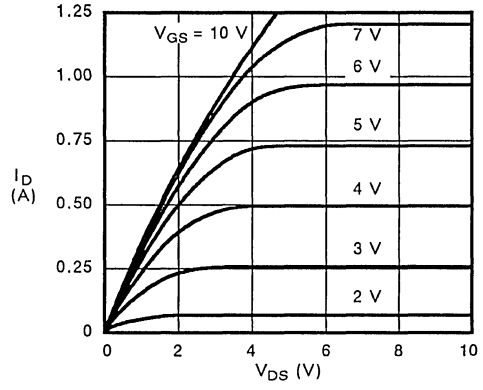
TYPE	PACKAGE	DEVICE
Single	TO-206AC	• VN10KE
	TO-92	• VN0610L, VN2222L
	TO-237	• VN10KM, VN2222KM
	Chip	• Available as above specifications

GEOMETRY DIAGRAM

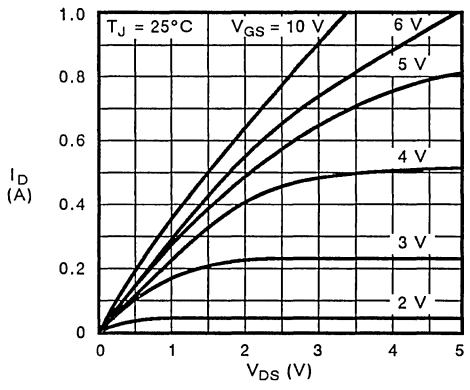


TYPICAL CHARACTERISTICS

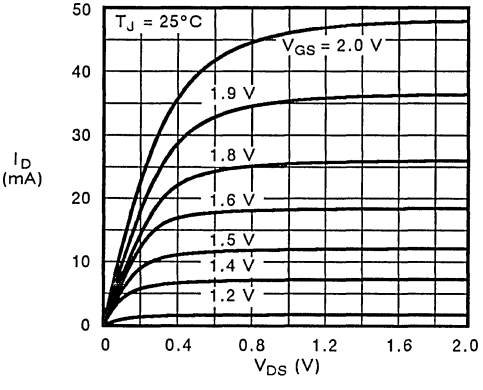
Output Characteristics



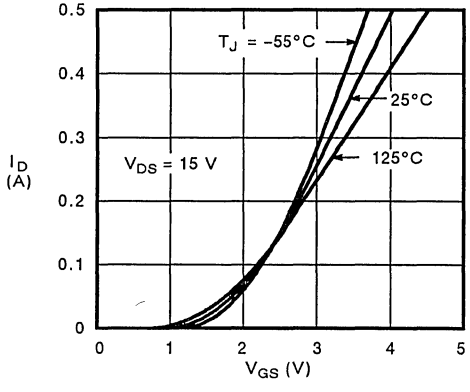
Ohmic Region Characteristics



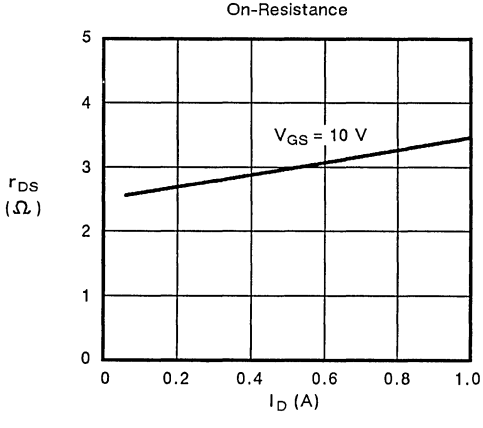
Output Characteristics for Low Gate Drive



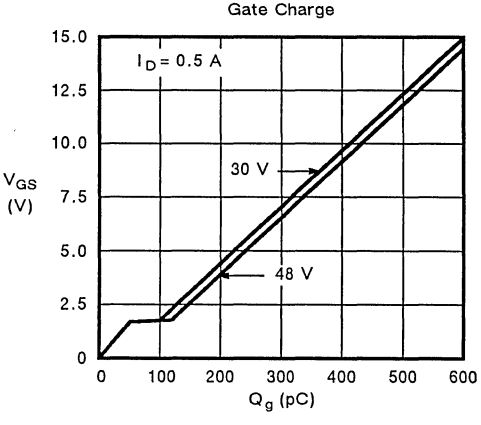
Transfer Characteristics



On-Resistance



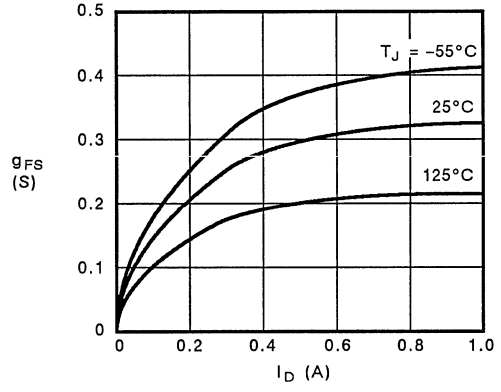
Gate Charge



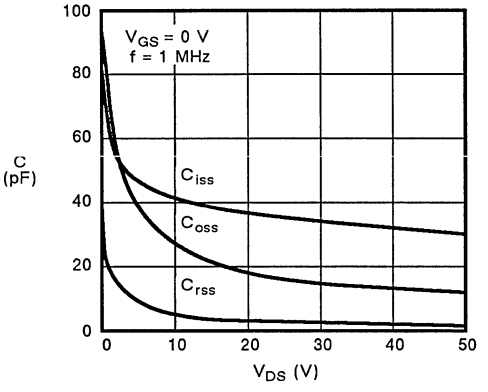
7

TYPICAL CHARACTERISTICS

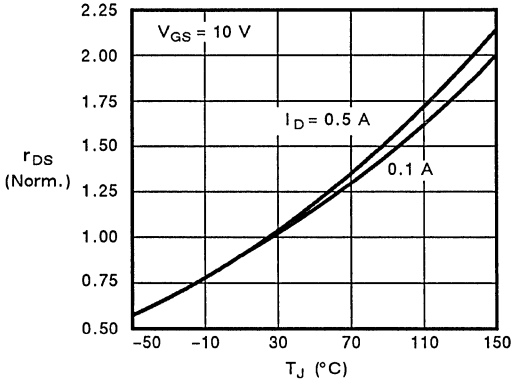
Transconductance



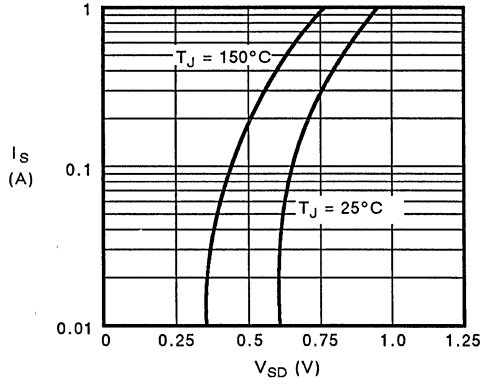
Capacitance



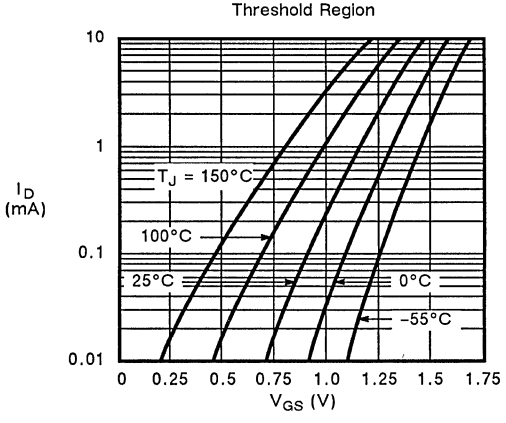
On-Resistance vs. Junction Temperature



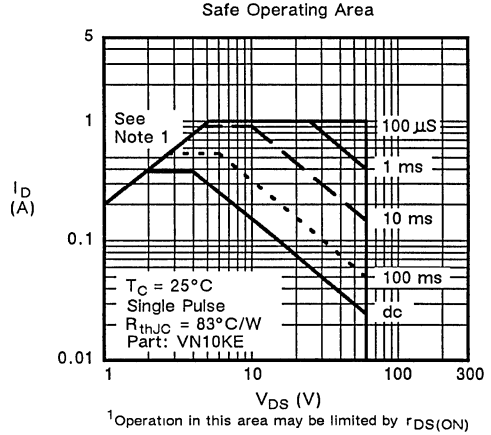
Source-Drain Diode Forward Voltage



Threshold Region



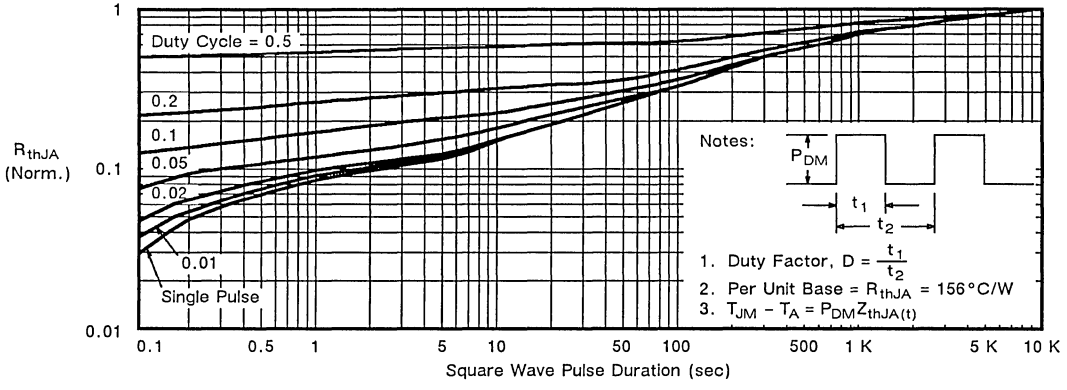
Safe Operating Area



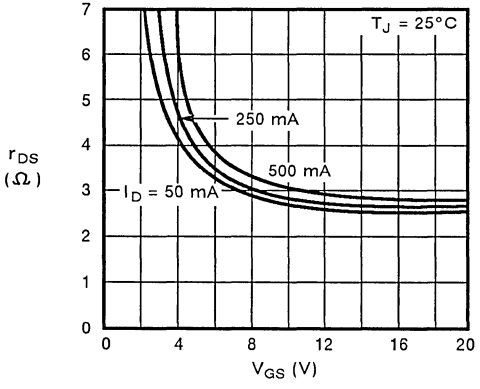
[1]Operation in this area may be limited by $r_{DS(ON)}$

TYPICAL CHARACTERISTICS

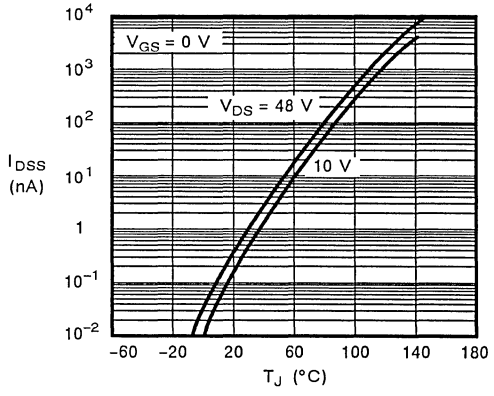
Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



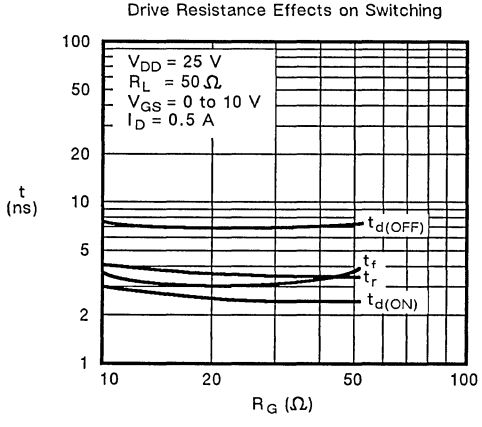
On-Resistance vs. Gate to Source Voltage



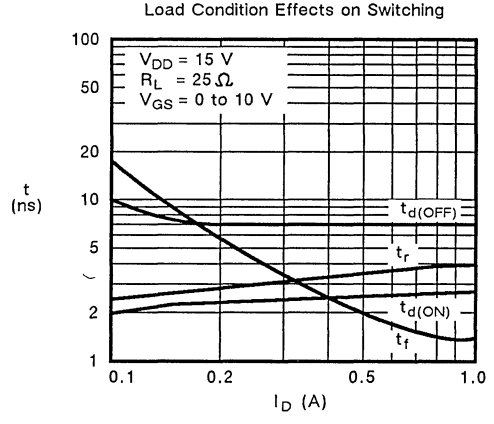
Off State Current



Drive Resistance Effects on Switching



Load Condition Effects on Switching



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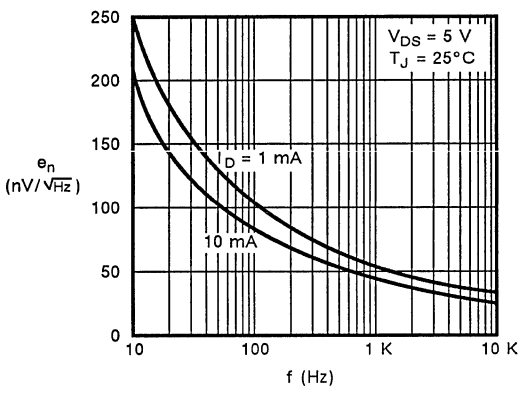
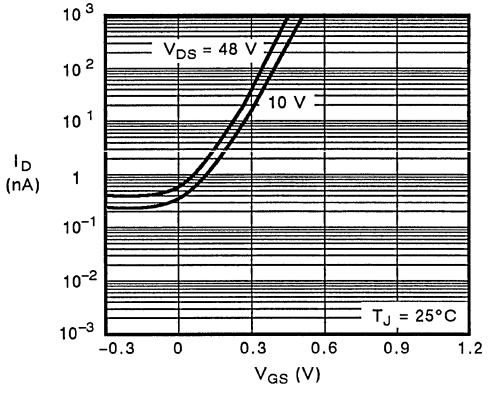
TYPICAL CHARACTERISTICS

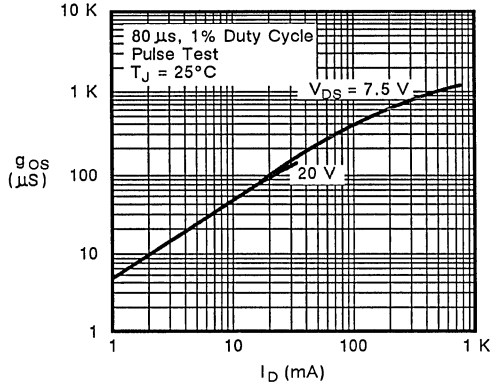
Equivalent Input Noise Voltage vs. Frequency



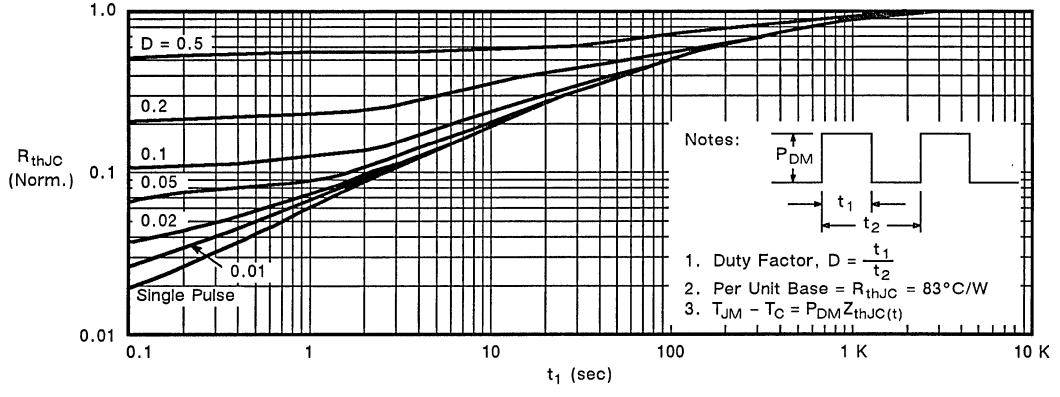
Body-Drain Leakage Current



Output Conductance vs. Drain Current



Transient Thermal Response (TO-206AC)



VNDQ03

N-Channel Enhancement-Mode MOSFET

DESIGNED FOR:

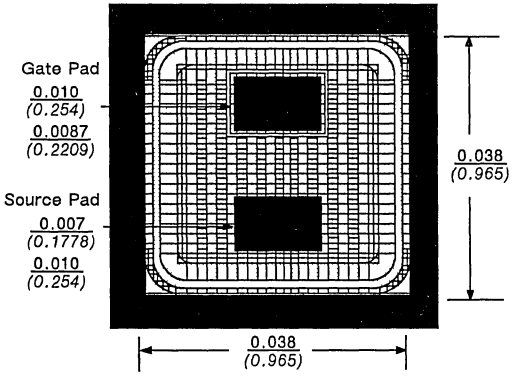
- Switching
- Amplification

FEATURES

- Low $r_{DS(on)} < 3\ \Omega$

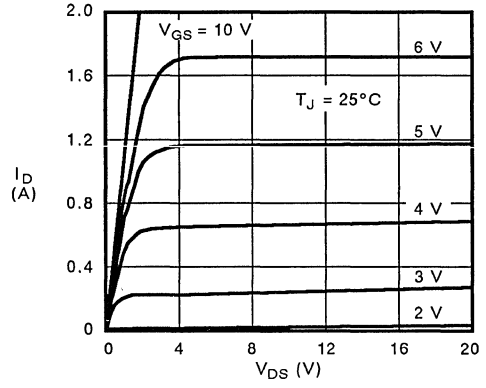
TYPE	PACKAGE	DEVICE
Single	TO-205AD	• VN0300B
	TO-92	• VN0300L
	TO-237	• VN0300M
Quad	14-Pin Plastic	• VQ1001J
	14-Pin Dual-In-Line	• VQ1001P
	Chip	• Available as above specifications

GEOMETRY DIAGRAM

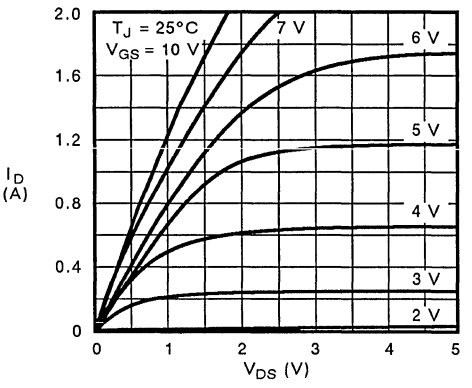


TYPICAL CHARACTERISTICS

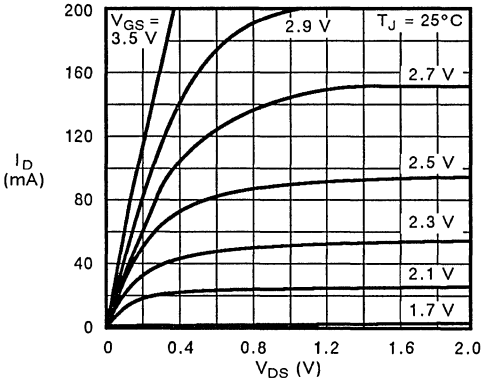
Output Characteristics



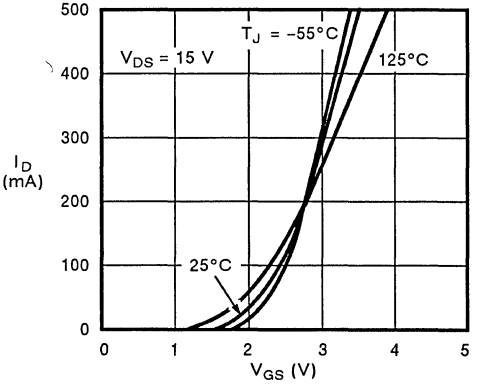
Ohmic Region Characteristics



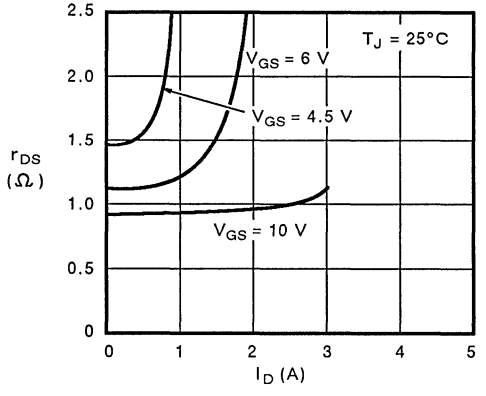
Output Characteristics for Low Gate Drive



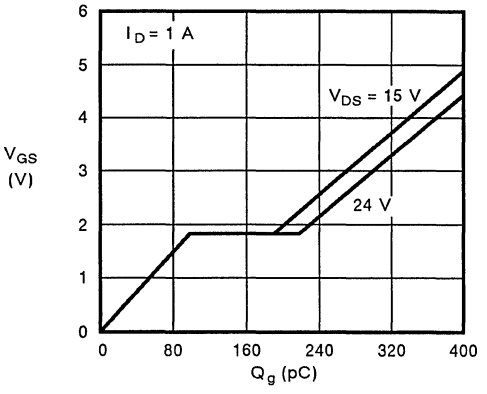
Transfer Characteristics



On-Resistance

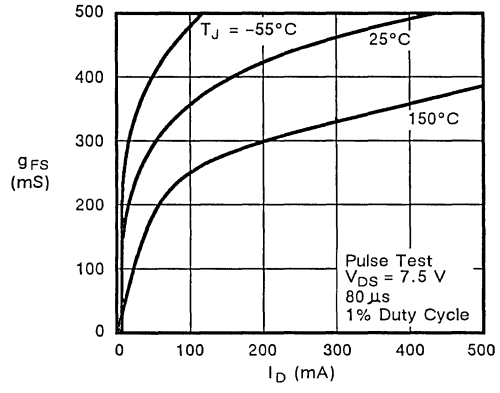


Gate Charge

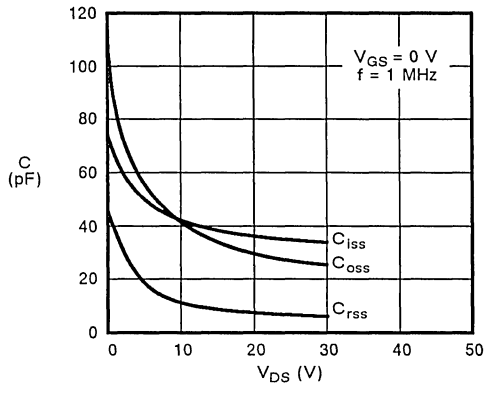


TYPICAL CHARACTERISTICS

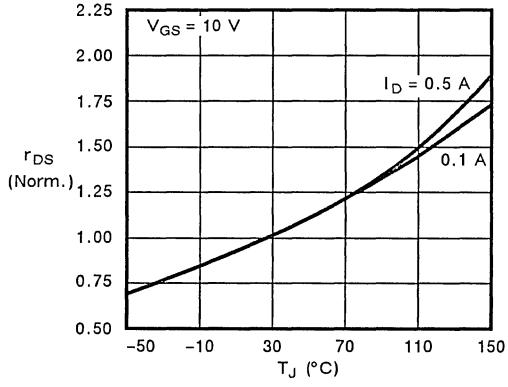
Transconductance



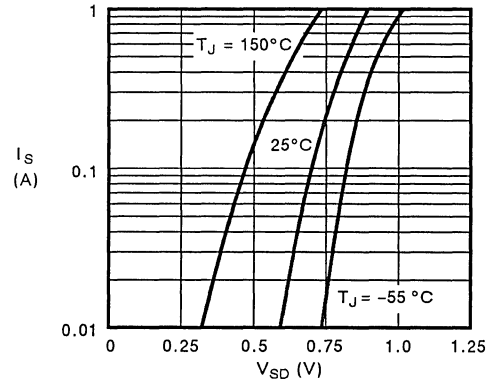
Capacitance



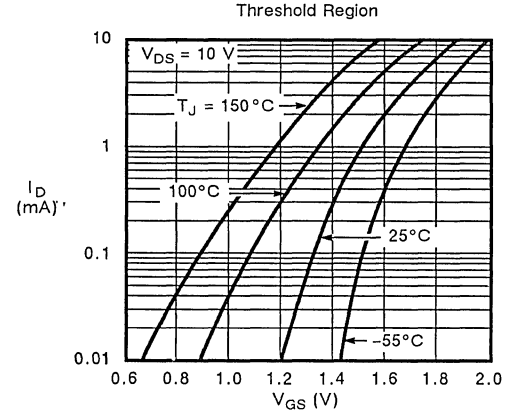
On-Resistance vs. Junction Temperature



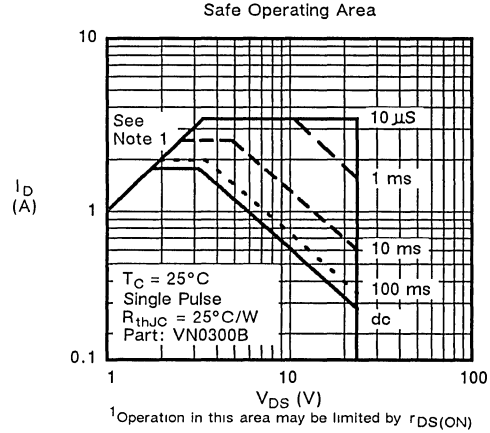
Source-Drain Diode Forward Voltage



Threshold Region



Safe Operating Area

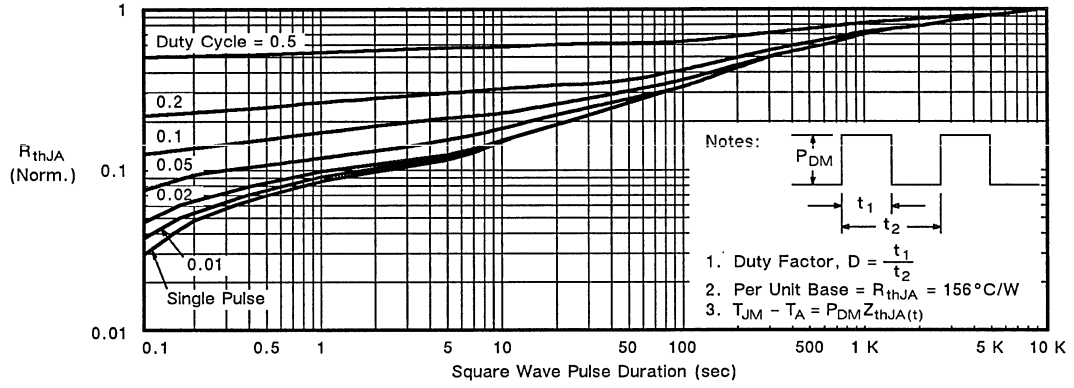


[1]Operation in this area may be limited by $r_{DS(ON)}$

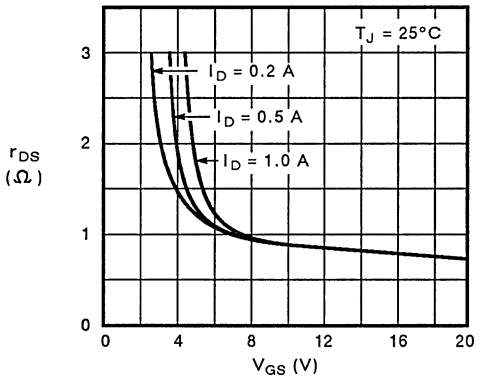
7

TYPICAL CHARACTERISTICS

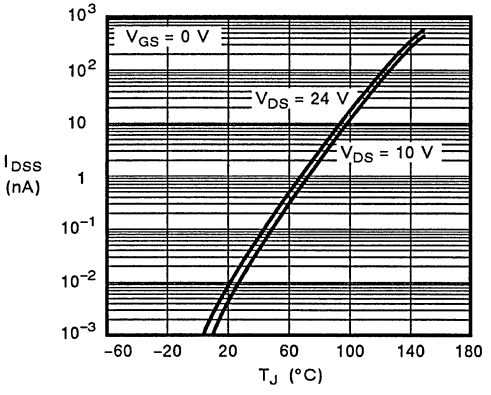
Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



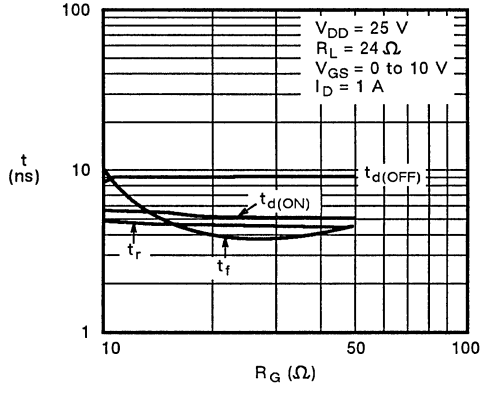
On-Resistance vs. Gate to Source Voltage



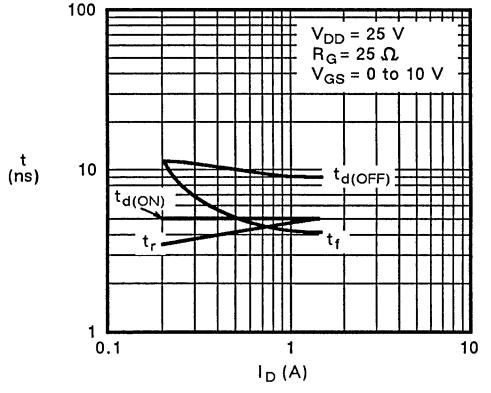
Off-State Current



Drive Resistance Effects on Switching

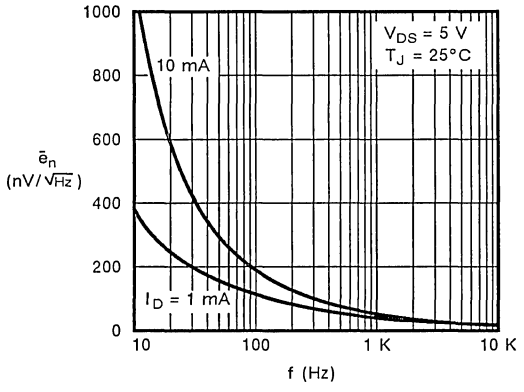


Load Condition Effects on Switching

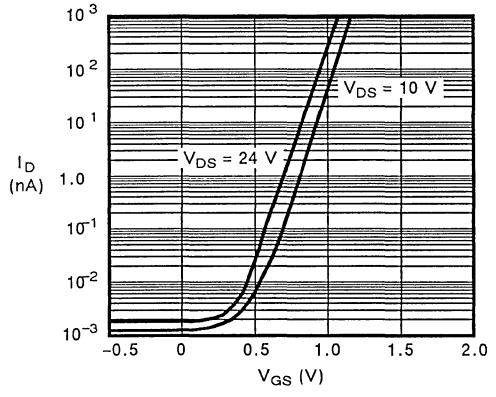


TYPICAL CHARACTERISTICS

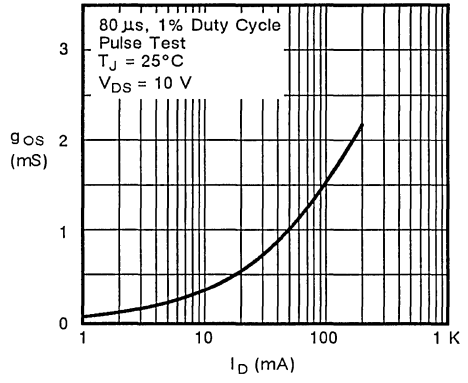
Equivalent Input Noise Voltage vs. Frequency



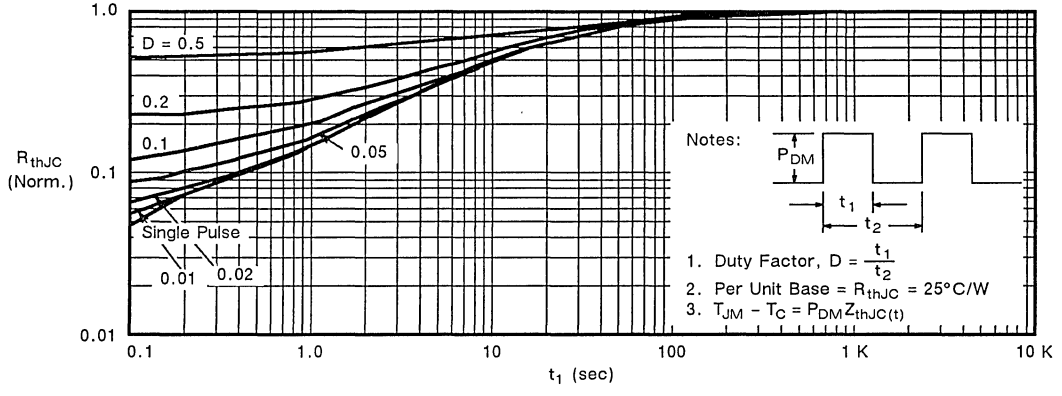
Body-Drain Leakage Current



Output Conductance vs. Drain Current



Transient Thermal Response (TO-205AD)



7

VNDQ06

Siliconix incorporated

N-Channel Enhancement-Mode MOSFET

DESIGNED FOR:

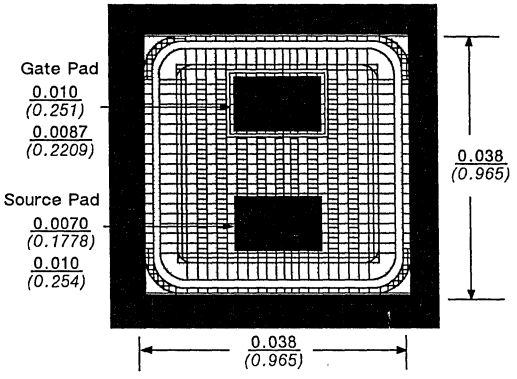
- Switching
- Amplification

FEATURES

- Low $r_{DS(on)}$ < 3.5 Ω

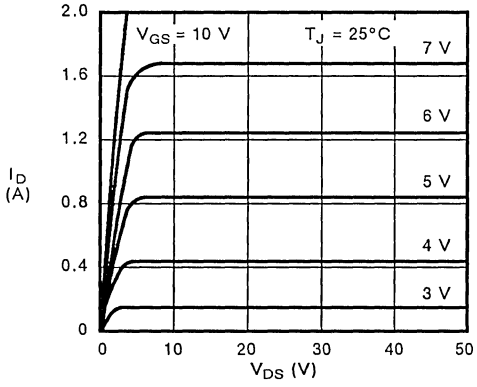
TYPE	PACKAGE	DEVICE
Single	TO-205AD	• 2N6659, 2N6660 VN67AB
	TO-220SD	• VN40AFD, VN46AFD, VN66AFD, VN67AFD
	TO-220	• VN66AD, VN67AD
Quad	14-Pin Plastic	• VQ1004J
	14-Pin Dual-In-Line	• VQ1004P
	Chip	• Available as above specifications

GEOMETRY DIAGRAM

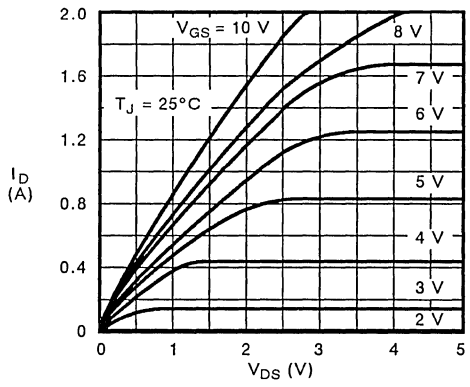


TYPICAL CHARACTERISTICS

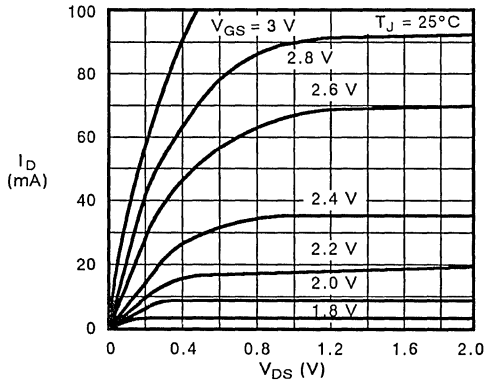
Output Characteristics



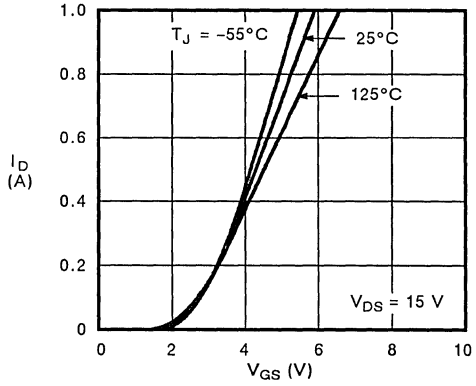
Ohmic Region Characteristics



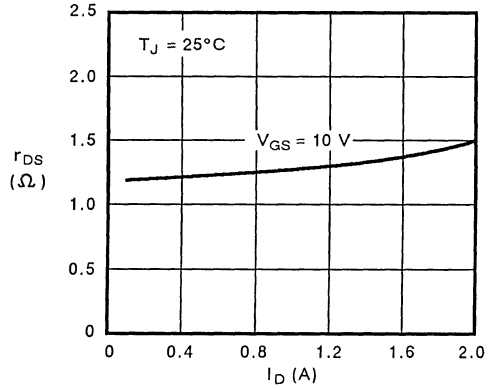
Output Characteristics for Low Gate Drive



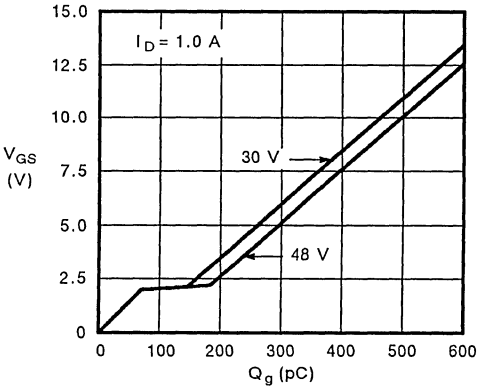
Transfer Characteristics



On-Resistance



Gate Charge



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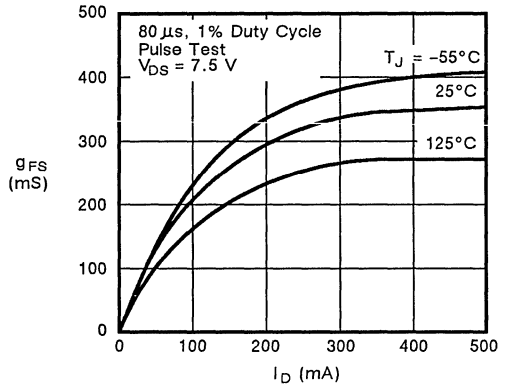
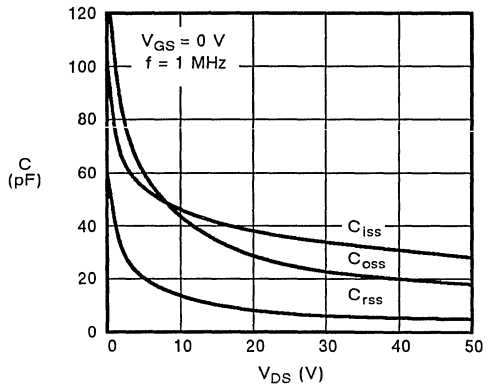
TYPICAL CHARACTERISTICS

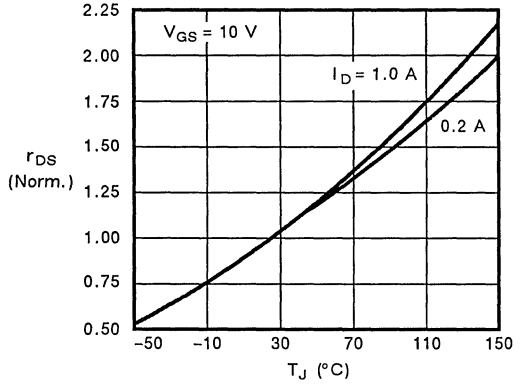
Transconductance



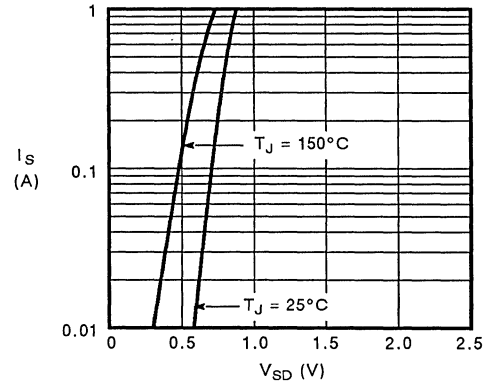
Capacitance



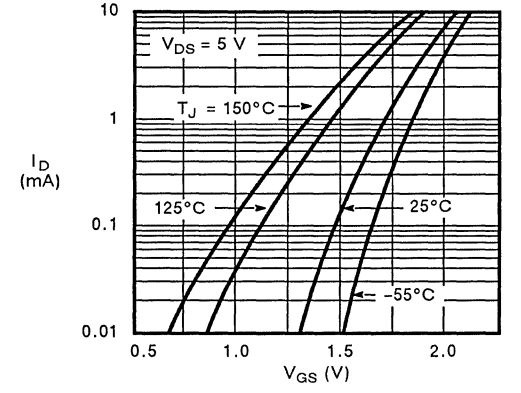
On-Resistance vs. Junction Temperature



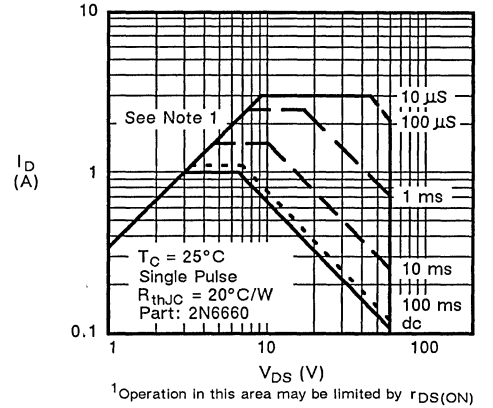
Source-Drain Diode Forward Voltage



Threshold Region



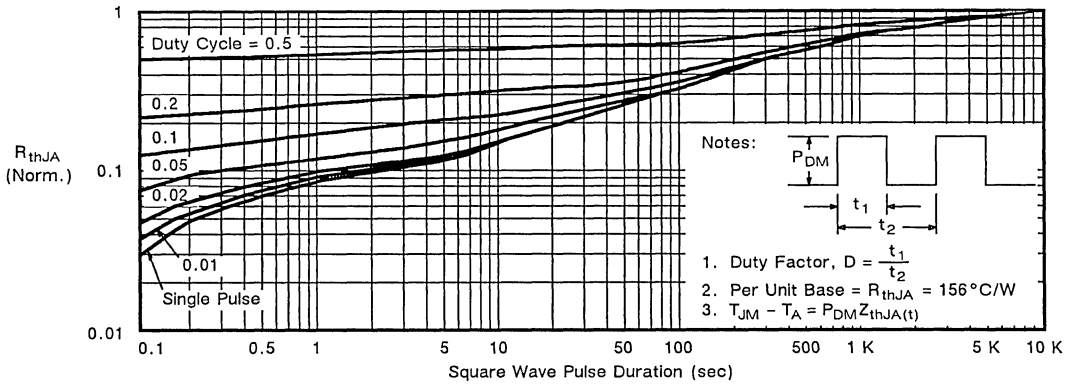
Safe Operating Area



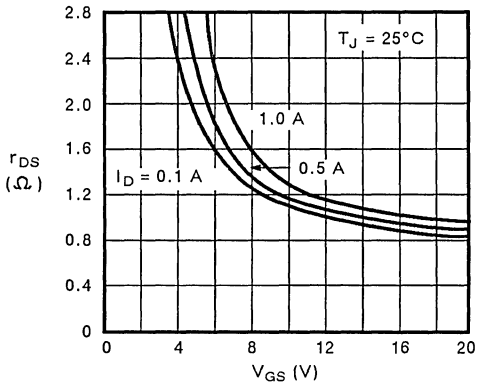
[1]Operation in this area may be limited by $r_{DS(ON)}$

TYPICAL CHARACTERISTICS

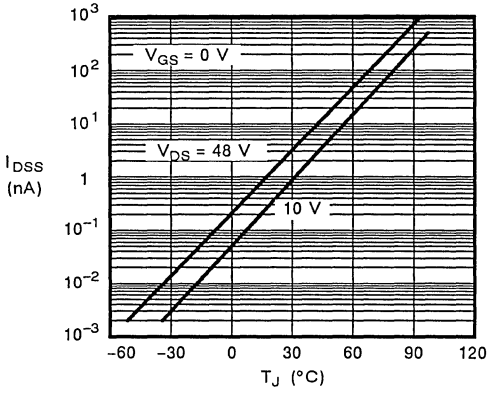
Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



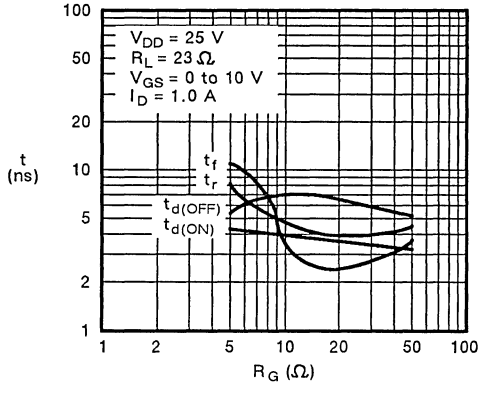
On-Resistance vs. Gate to Source Voltage



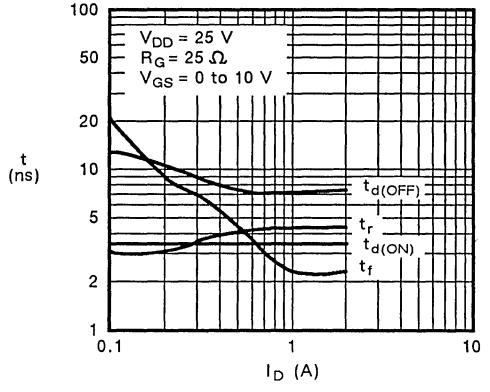
Off State Current



Drive Resistance Effects on Switching



Load Condition Effects on Switching



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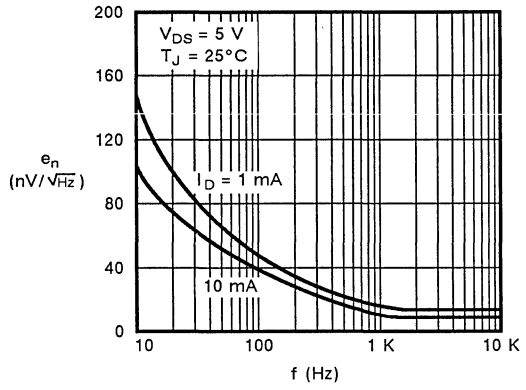
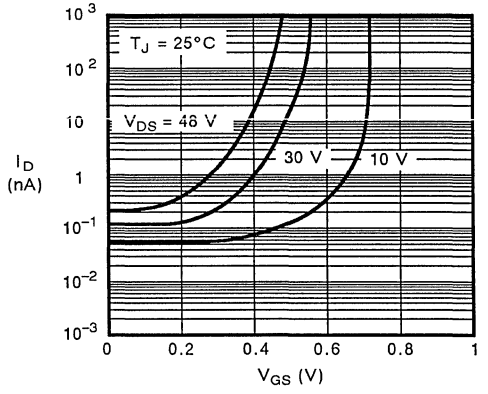
TYPICAL CHARACTERISTICS

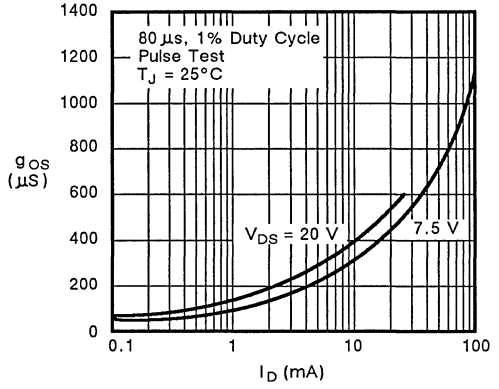
Equivalent Input Noise Voltage vs. Frequency



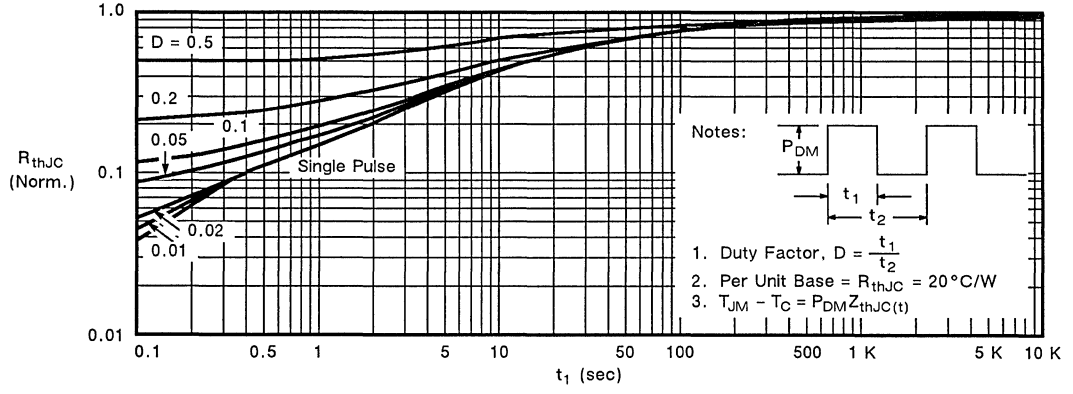
Body-Drain Leakage Current



Output Conductance vs. Drain Current



Transient Thermal Response (TO-205AD)



VNDQ09

N-Channel Enhancement-Mode MOSFET

DESIGNED FOR:

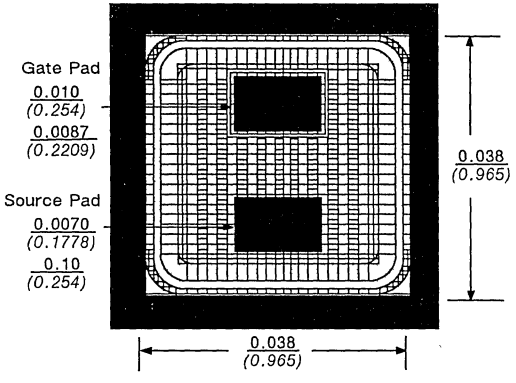
- Switching
- Amplification

FEATURES

- Low $r_{DS(on)} < 4\ \Omega$

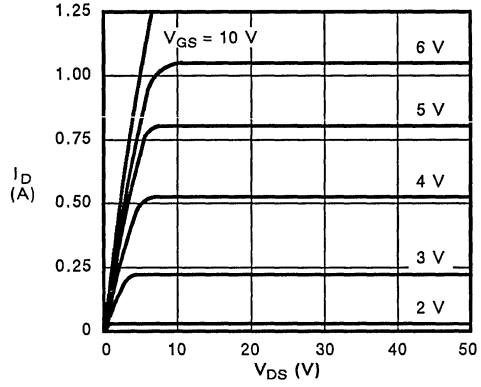
TYPE	PACKAGE	DEVICE
Single	TO-205AD	• VN90AB 2N6661
	TO-92	• VN0808L
	TO-237	• VN0808M
	TO-220SD	• VN88AFD
	TO-220	• VN88AD
Quad	14-Pin Plastic	• VQ1006J
	14-Pin Dual-In-Line	• VQ1004P

GEOMETRY DIAGRAM

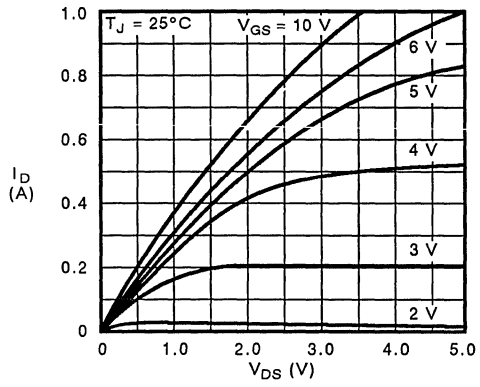


TYPICAL CHARACTERISTICS

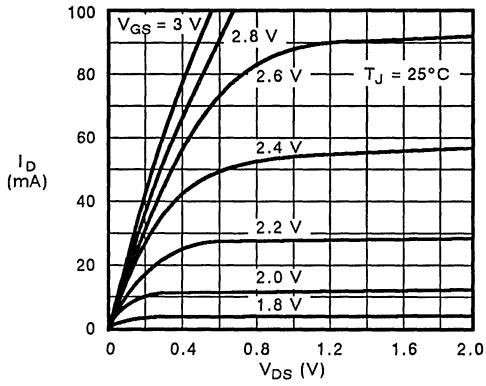
Output Characteristics



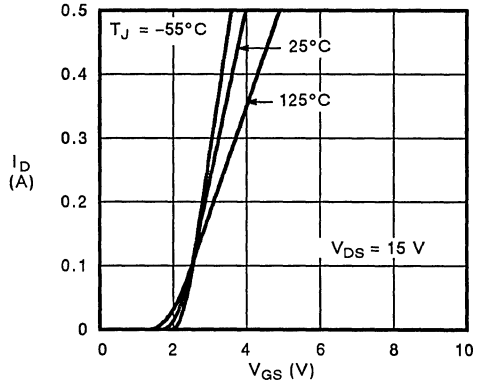
Ohmic Region Characteristics



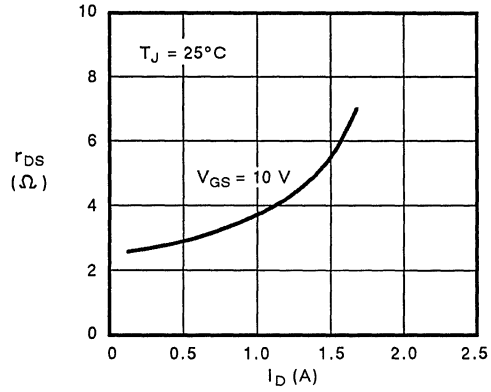
Output Characteristics for Low Gate Drive



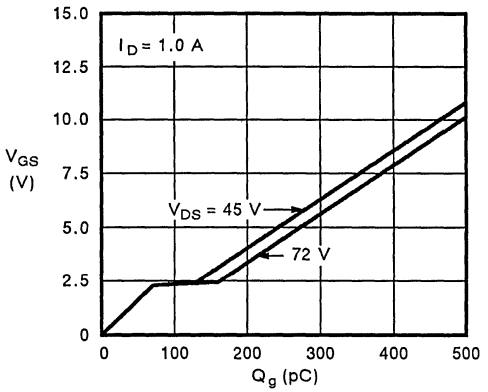
Transfer Characteristics



On-Resistance

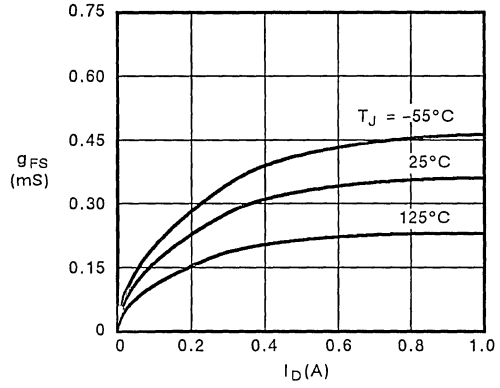


Gate Charge

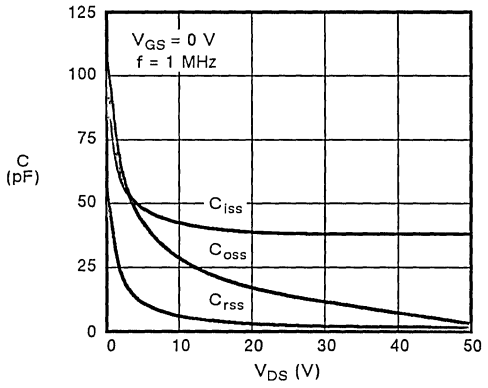


TYPICAL CHARACTERISTICS

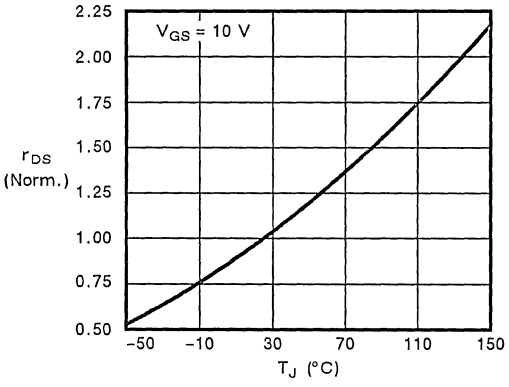
Transconductance



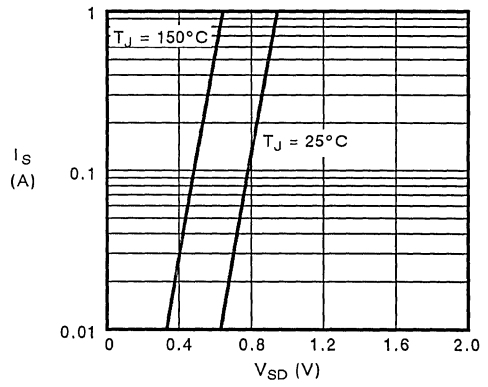
Capacitance



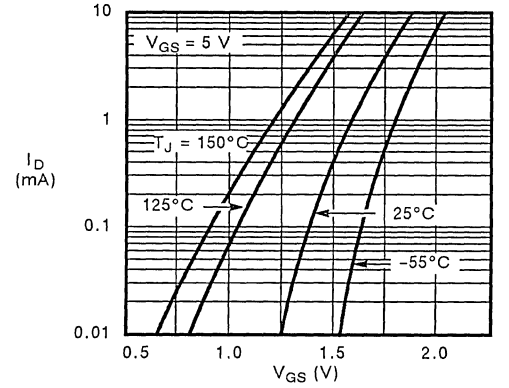
On-Resistance vs. Junction Temperature



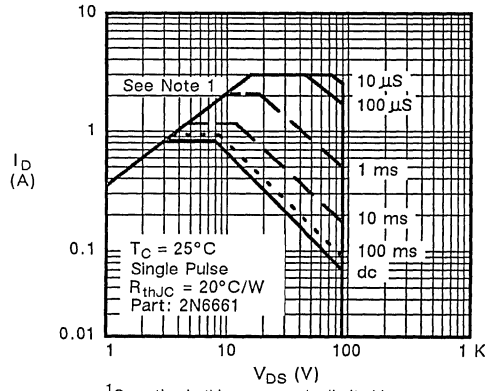
Source-Drain Diode Forward Voltage



Threshold Region



Safe Operating Area

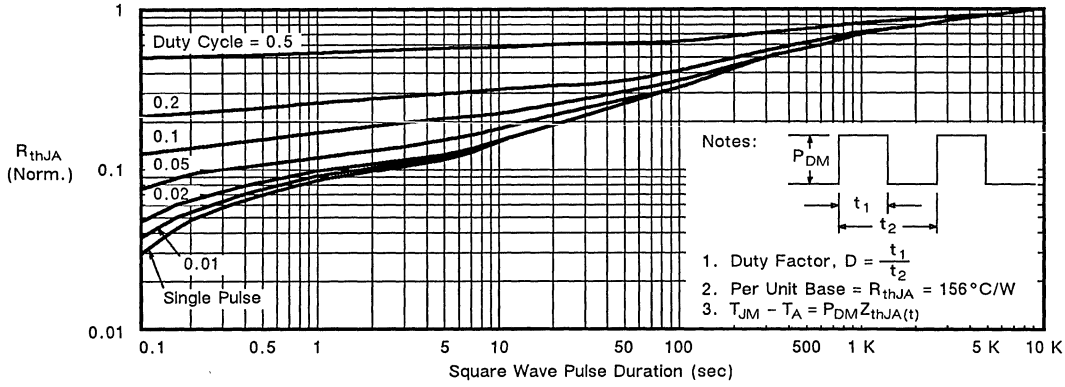


[1]Operation in this area may be limited by $r_{DS(ON)}$

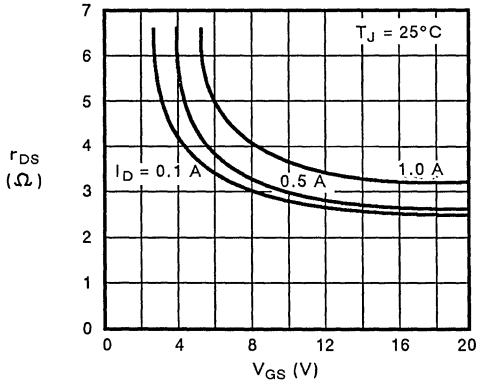
7

TYPICAL CHARACTERISTICS

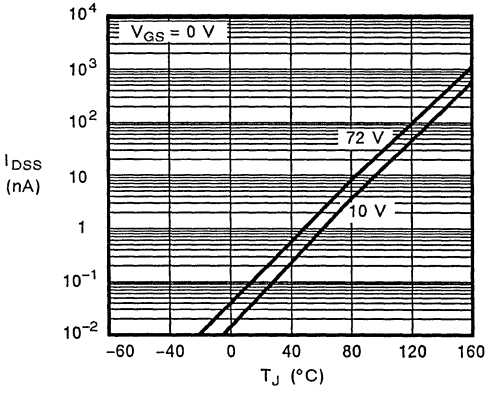
Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



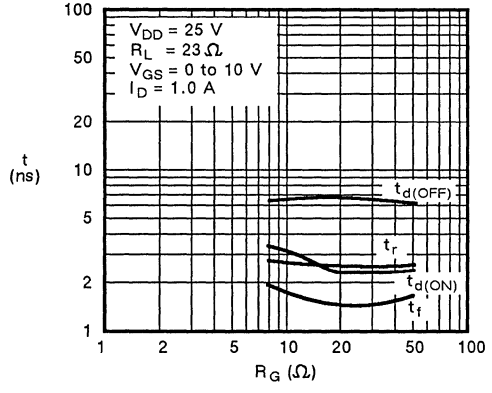
On-Resistance vs. Gate to Source Voltage



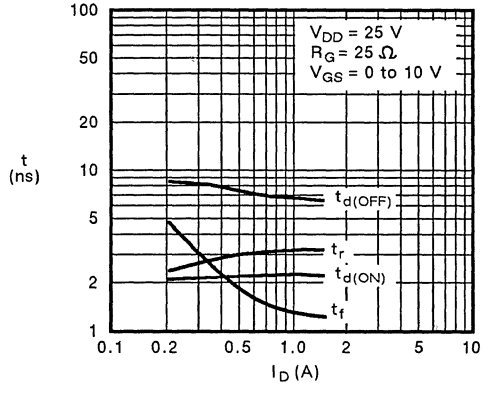
Off State Current



Drive Resistance Effects on Switching

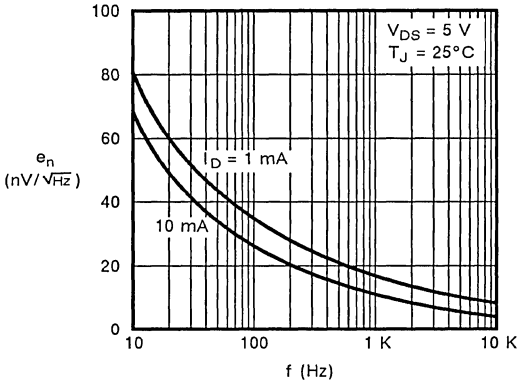


Load Condition Effects on Switching

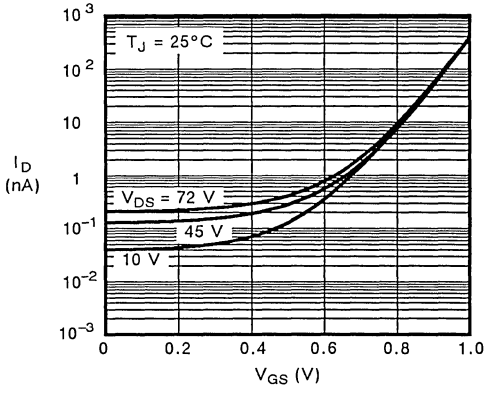


TYPICAL CHARACTERISTICS

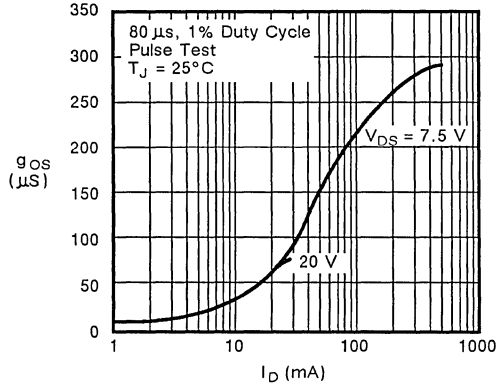
Equivalent Input Noise Voltage vs. Frequency



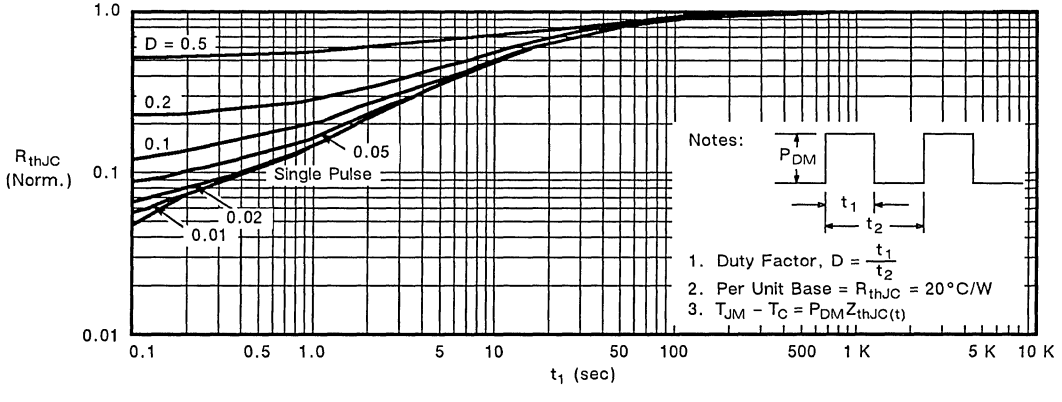
Body Drain Leakage Current



Output Conductance vs. Drain Current



Transient Thermal Response (TO-205AD)



7

VNDQ12

Siliconix incorporated

N-Channel Enhancement-Mode MOSFET

DESIGNED FOR:

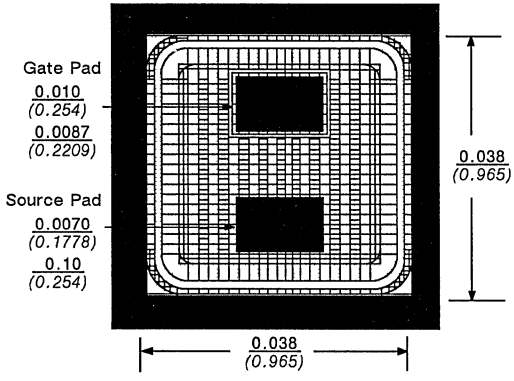
- Switching
- Amplification

FEATURES

- Low $r_{DS(on)} < 4.5\ \Omega$

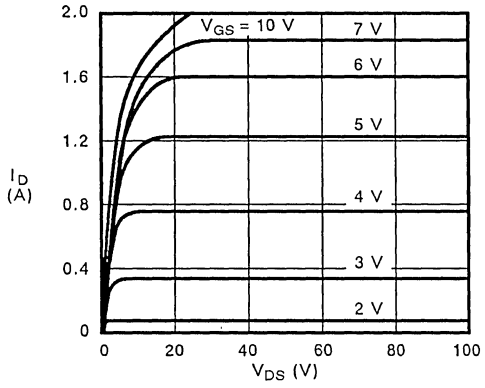
TYPE	PACKAGE	DEVICE
Single	TO-205AD	• VN1206B
	TO-220	• VN1206D
	TO-237	• VN1206M, VN1210M
	TO-92	• VN1206L, VN1210L
	Chip	• Available as above specifications

GEOMETRY DIAGRAM

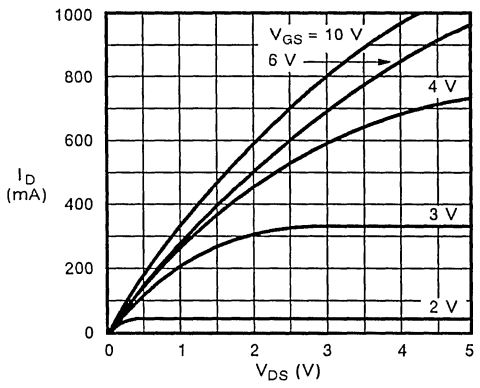


TYPICAL CHARACTERISTICS

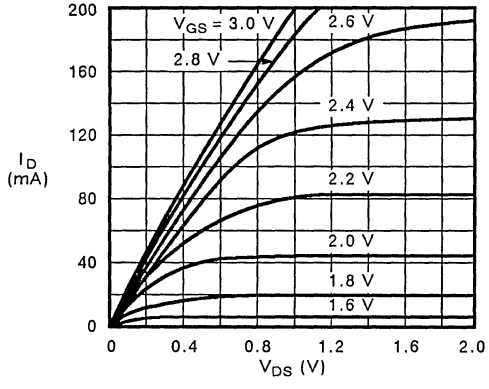
Output Characteristics



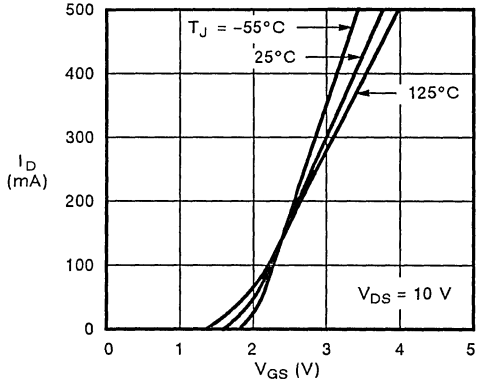
Ohmic Region Characteristics



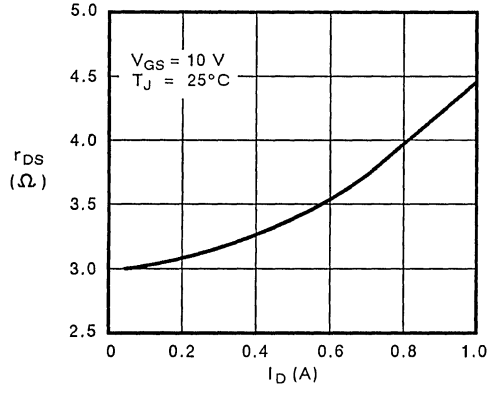
Output Characteristics for Low Gate Drive



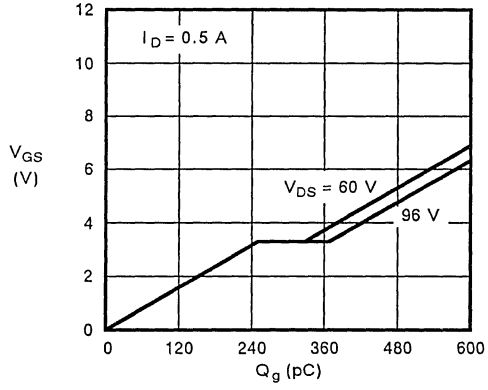
Transfer Characteristics



On-Resistance



Gate Charge



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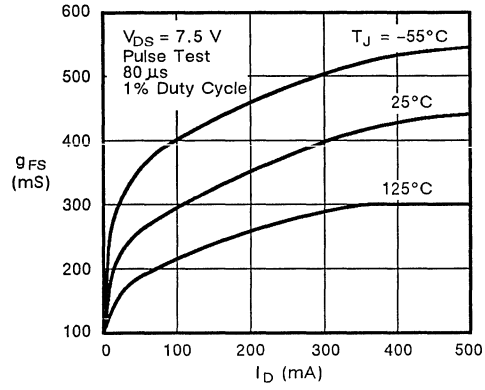
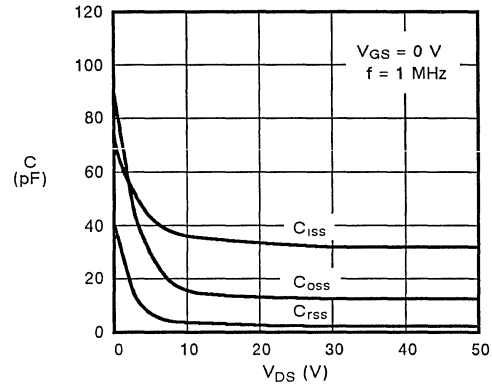
TYPICAL CHARACTERISTICS

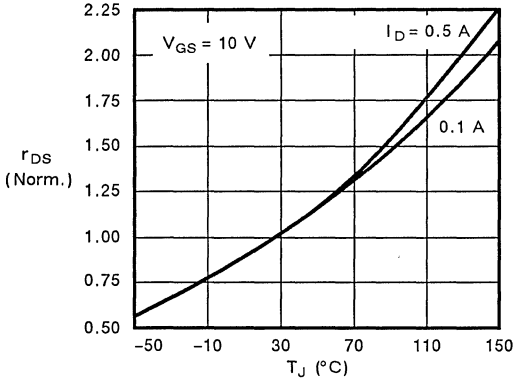
Transconductance



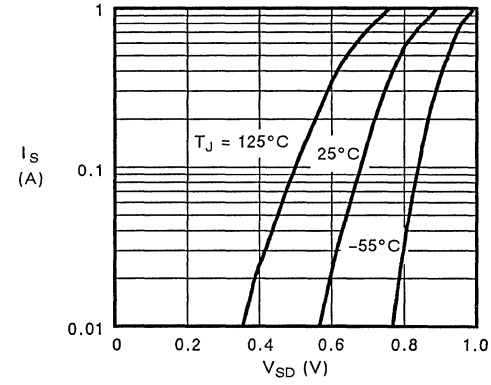
Capacitance



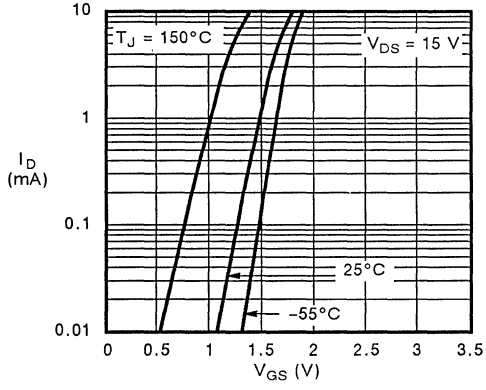
On-Resistance vs. Junction Temperature



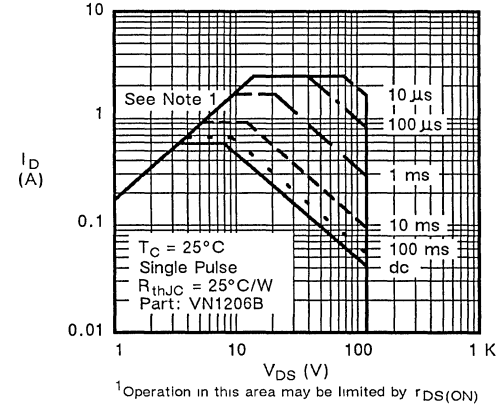
Source-Drain Diode Forward Voltage



Threshold Region



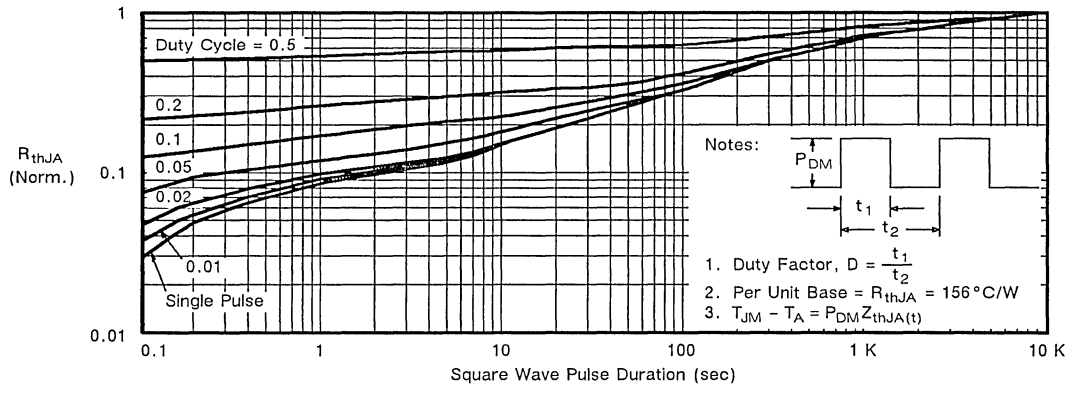
Safe Operating Area



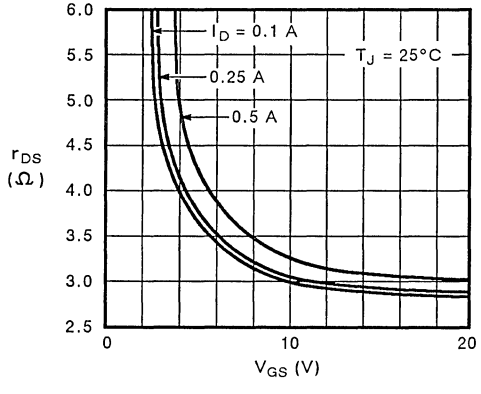
[1]Operation in this area may be limited by $r_{DS(ON)}$

TYPICAL CHARACTERISTICS

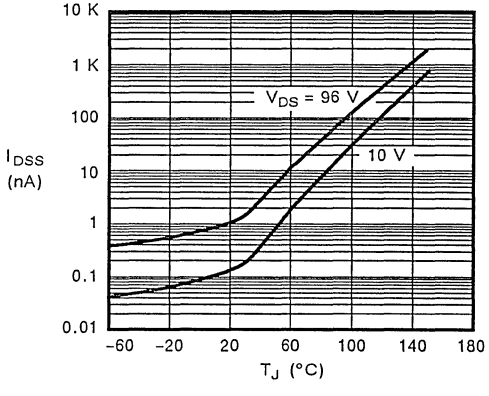
Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



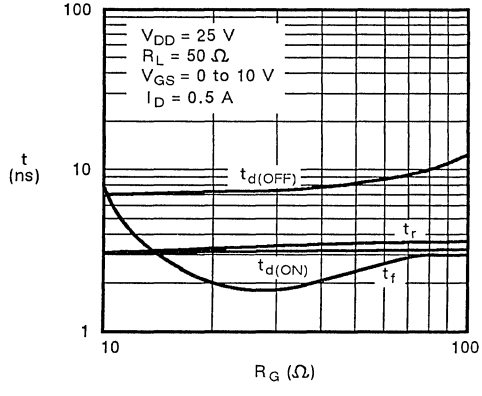
On-Resistance vs. Gate to Source Voltage



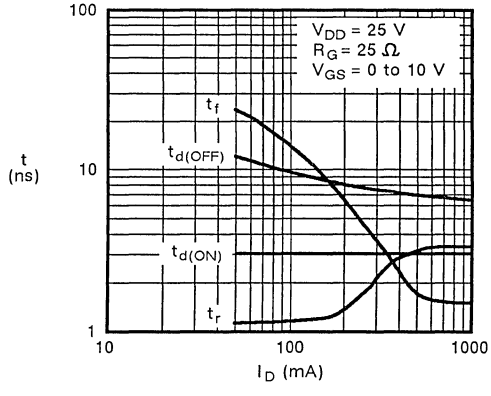
Off State Current



Drive Resistance Effects on Switching



Load Condition Effects on Switching



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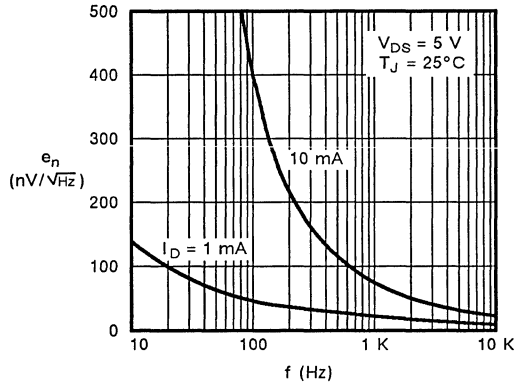
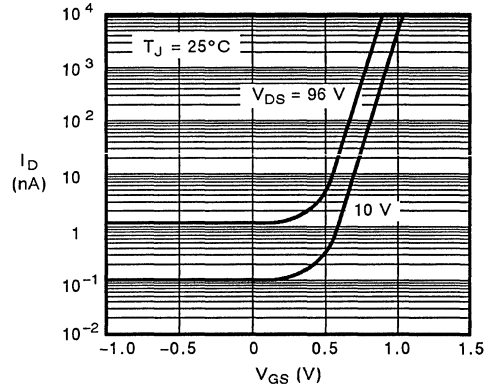
TYPICAL CHARACTERISTICS

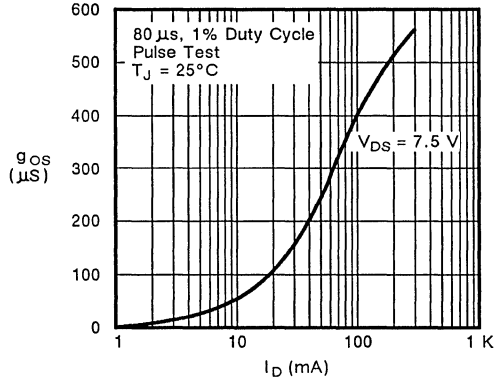
Equivalent Input Noise Voltage vs. Frequency



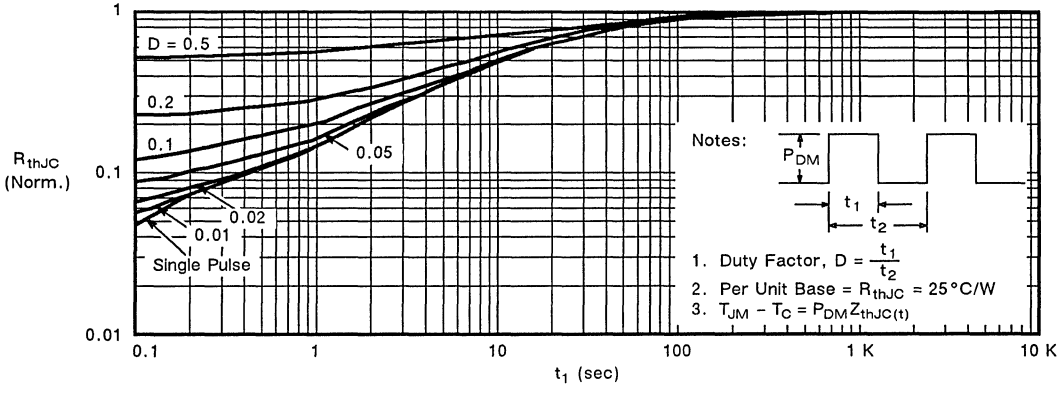
Body Drain Leakage Current



Output Conductance vs. Drain Current



Transient Thermal Response (TO-205AD)



VNDQ20

N-Channel Enhancement-Mode MOSFET

DESIGNED FOR:

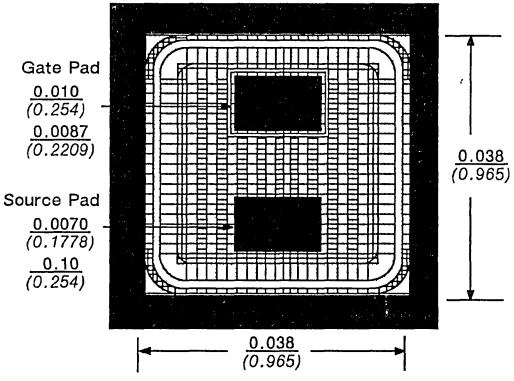
- Switching
- Amplification

FEATURES

- High Breakdown > 200 V
- Low $r_{DS(on)}$ < 10 Ω

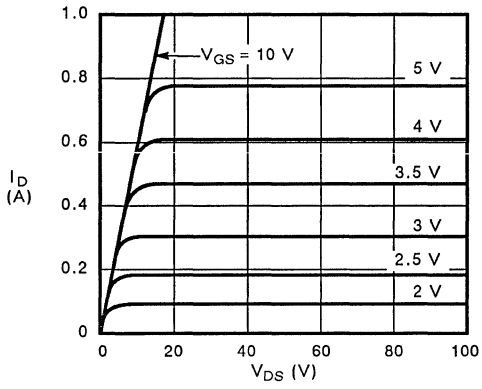
TYPE	PACKAGE	DEVICE
Single	TO-92	• BS107 VN2010L, VN2020L
	Chip	• Available as above specifications

GEOMETRY DIAGRAM

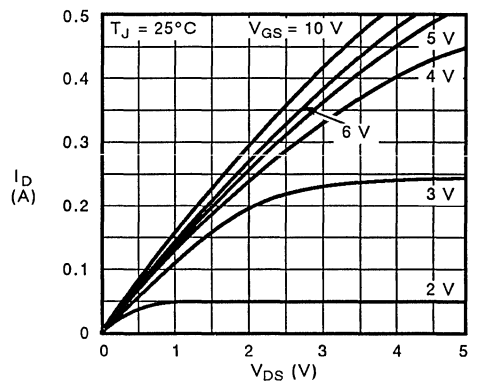


TYPICAL CHARACTERISTICS

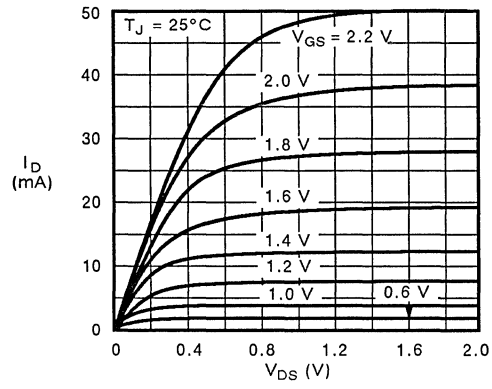
Output Characteristics



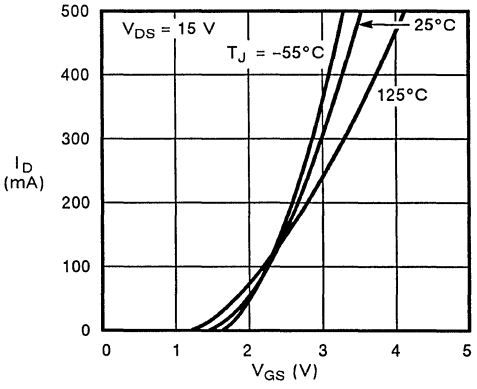
Ohmic Region Characteristics



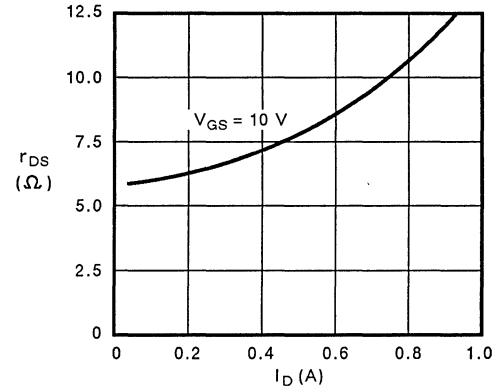
Output Characteristics for Low Gate Drive



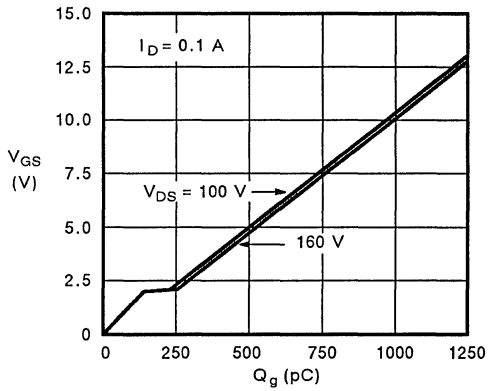
Transfer Characteristics



On-Resistance

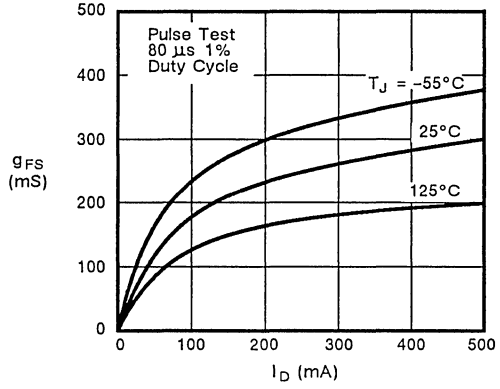


Gate Charge

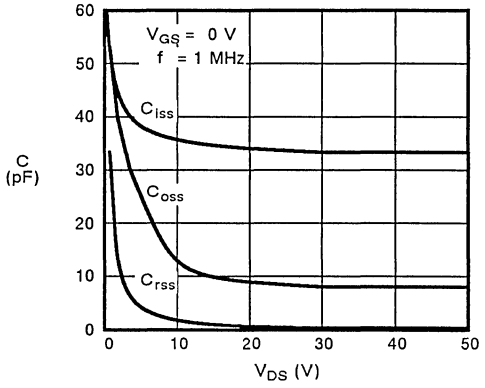


TYPICAL CHARACTERISTICS

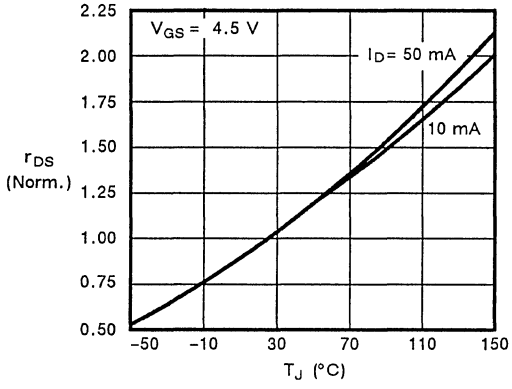
Transconductance



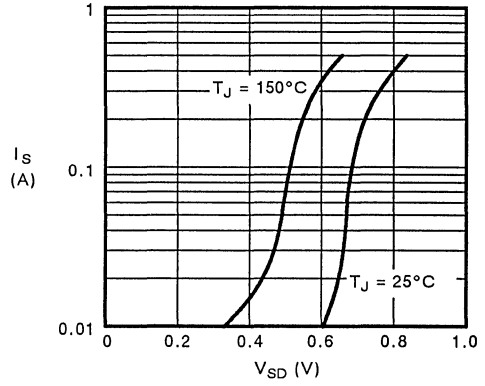
Capacitance



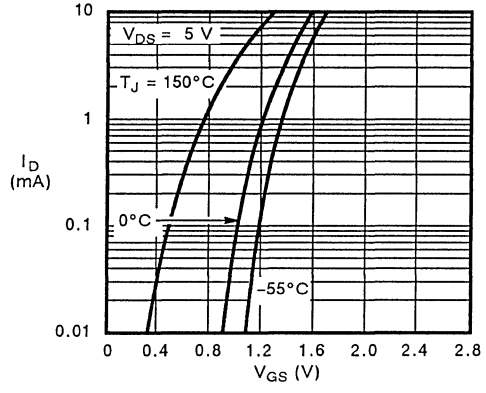
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



Threshold Region



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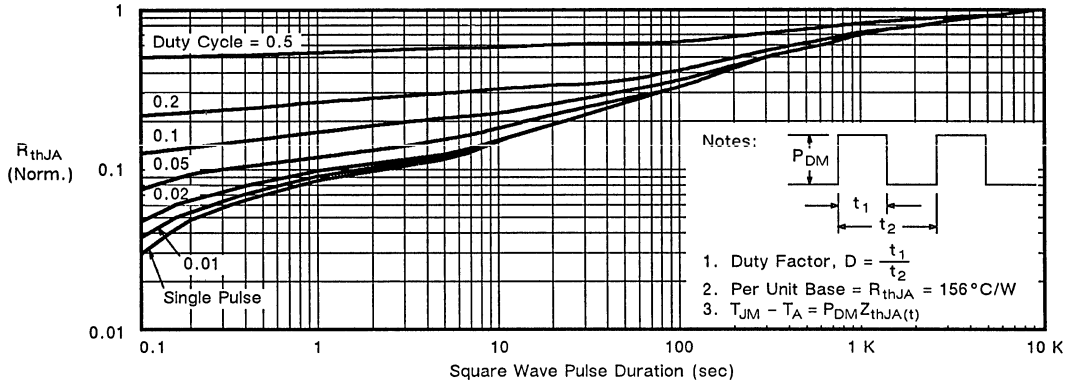
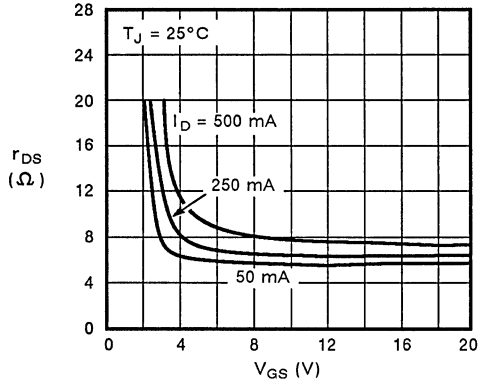
TYPICAL CHARACTERISTICS

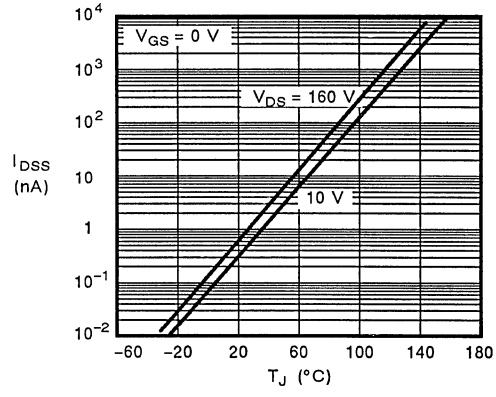
Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



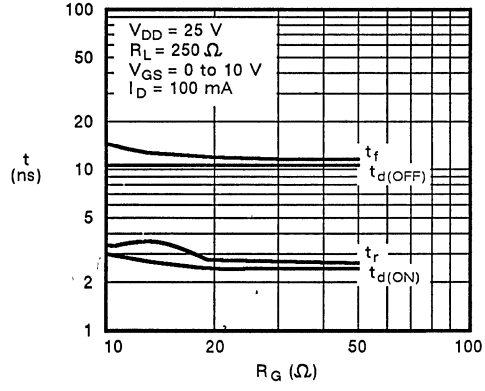
On-Resistance vs. Gate to Source Voltage



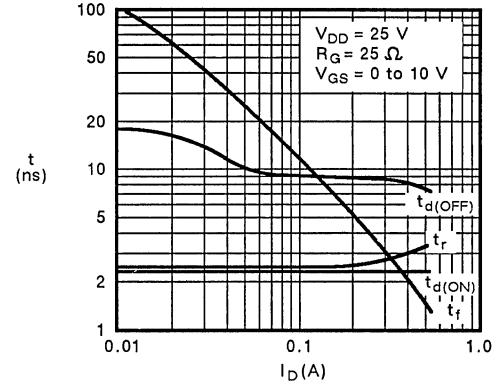
Off State Current



Drive Resistance Effects on Switching

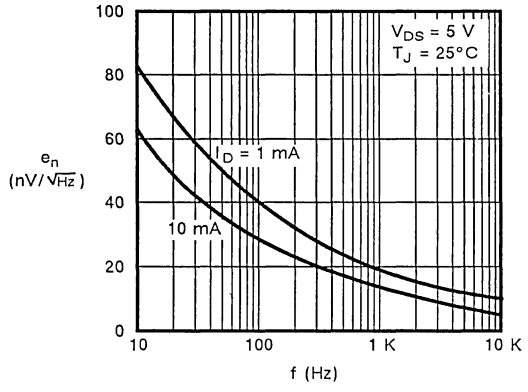


Load Condition Effects on Switching

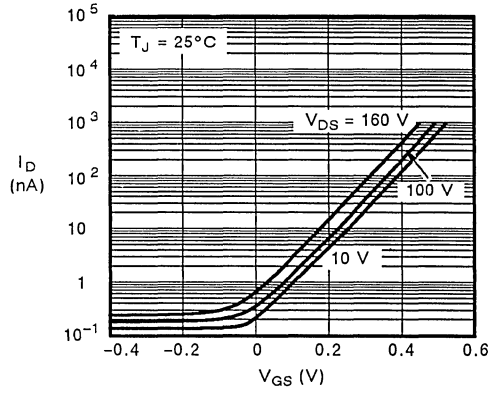


TYPICAL CHARACTERISTICS

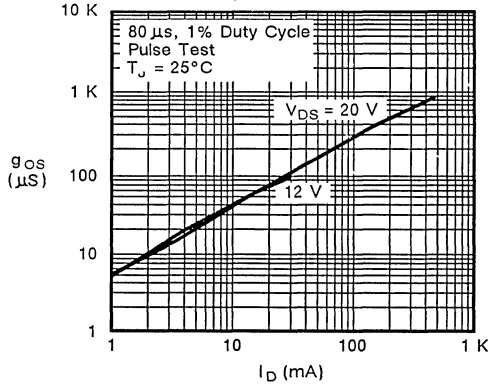
Equivalent Input Noise Voltage vs. Frequency



Body Drain Leakage Current



Output Conductance vs. Drain Current



7

Siliconix incorporated

N-Channel Enhancement-Mode MOSFET

DESIGNED FOR:

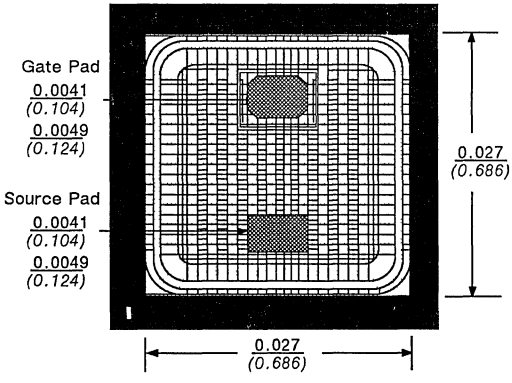
- Switching
- Amplification

FEATURES

- Low $r_{DS(on)}$ < 10 Ω
- Low Cost
- Surface Mount Package SOT-23

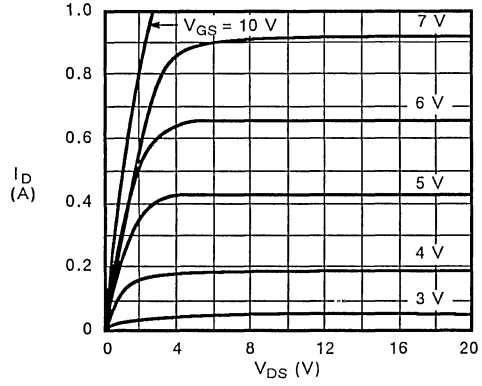
TYPE	PACKAGE	DEVICE
Single	TO-206AC	• VN10LE
	TO-92	• 2N7000, 2N7008 VN0603L, VN0610LL VN2222LL
	TO-237	• VN2222LM
	SOT-23	• VN0603T, VN0605T 2N7002
Quad	14-Pin Plastic	• VQ1000J
	14-Pin Dual-In-Line	• VQ1000P
	Chip	• Available as above specifications

GEOMETRY DIAGRAM

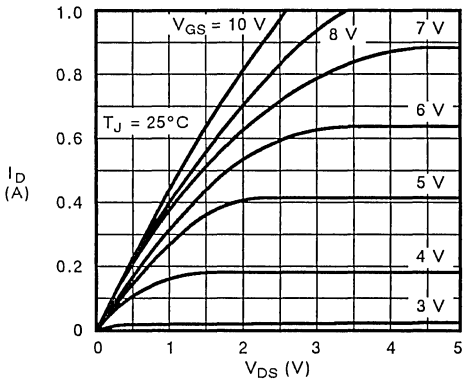


TYPICAL CHARACTERISTICS

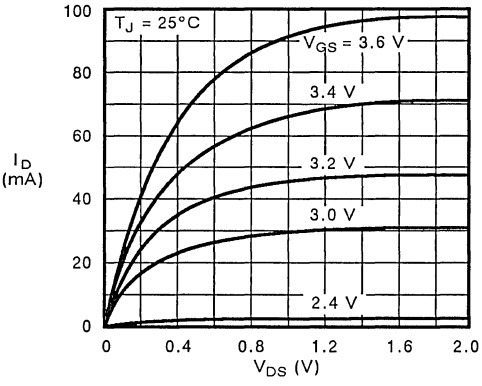
Output Characteristics



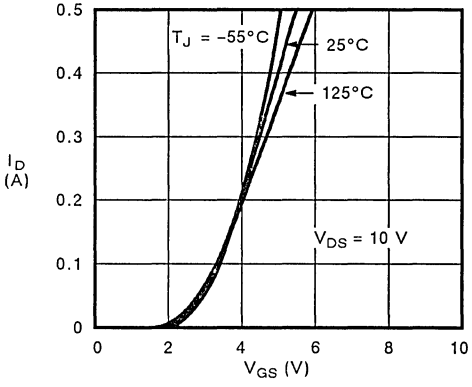
Ohmic Region Characteristics



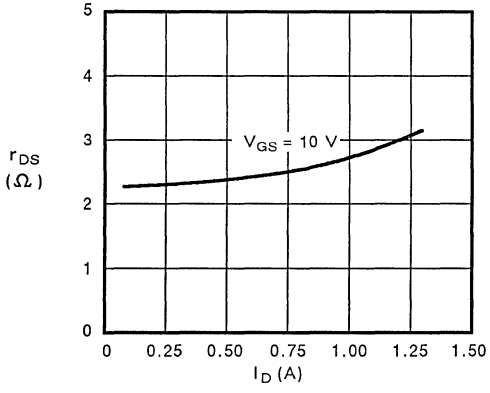
Output Characteristics for Low Gate Drive



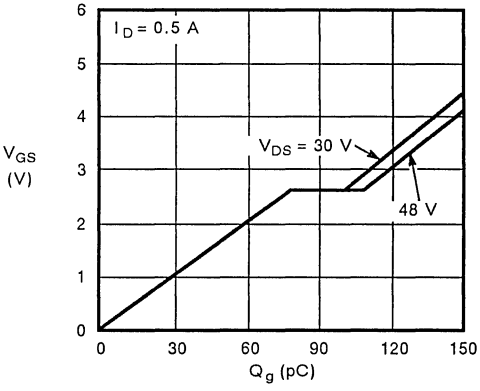
Transfer Characteristics



On-Resistance



Typical Gate Charge



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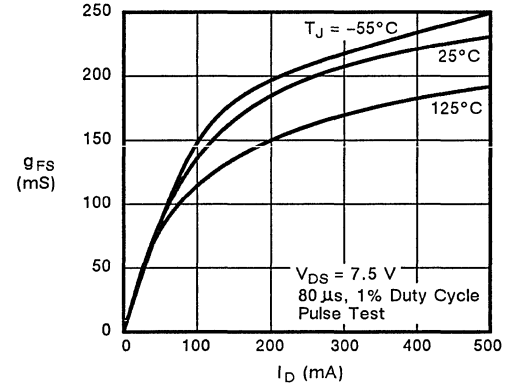
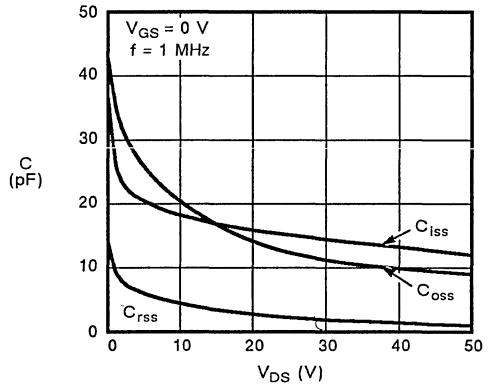
TYPICAL CHARACTERISTICS

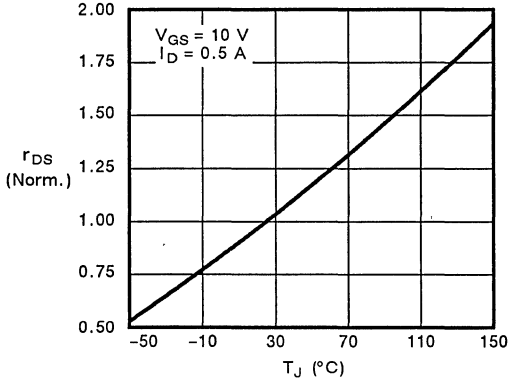
Typical Transconductance



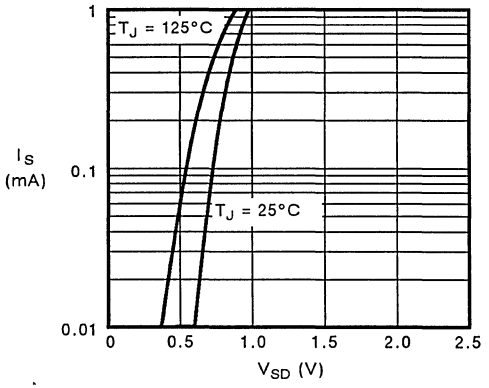
Capacitance



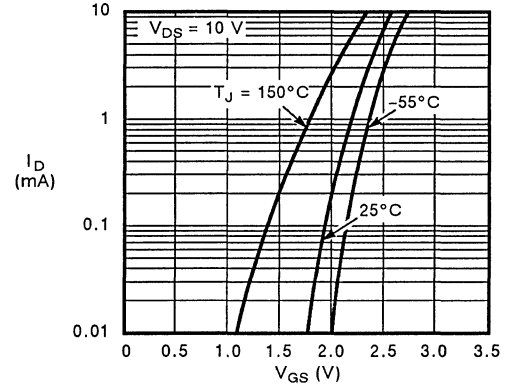
On-Resistance vs. Junction Temperature



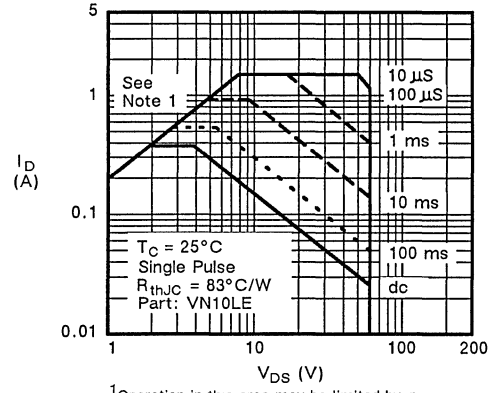
Source-Drain Diode Forward Voltage



Threshold Region



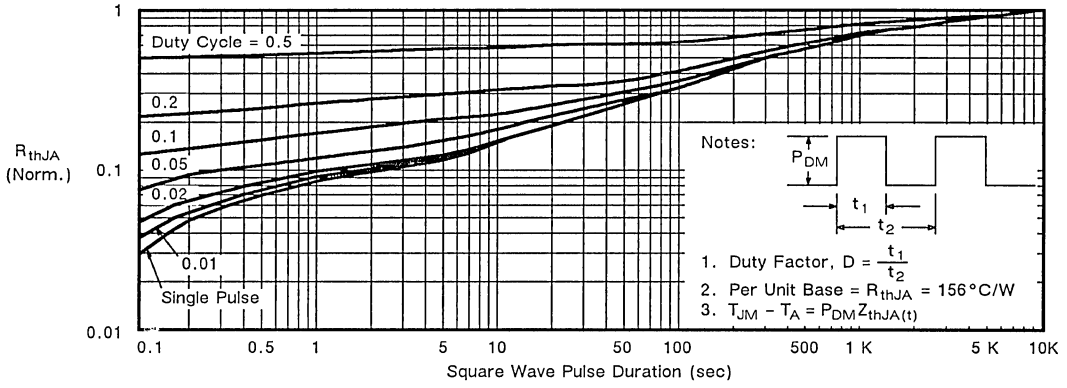
VN10LE – Safe Operating Area



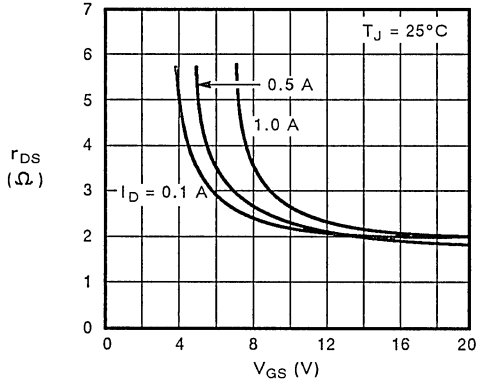
[1]Operation in this area may be limited by $r_{DS(ON)}$

TYPICAL CHARACTERISTICS

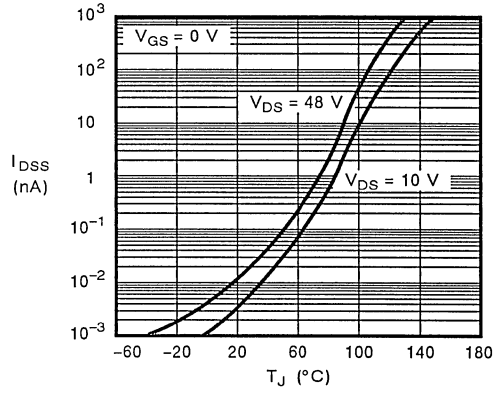
Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



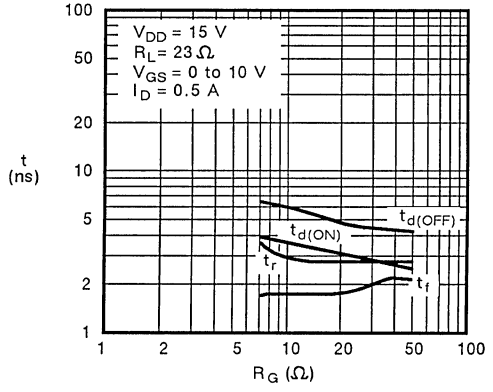
On-Resistance vs. Gate to Source Voltage



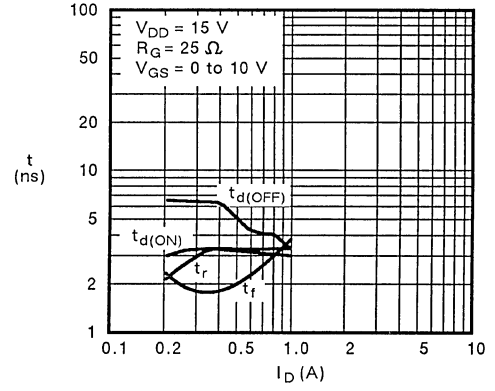
Off State Current



Drive Resistance Effects on Switching



Load Condition Effects on Switching



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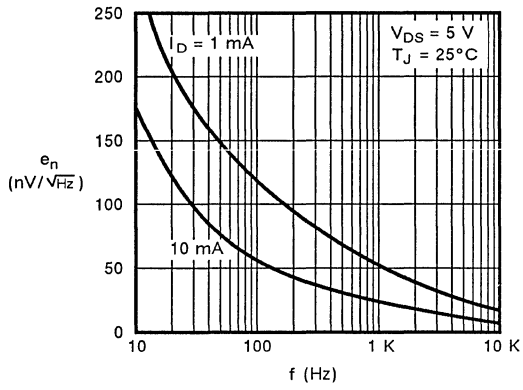
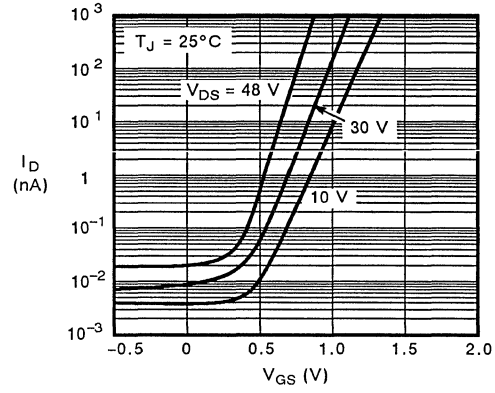
TYPICAL CHARACTERISTICS

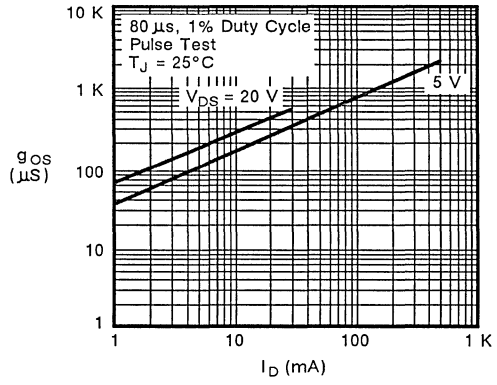
Equivalent Input Noise Voltage vs. Frequency



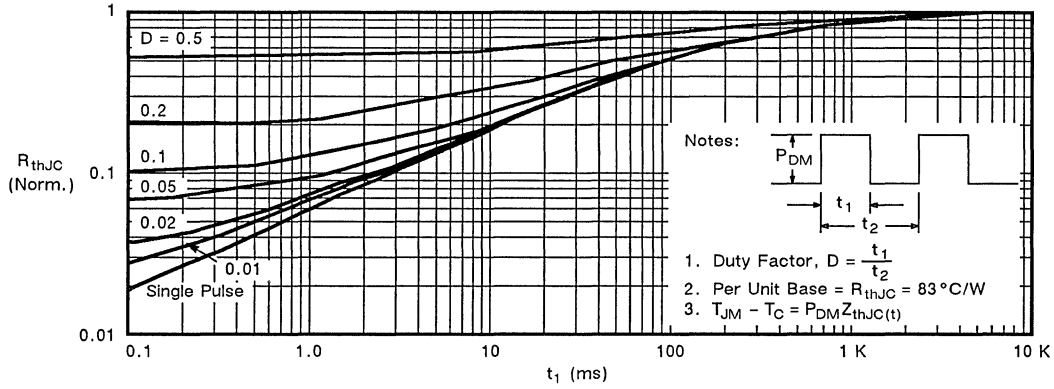
Body Drain Leakage Current



Output Conductance vs. Drain Current



Transient Thermal Response (TO-206AC)



VNDV40

N-Channel Enhancement-Mode MOSFET

DESIGNED FOR:

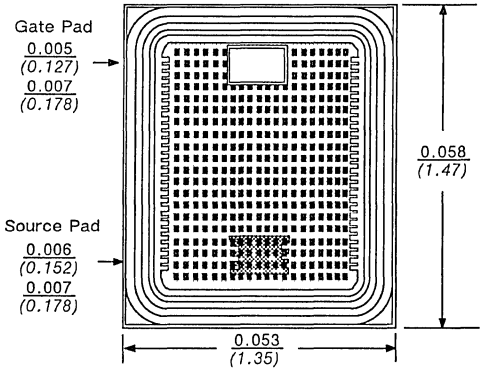
- Switching
- Amplification

FEATURES

- High Breakdown > 400 V
- Low $r_{DS(on)}$ < 12 Ω

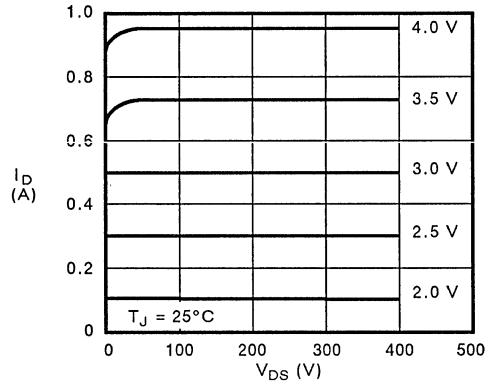
TYPE	PACKAGE	DEVICE
Single	TO-205AD	• VN4012B
	TO-92	• VN3515L, VN4012L
	Chip	• Available as above specifications

GEOMETRY DIAGRAM

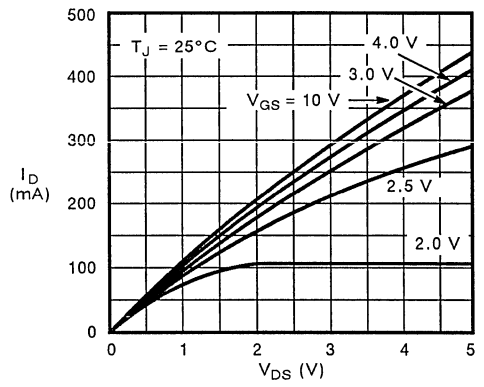


TYPICAL CHARACTERISTICS

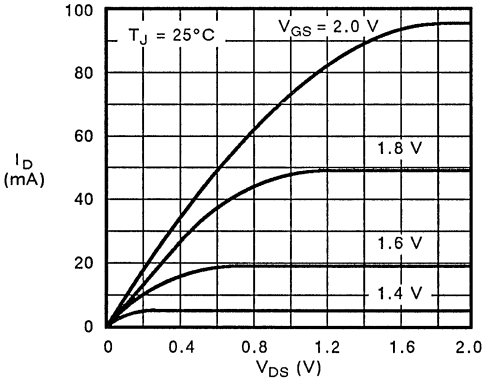
Output Characteristics



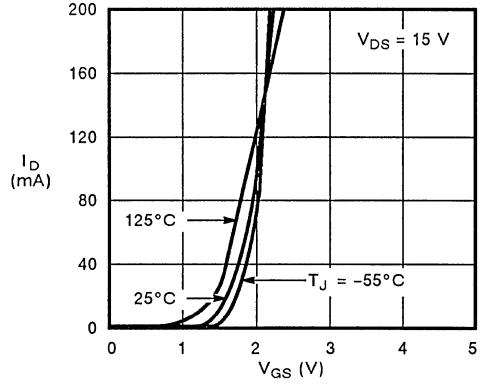
Ohmic Region Characteristics



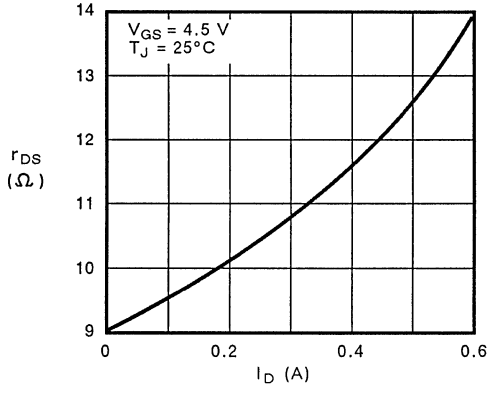
Output Characteristics for Low Gate Drive



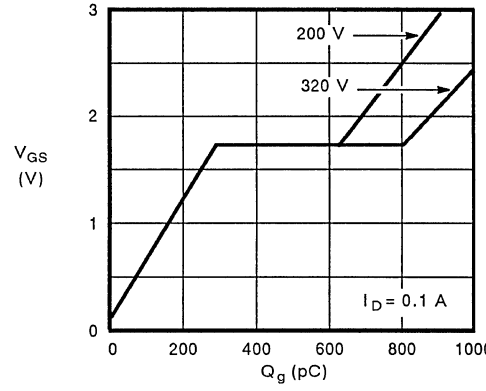
Transfer Characteristics



On-Resistance

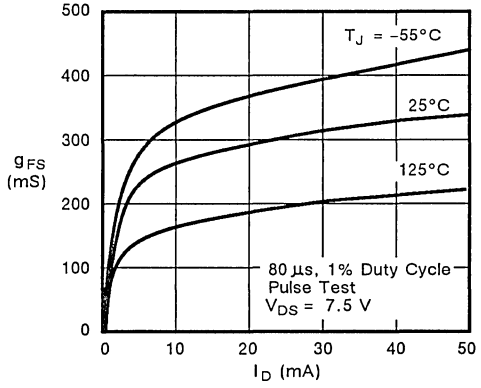


Gate Charge

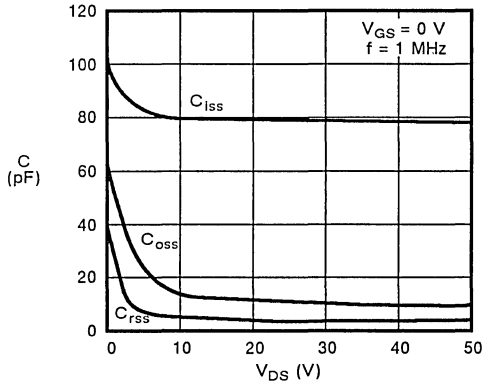


TYPICAL CHARACTERISTICS

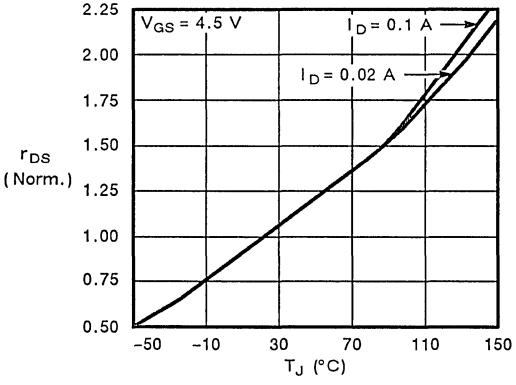
Transconductance



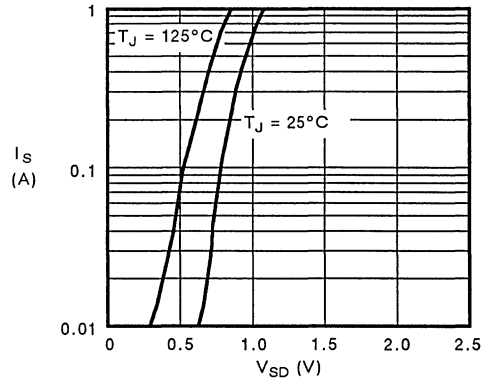
Capacitance



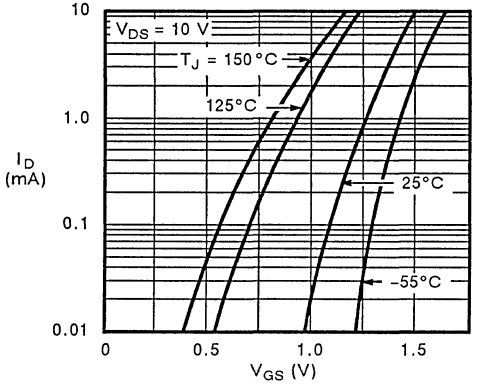
On-Resistance vs. Junction Temperature



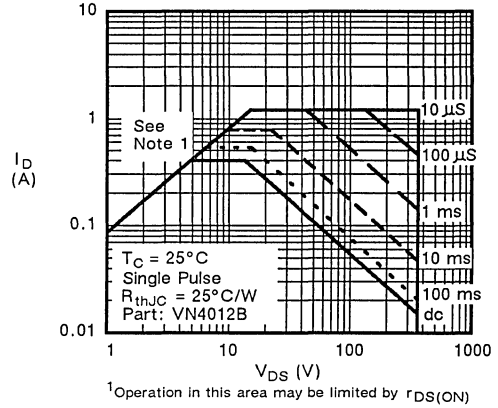
Source-Drain Diode Forward Voltage



Threshold Region



Safe Operating Area

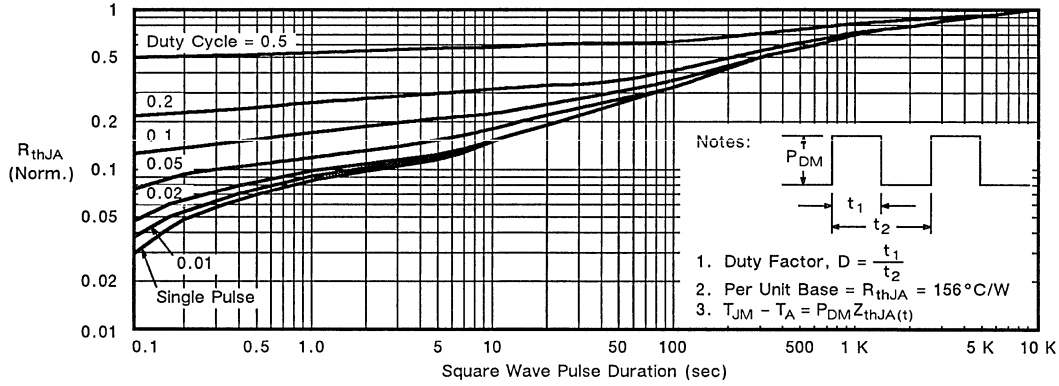


[1]Operation in this area may be limited by $r_{DS(ON)}$

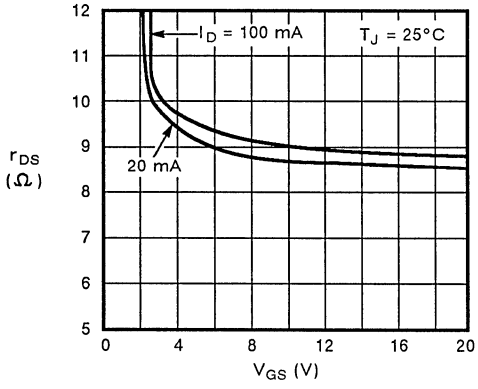
7

TYPICAL CHARACTERISTICS

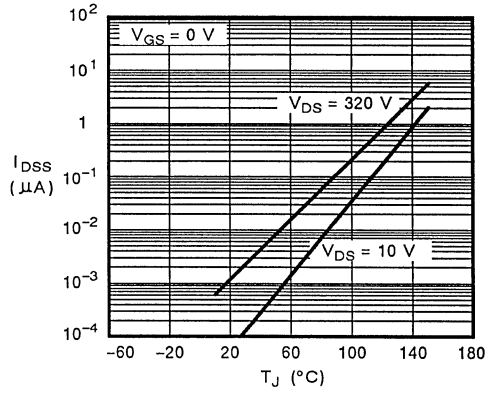
Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



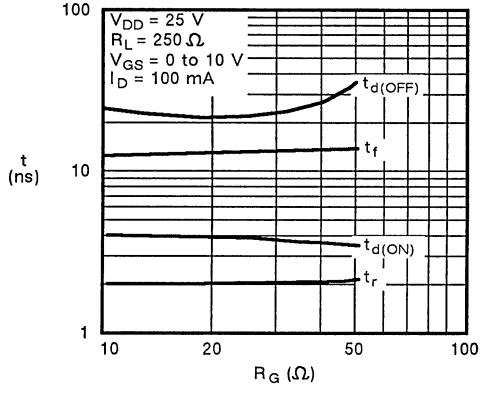
On-Resistance vs. Gate to Source Voltage



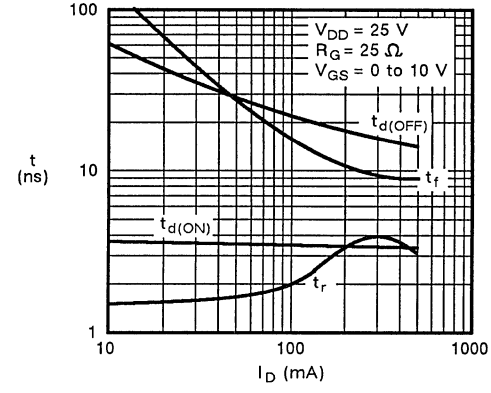
Off State Current



Drive Resistance Effects on Switching

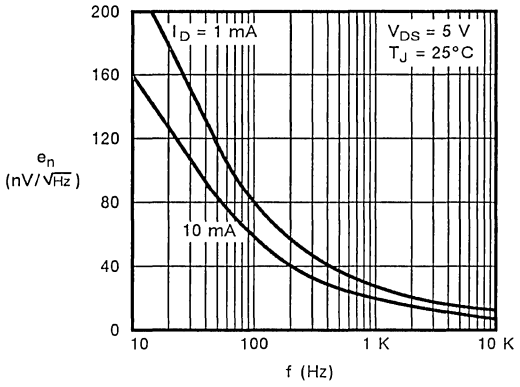


Load Condition Effects on Switching

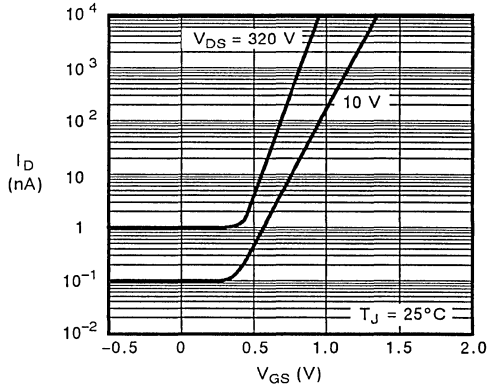


TYPICAL CHARACTERISTICS

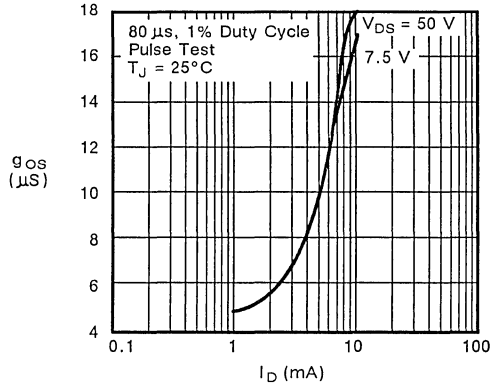
Equivalent Input Noise Voltage vs. Frequency



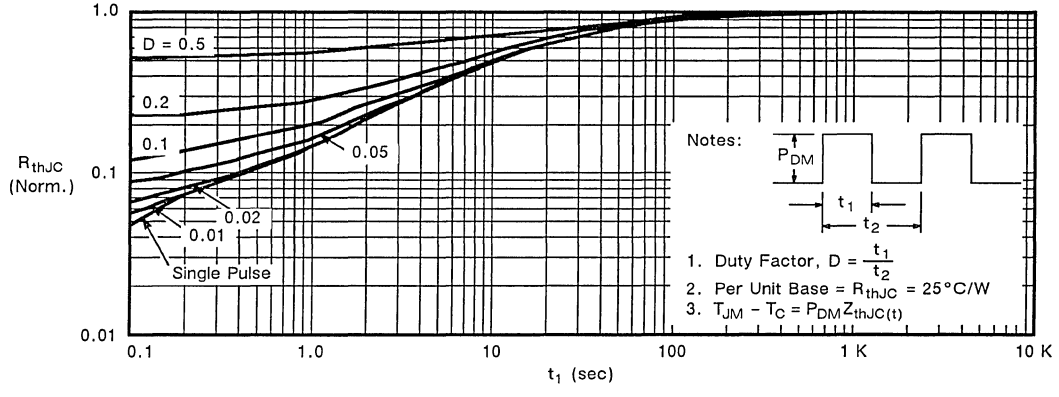
Body-Drain Leakage Current



Output Conductance vs. Drain Current



Transient Thermal Response (TO-205AF)



7

VNMA06

Siliconix incorporated

N-Channel Enhancement-Mode MOSFET

DESIGNED FOR:

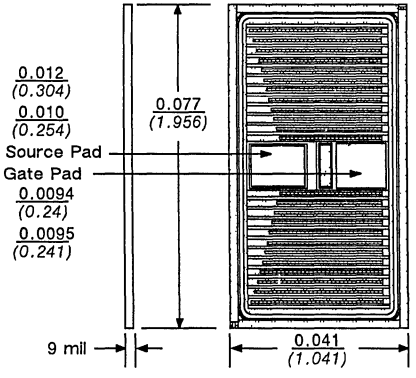
- Switching

TYPE	PACKAGE	DEVICE
Single	TO-205AD	• JANTX2N6660

FEATURES

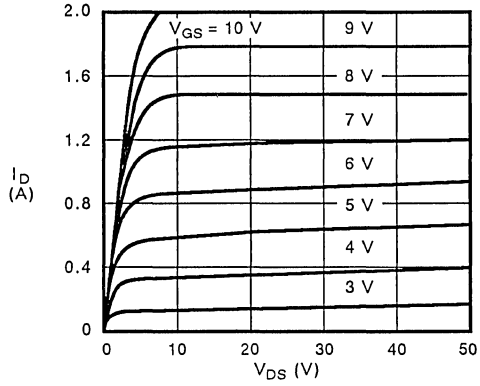
- High Speed for Military Applications
  (see VNDQ06 for Industrial Applications)

GEOMETRY DIAGRAM

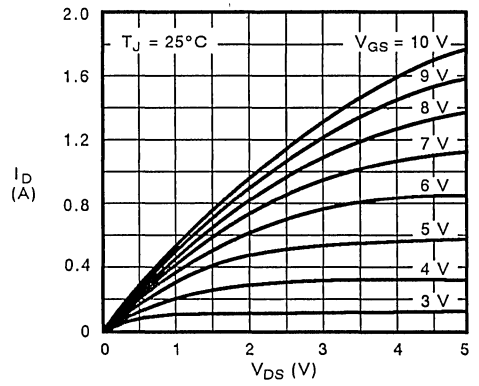


TYPICAL CHARACTERISTICS

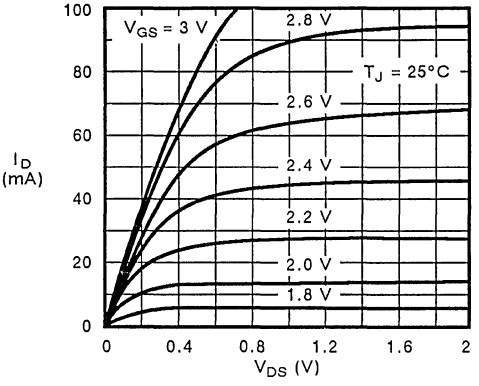
Output Characteristics



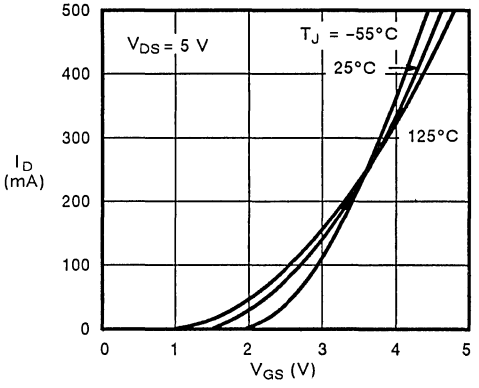
Ohmic Region Characteristics



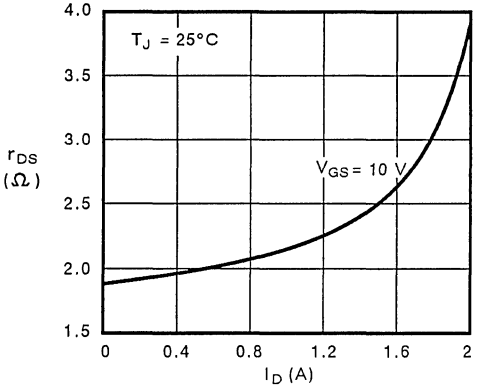
Output Characteristics for Low Gate Drive



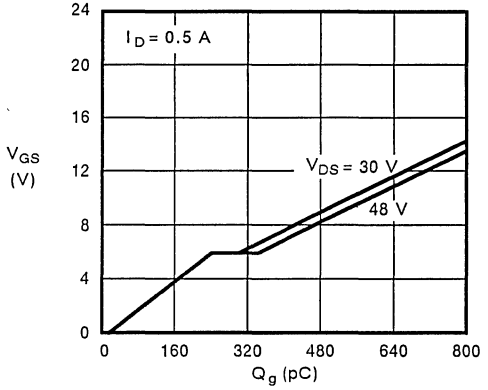
Transfer Characteristics



On-Resistance



Gate Charge



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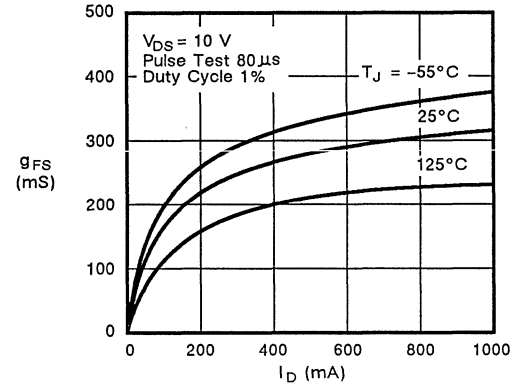
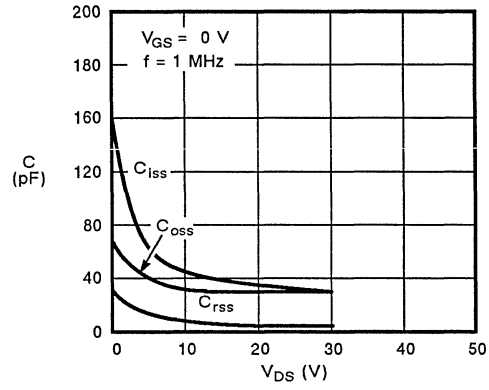
TYPICAL CHARACTERISTICS

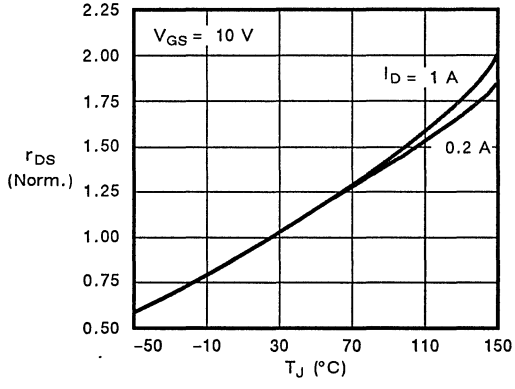
Transconductance



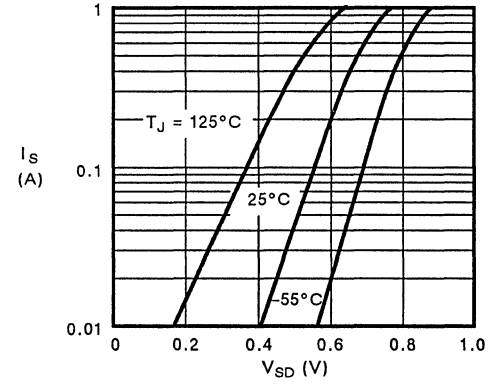
Capacitance



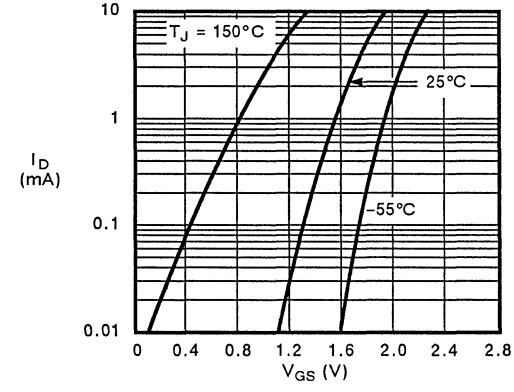
On-Resistance vs. Junction Temperature



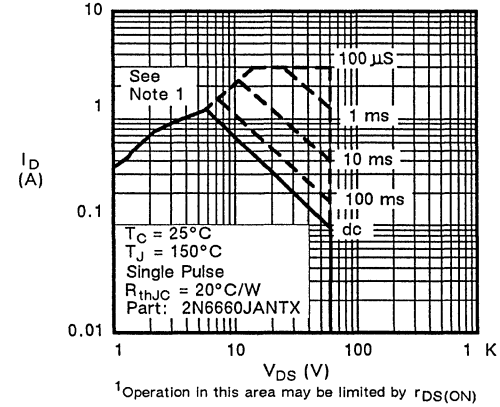
Source-Drain Diode Forward Voltage



Threshold Region



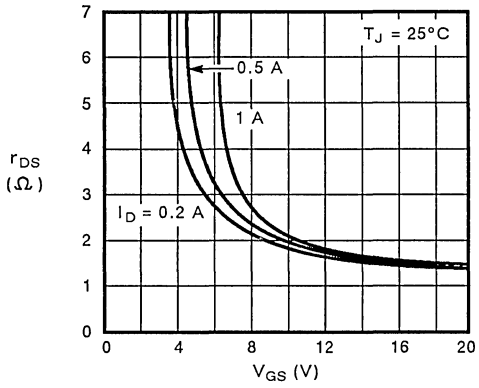
Safe Operating Area



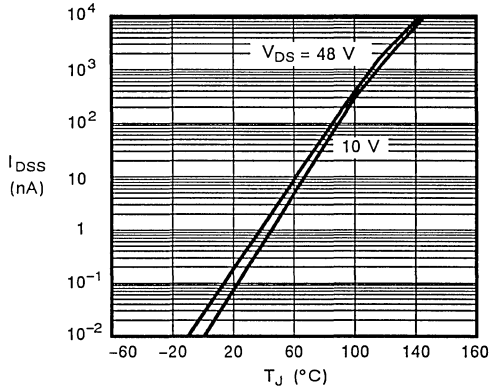
[1]Operation in this area may be limited by $r_{DS(ON)}$

TYPICAL CHARACTERISTICS

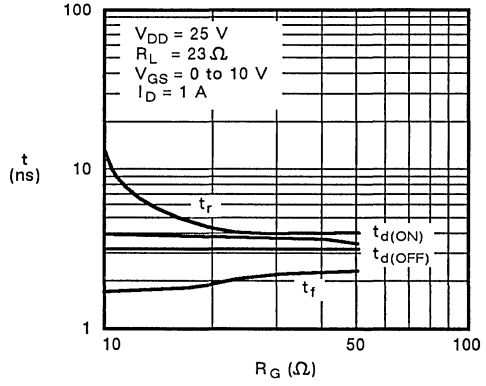
On-Resistance vs. Gate to Source Voltage



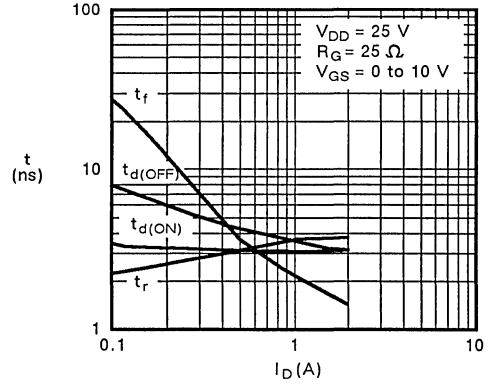
Off State Current



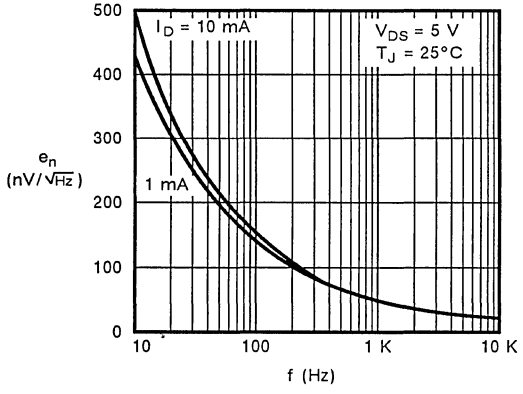
Drive Resistance Effects on Switching



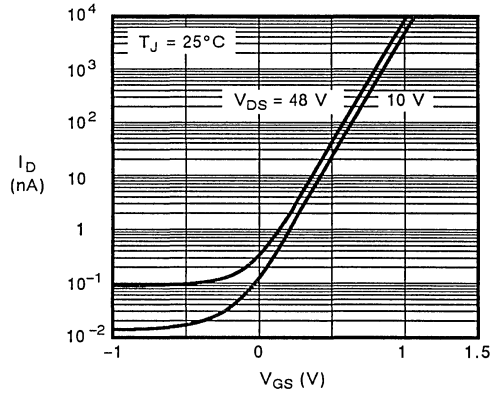
Load Condition Effects on Switching



Equivalent Input Noise Voltage vs. Frequency



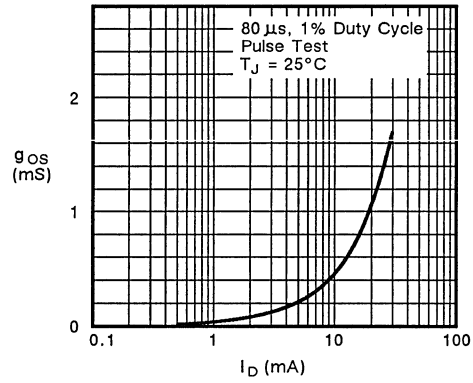
Body-Drain Leakage Current



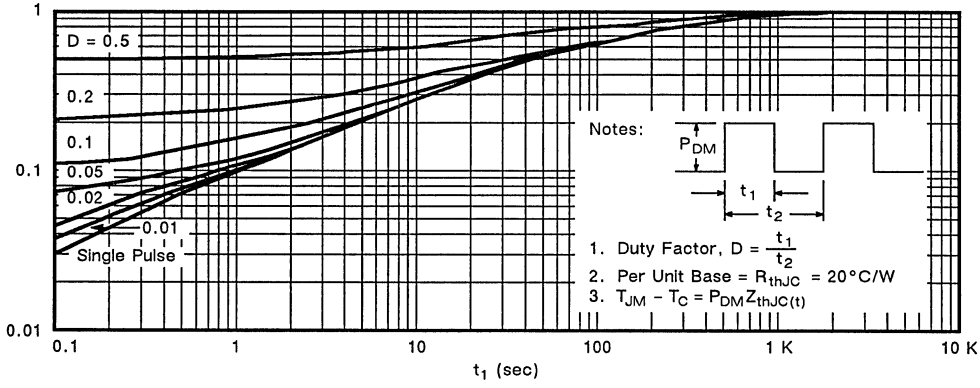
7

TYPICAL CHARACTERISTICS

Output Conductance vs. Drain Current



Transient Thermal Response (TO-39)



N-Channel Enhancement-Mode MOSFET

DESIGNED FOR:

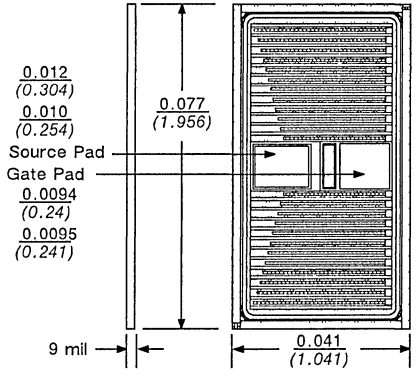
- Switching

FEATURES

- High Speed for Military Applications (see VNDQ09 for Industrial Applications)

TYPE	PACKAGE	DEVICE
Single	TO-205AD	• JANTX2N6661

GEOMETRY DIAGRAM



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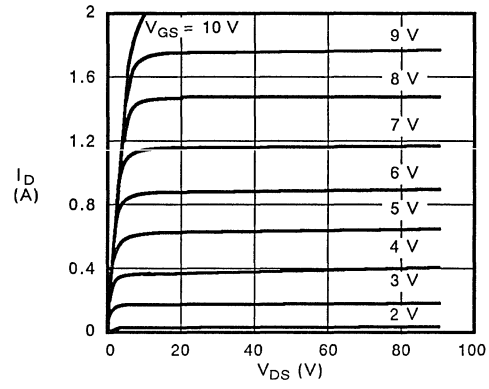
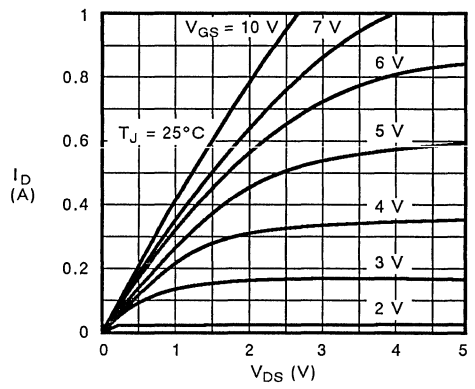
TYPICAL CHARACTERISTICS

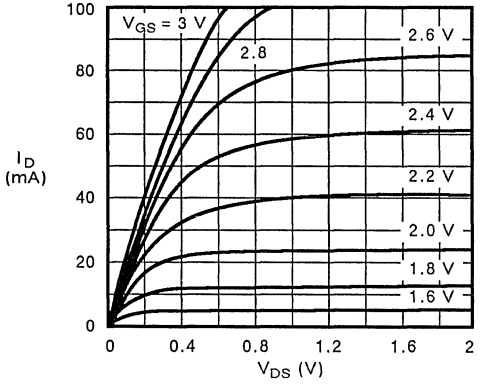
Output Characteristics



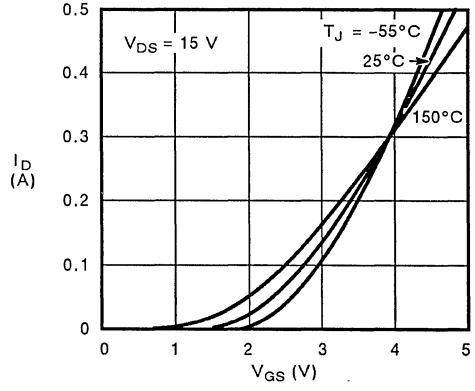
Ohmic Region Characteristics



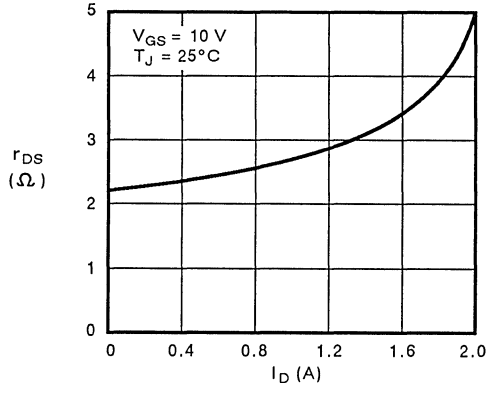
Output Characteristics for Low Gate Drive



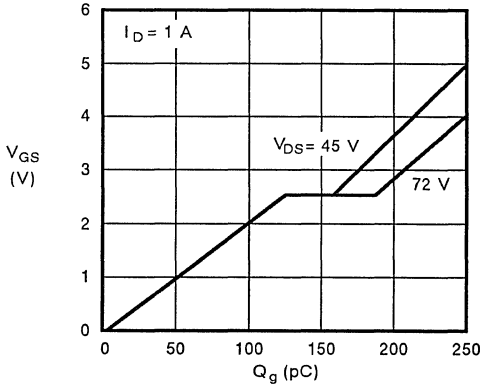
Transfer Characteristics



On-Resistance

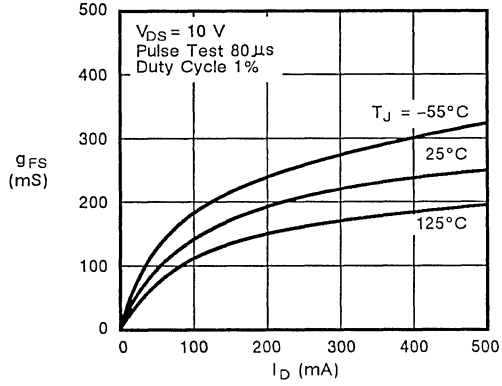


Gate Charge

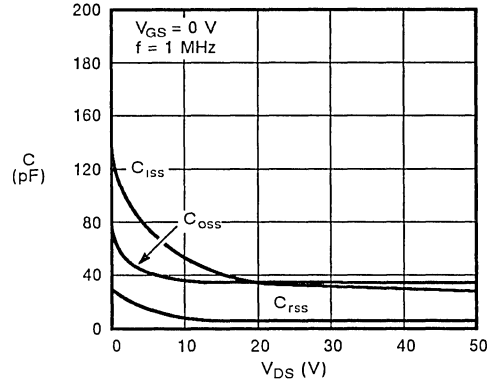


TYPICAL CHARACTERISTICS

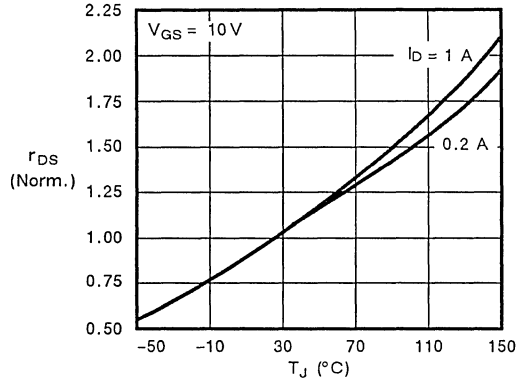
Transconductance



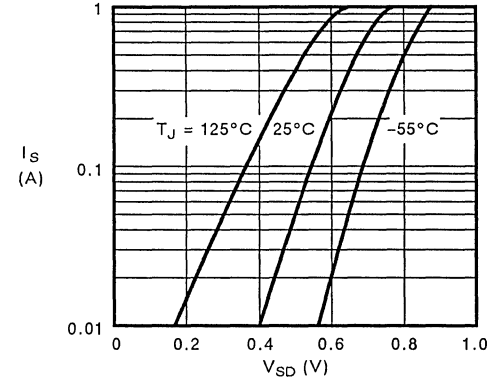
Capacitance



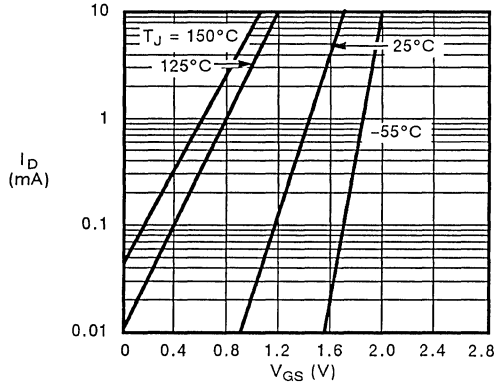
On-Resistance vs. Junction Temperature



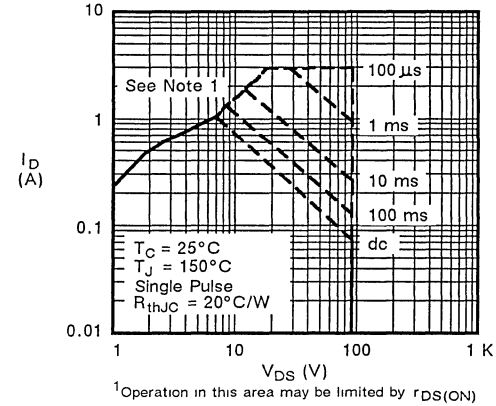
Source-Drain Diode Forward Voltage



Threshold Region



Safe Operating Area

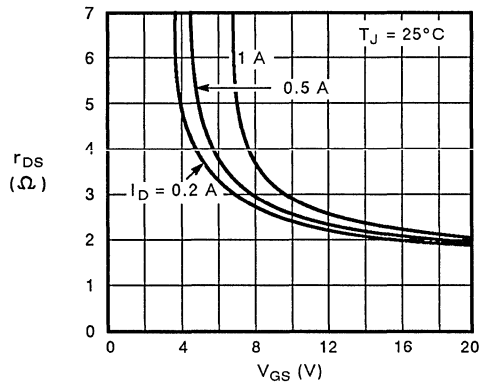


[1]Operation in this area may be limited by $r_{DS(ON)}$

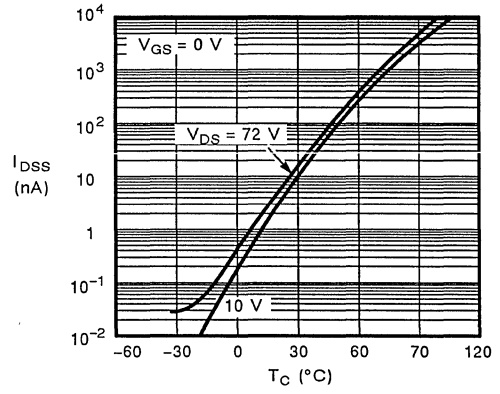
7

TYPICAL CHARACTERISTICS

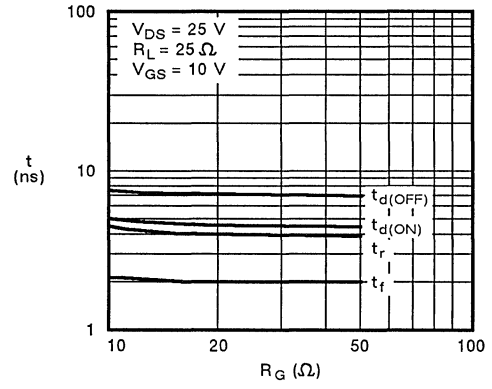
On-Resistance vs. Gate to Source Voltage



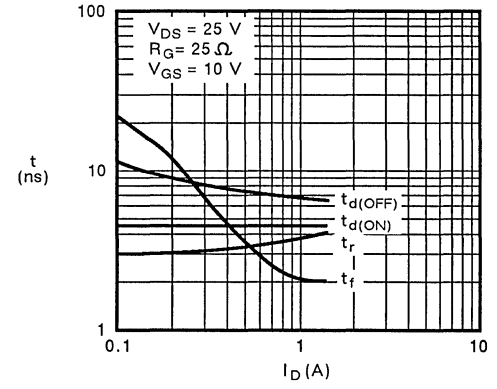
Off State Current



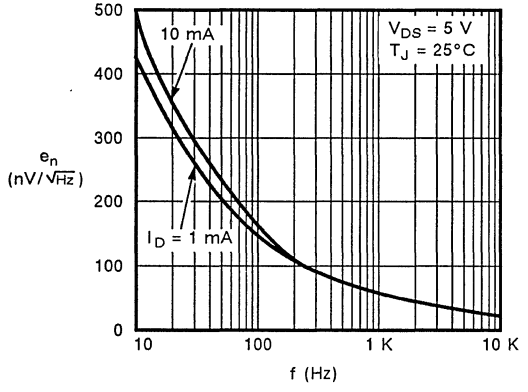
Drive Resistance Effects on Switching



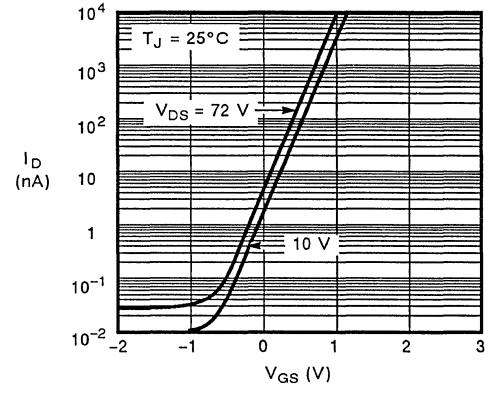
Load Condition Effects on Switching



Equivalent Input Noise Voltage vs. Frequency

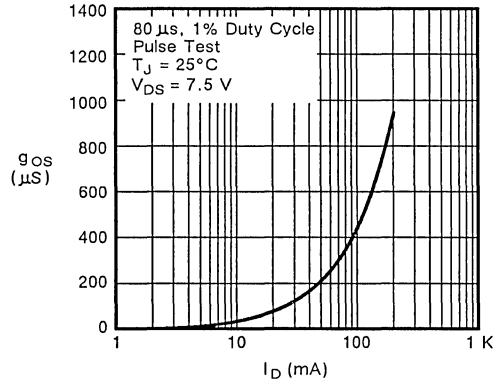


Body Drain Leakage Current

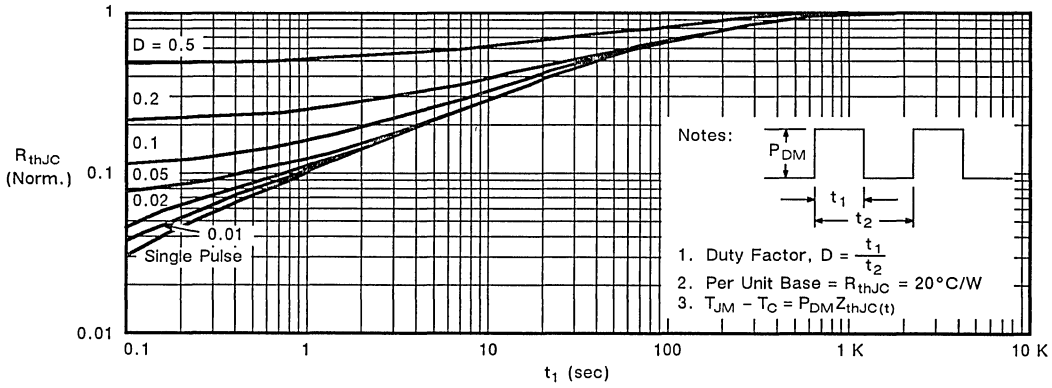


TYPICAL CHARACTERISTICS

Output Conductance vs. Drain Current



Transient Thermal Response (TO-39)



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VPDQ20

Siliconix incorporated

P-Channel Enhancement-Mode MOSFET

DESIGNED FOR:

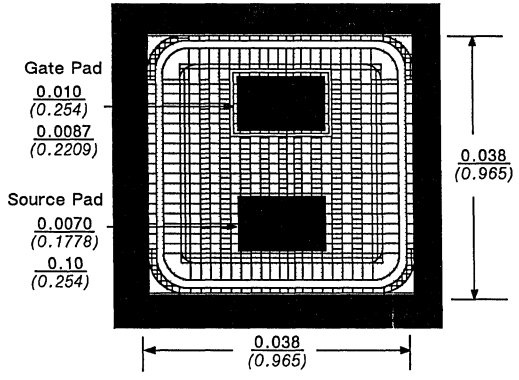
- Switching
- Amplification

FEATURES

- High Breakdown > 200 V
- Low $r_{DS(on)}$ < 20 Ω

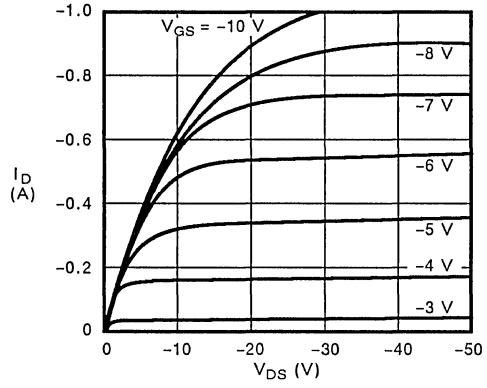
TYPE	PACKAGE	DEVICE
Single	TO-206AC	• VP2020E
	TO-92	• VP2020L BSS92
	Chip	• Available as above specifications

GEOMETRY DIAGRAM

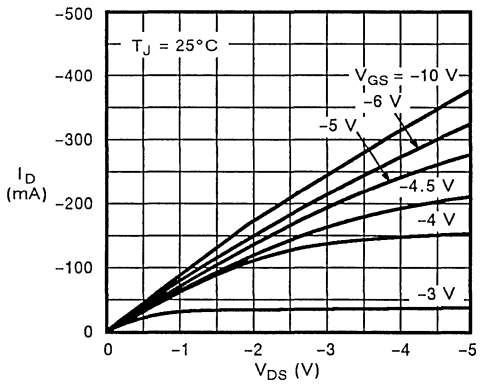


TYPICAL CHARACTERISTICS

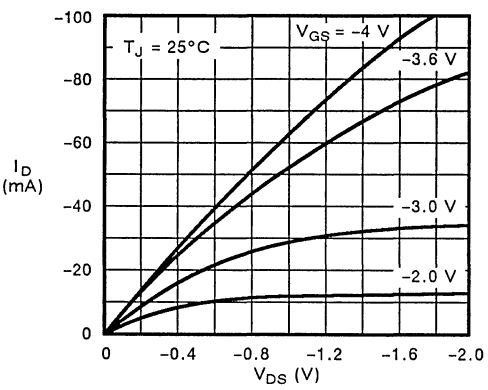
Output Characteristics



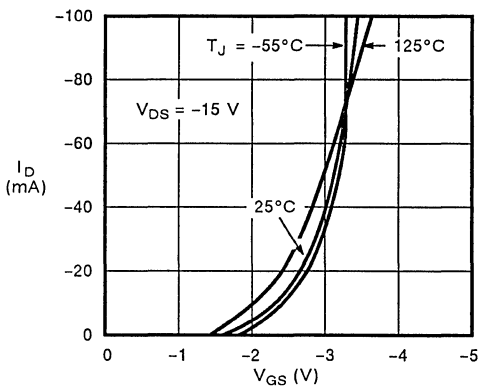
Ohmic Region Characteristics



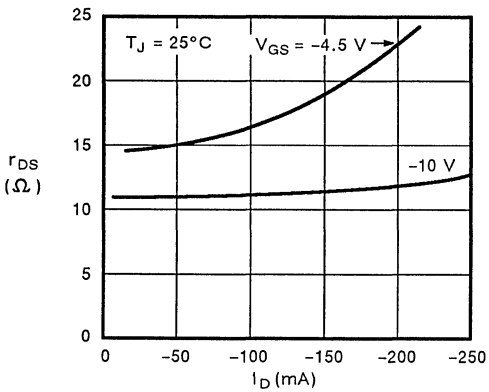
Output Characteristics for Low Gate Drive



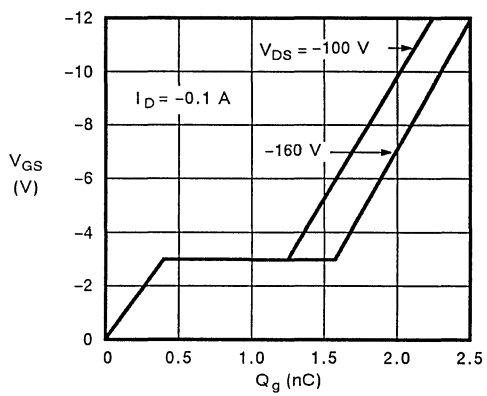
Transfer Characteristics



On-Resistance



Gate Charge



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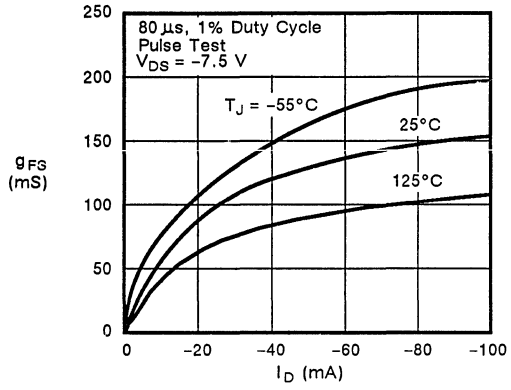
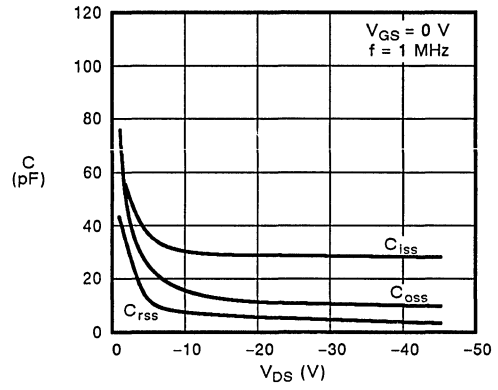
TYPICAL CHARACTERISTICS

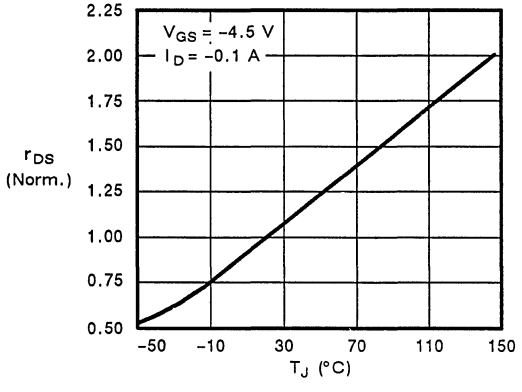
Transconductance



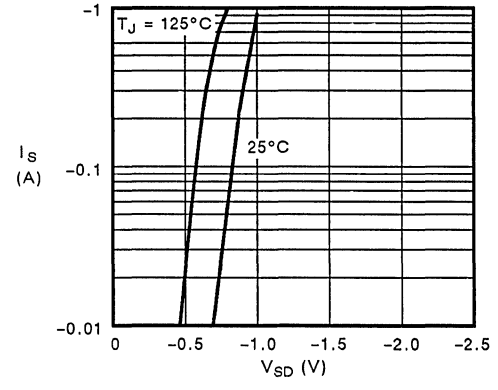
Capacitance



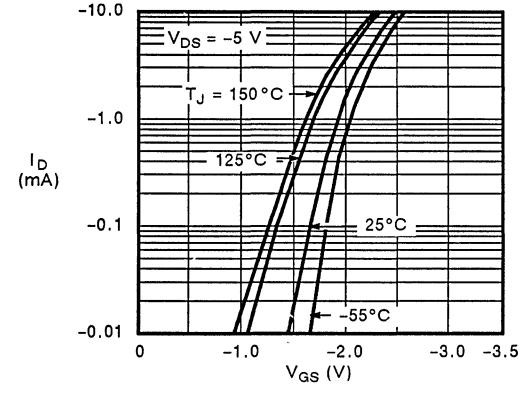
On-Resistance vs. Junction Temperature



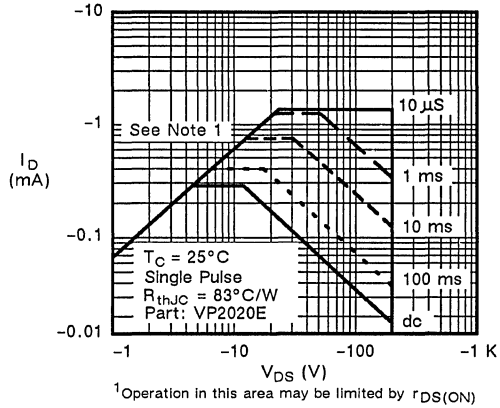
Source-Drain Diode Forward Voltage



Threshold Region



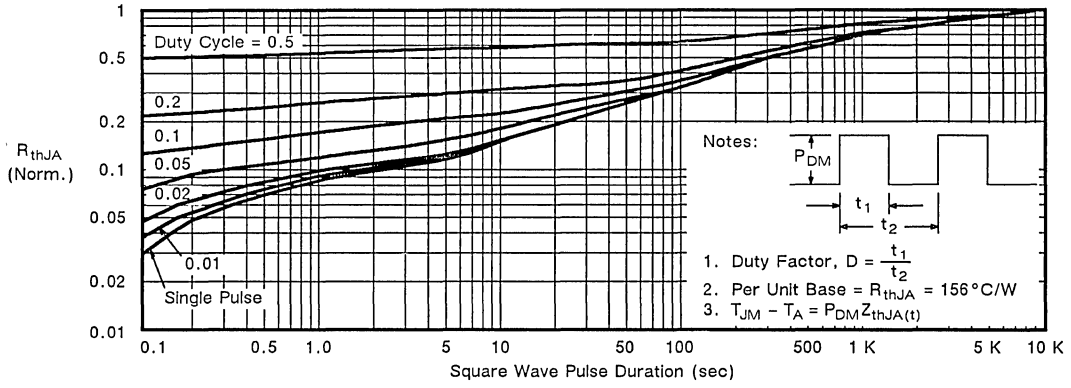
Safe Operating Area



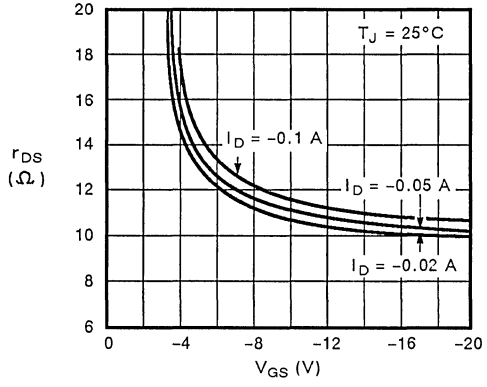
[1]Operation in this area may be limited by $r_{DS(ON)}$

TYPICAL CHARACTERISTICS

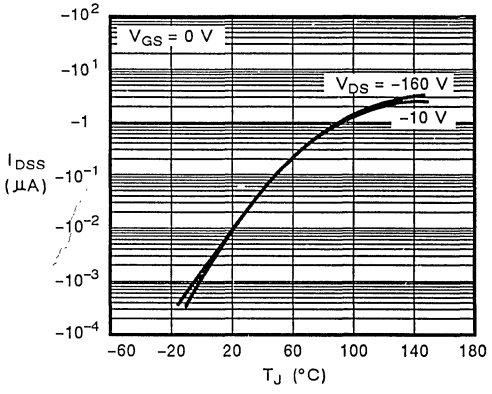
Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



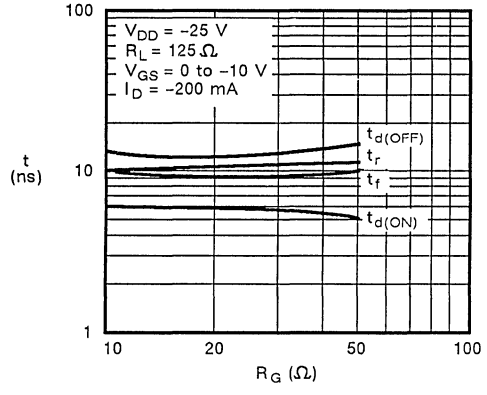
On-Resistance vs. Gate to Source Voltage



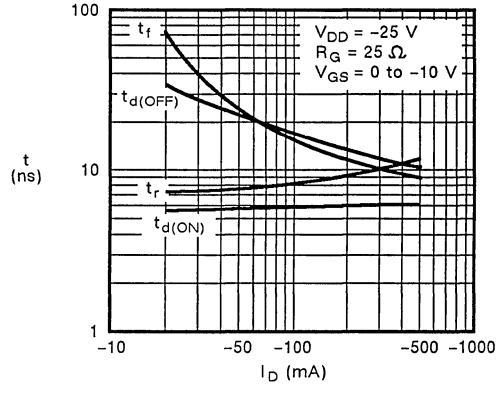
Off State Current



Drive Resistance Effects on Switching



Load Condition Effects on Switching



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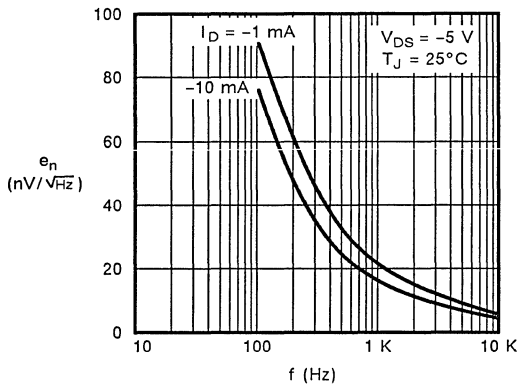
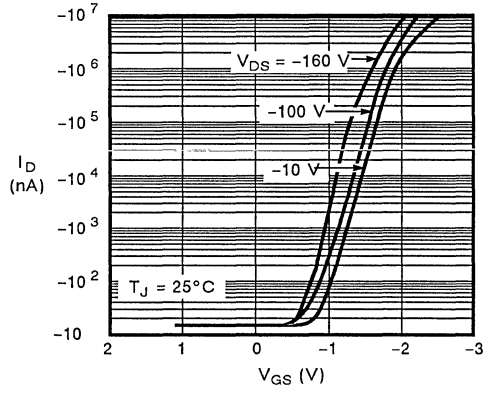
TYPICAL CHARACTERISTICS

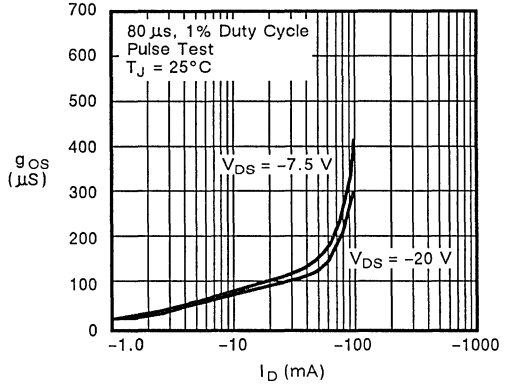
Equivalent Input Noise Voltage vs. Frequency



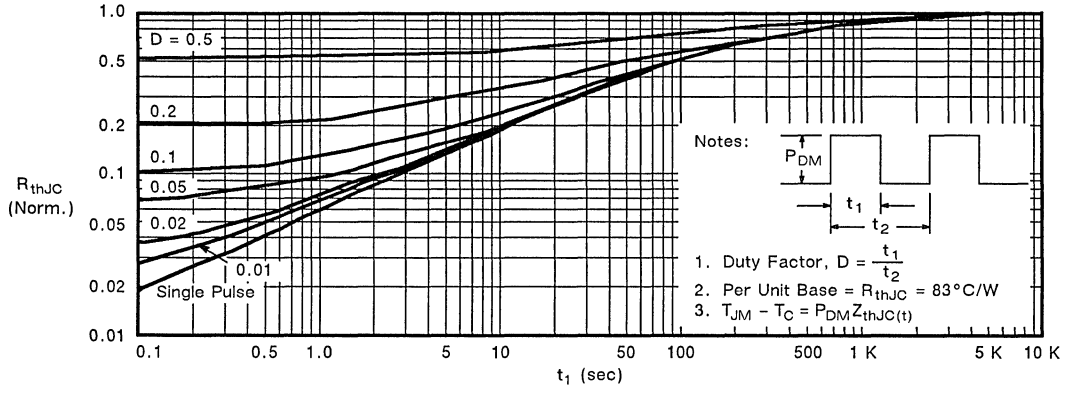
Body Drain Leakage Current



Output Conductance vs. Drain Current



Transient Thermal Response (TO-206AC)



P-Channel Enhancement-Mode MOSFET "FETlington"

DESIGNED FOR:

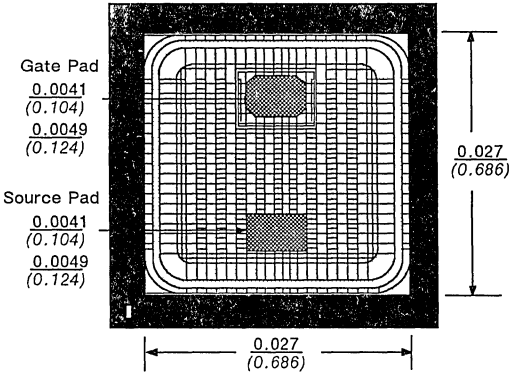
- Switching (P-Channel Complement to 2N7000)

FEATURES

- Low $r_{DS(on)}$ < 10 Ω
- Available in Surface Mount

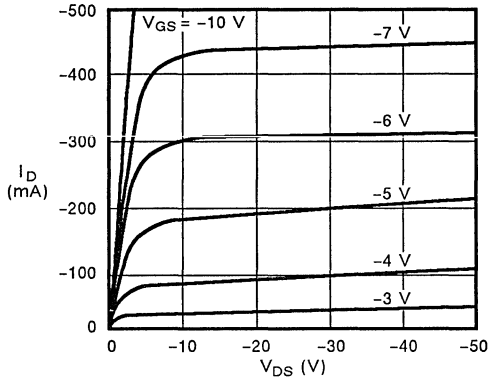
TYPE	PACKAGE	DEVICE
Single	TO-206AC	• VP0610E, TP0610E
	TO-92	• VP0610L, TP0610L
	SOT-23	• VP0610T, TP0610T
	14-Pin Plastic	• VQ2000J
	14-Pin Dual-In-Line	• VQ2000P
	Chip	• Available as above specifications

GEOMETRY DIAGRAM

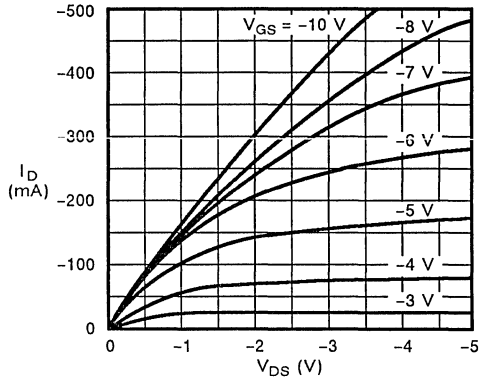


TYPICAL CHARACTERISTICS

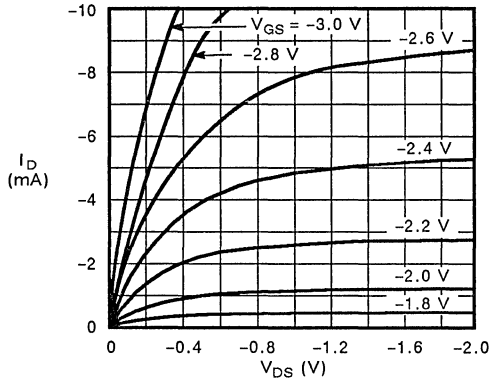
Output Characteristics



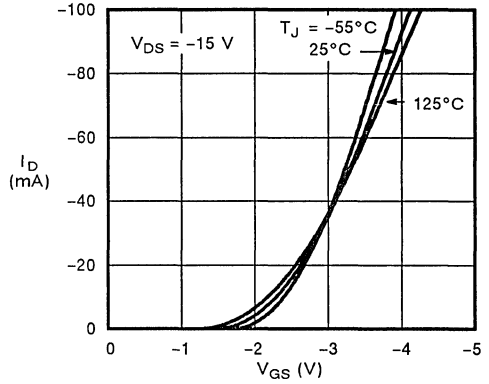
Ohmic Region Characteristics



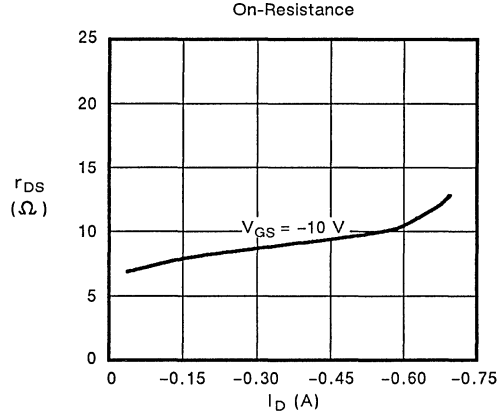
Output Characteristics for Low Gate Drive



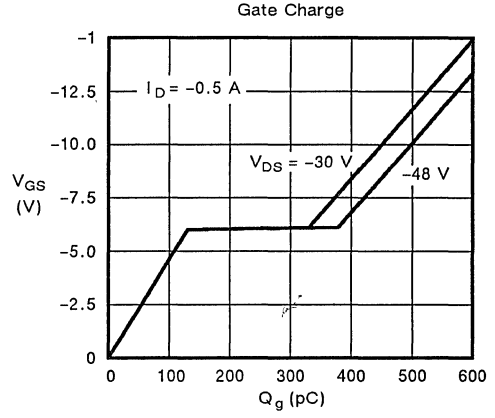
Transfer Characteristics



On-Resistance

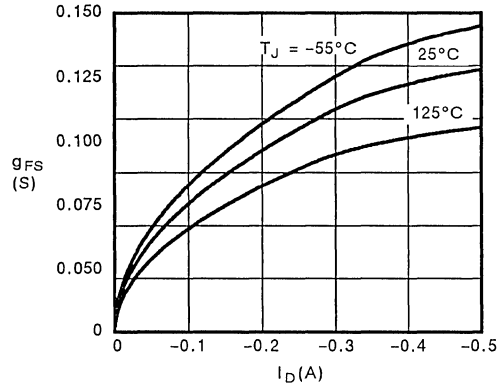


Gate Charge

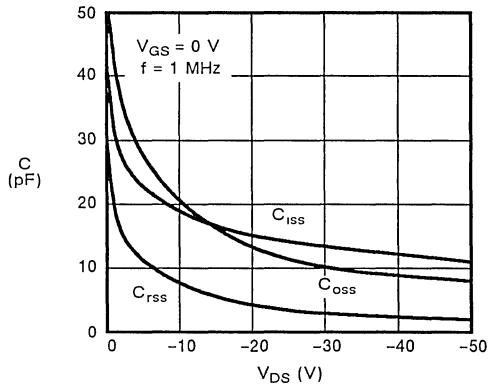


TYPICAL CHARACTERISTICS

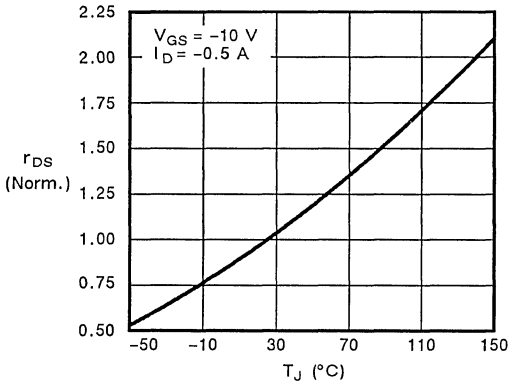
Transconductance



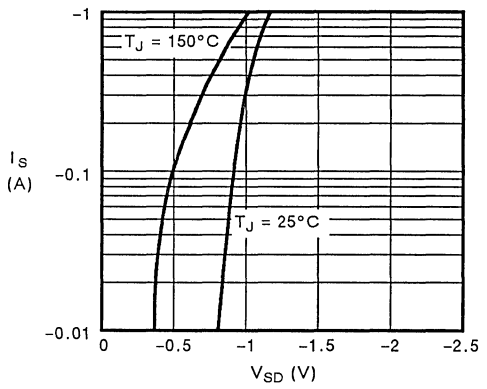
Capacitance



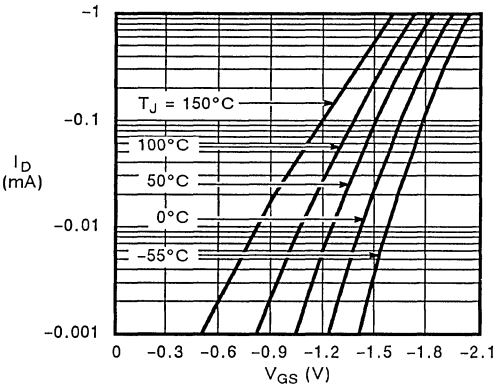
On-Resistance vs. Junction Temperature



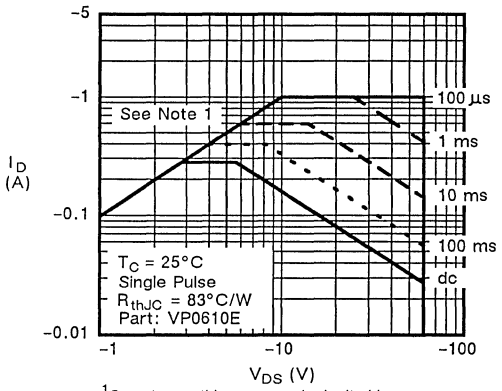
Source-Drain Diode Forward Voltage



Threshold Region



Safe Operating Area

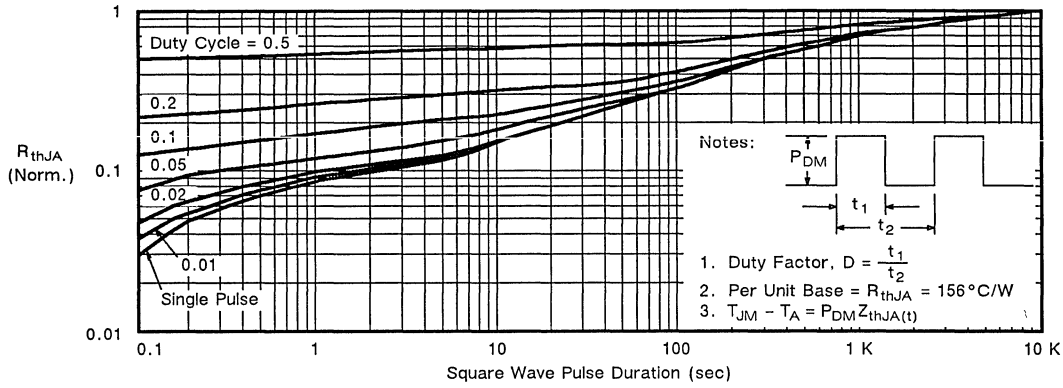


[1]Operation in this area may be limited by $r_{DS(ON)}$

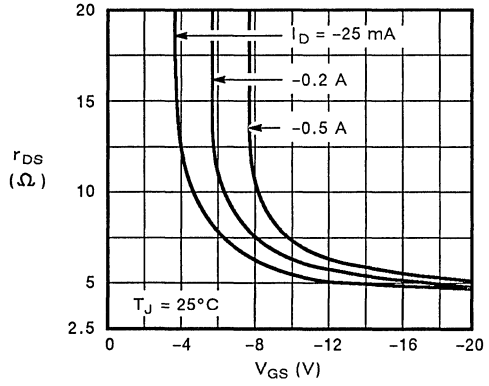
7

TYPICAL CHARACTERISTICS

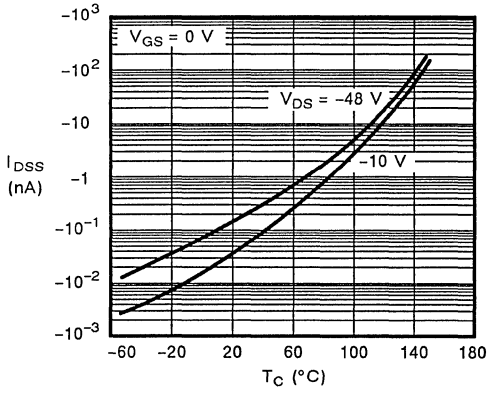
Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



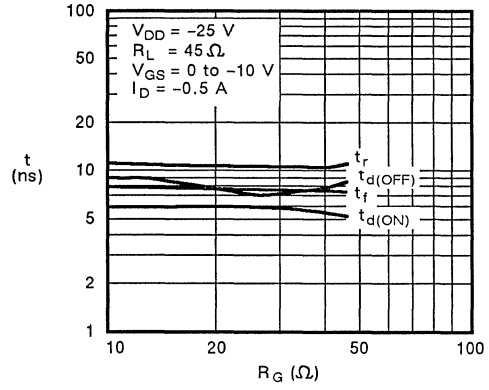
On-Resistance vs. Gate to Source Voltage



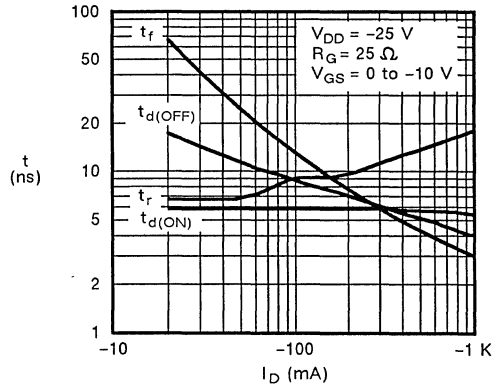
Off State Current



Drive Resistance Effects on Switching

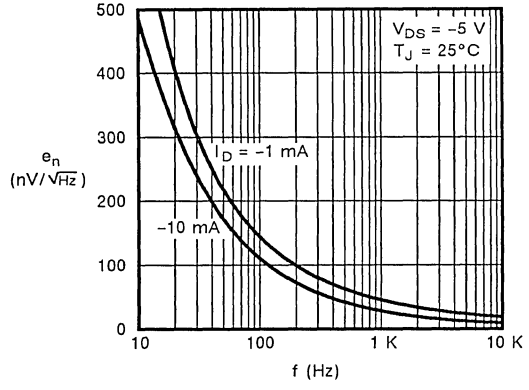


Load Condition Effects on Switching

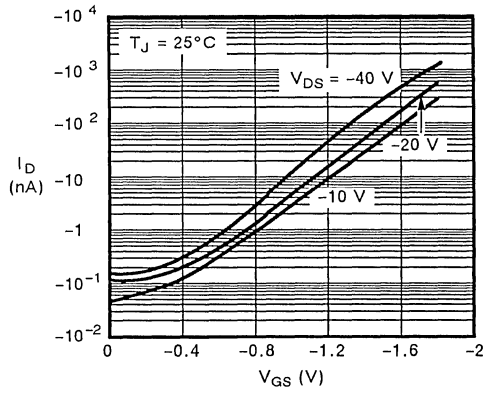


TYPICAL CHARACTERISTICS

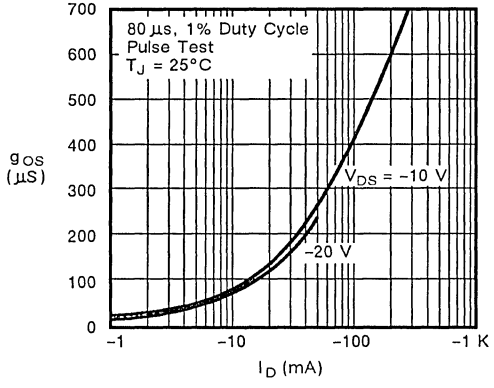
Equivalent Input Noise Voltage vs. Frequency



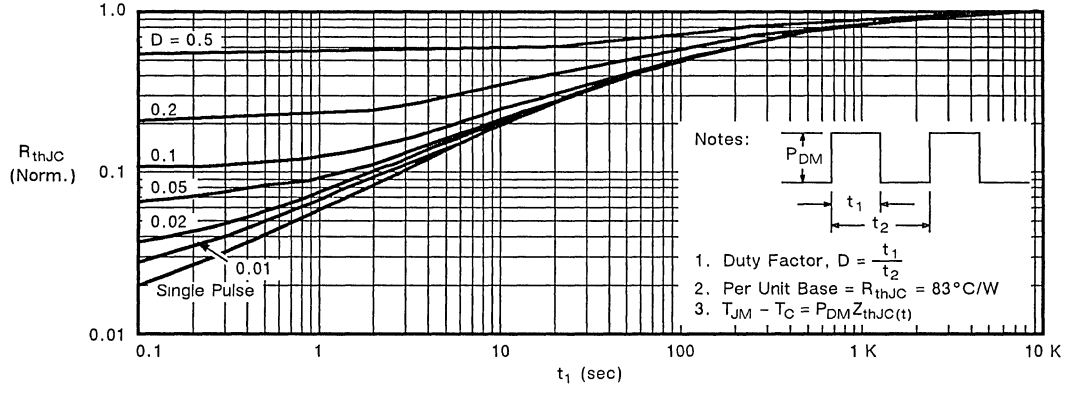
Body Drain Leakage Current



Output Conductance vs. Drain Current



Transient Thermal Response (TO-206AC)



7

VPDV10

Siliconix incorporated

P-Channel Enhancement-Mode MOSFET

DESIGNED FOR:

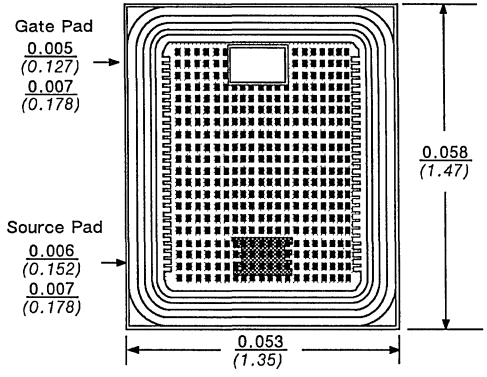
- Switching
- Amplification

FEATURES

- Low $r_{DS(on)} < 5\ \Omega$

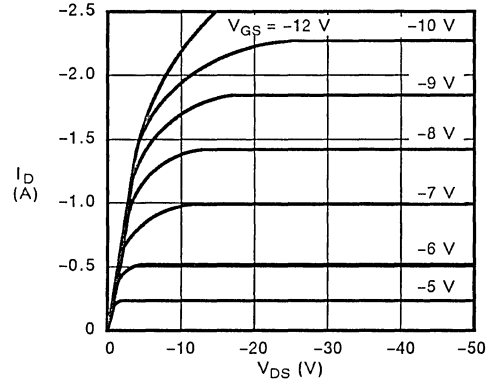
TYPE	PACKAGE	DEVICE
Single	TO-205AD	• VP0808B, VP1008B
	TO-92	• VP0808L, VP1008L
	TO-237	• VP0808M, VP1008M
Quad	14-Pin Plastic	• VQ2004J, VQ2006J
	14-Pin Dual-In-Line	• VQ2004P, VQ2006P
	Chip	• Available as above specifications

GEOMETRY DIAGRAM

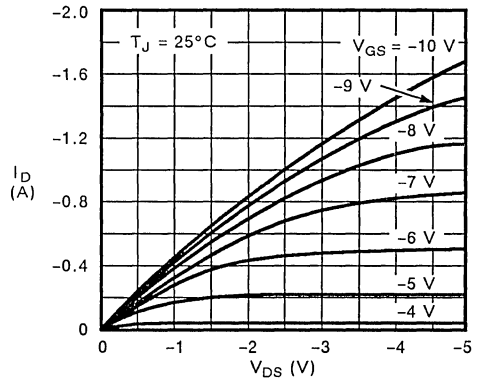


TYPICAL CHARACTERISTICS

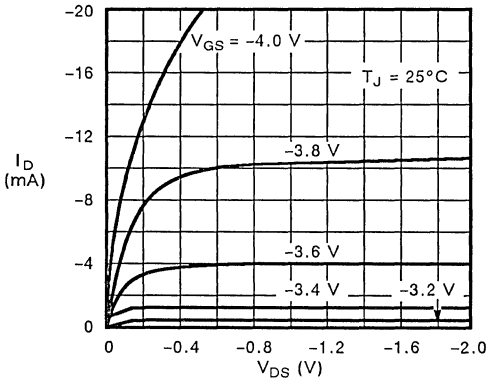
Output Characteristics



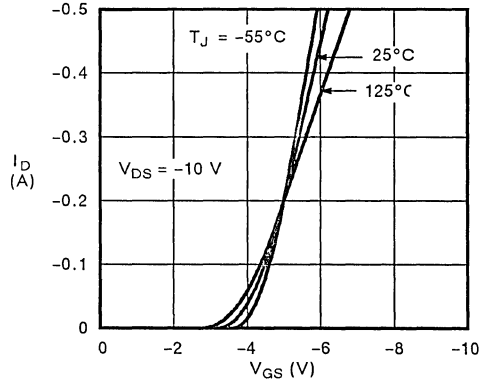
Ohmic Region Characteristics



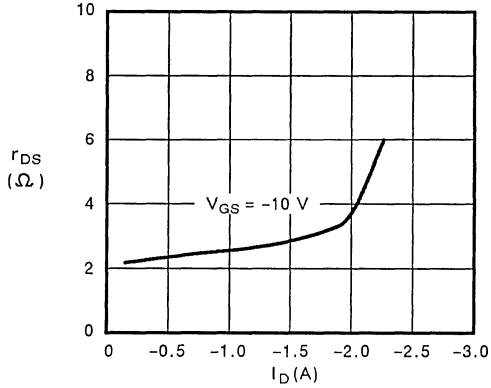
Output Characteristics for Low Gate Drive



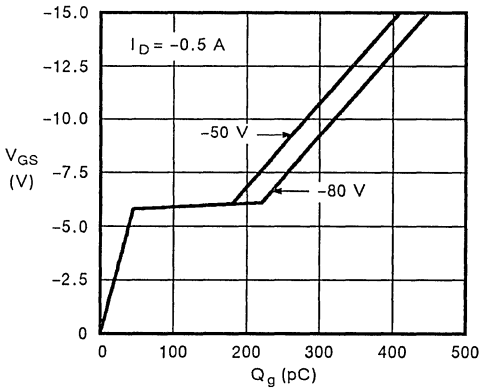
Transfer Characteristics



On-Resistance



Gate Charge



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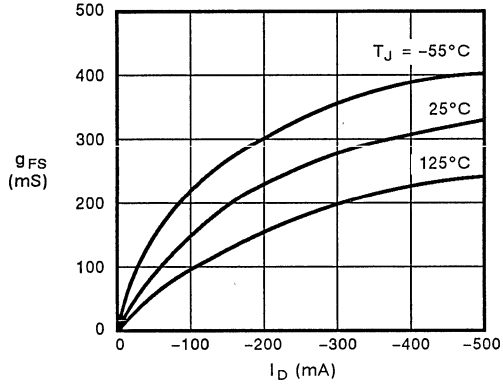
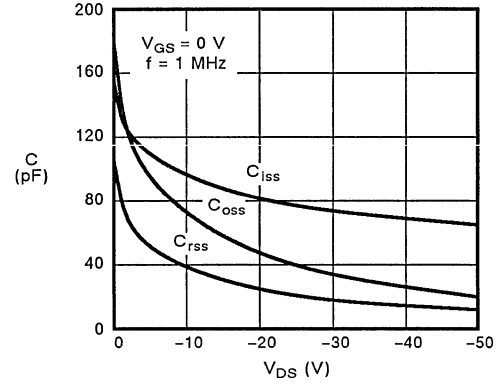
TYPICAL CHARACTERISTICS

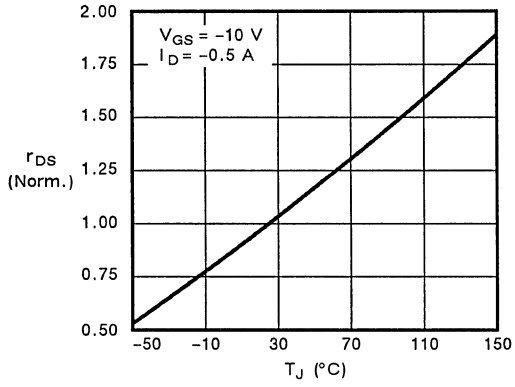
Transconductance



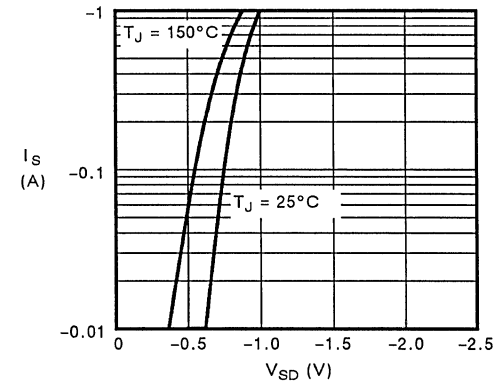
Capacitance



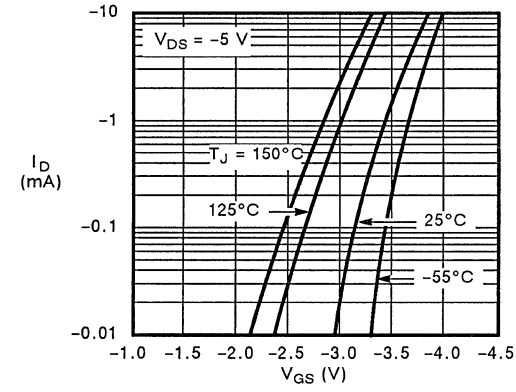
On-Resistance vs. Junction Temperature



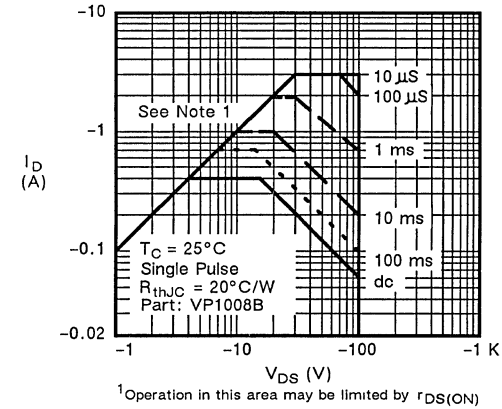
Source-Drain Diode Forward Voltage



Threshold Region



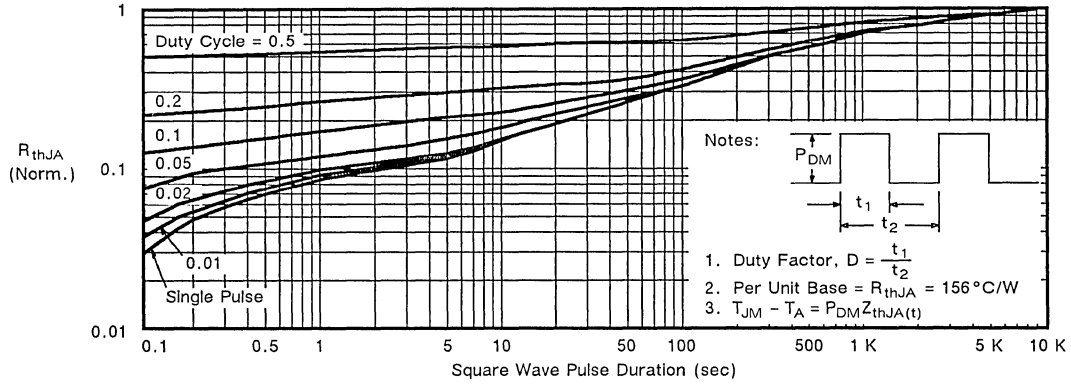
Safe Operating Area



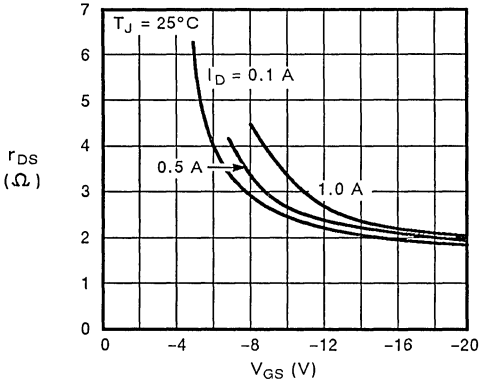
[1]Operation in this area may be limited by $r_{DS(ON)}$

TYPICAL CHARACTERISTICS

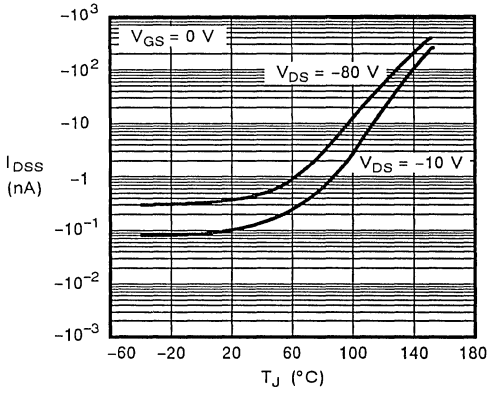
Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



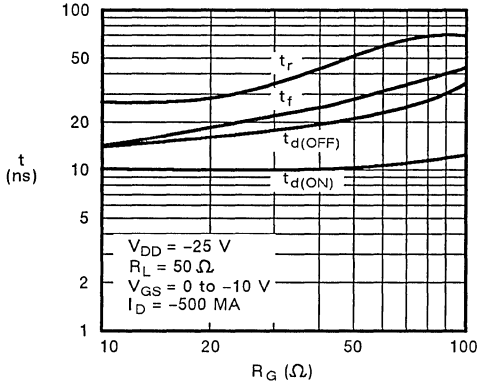
On-Resistance vs. Gate to Source Voltage



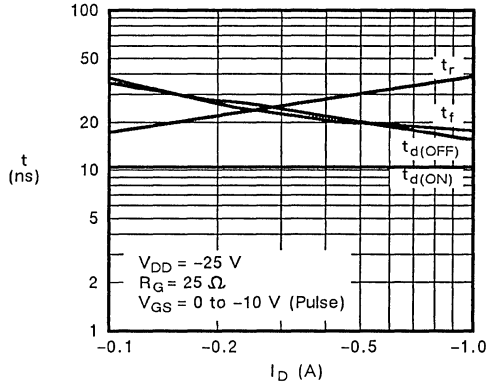
Off State Current



Drive Resistance Effects on Switching



Load Condition Effects on Switching



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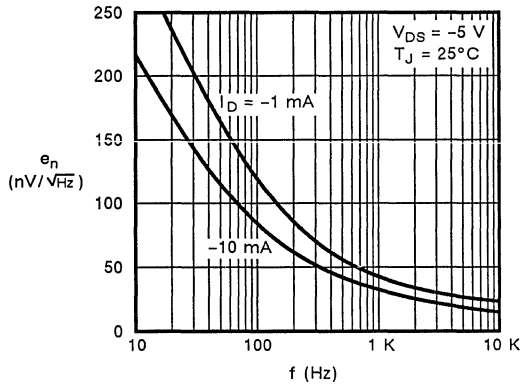
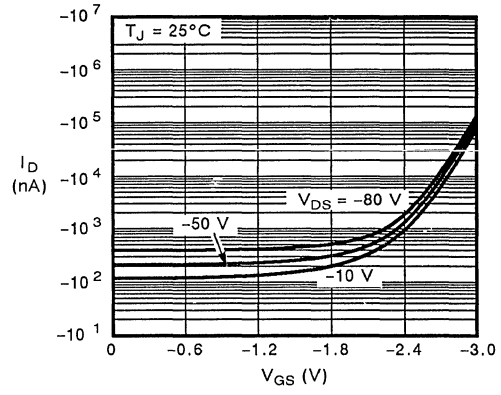
TYPICAL CHARACTERISTICS

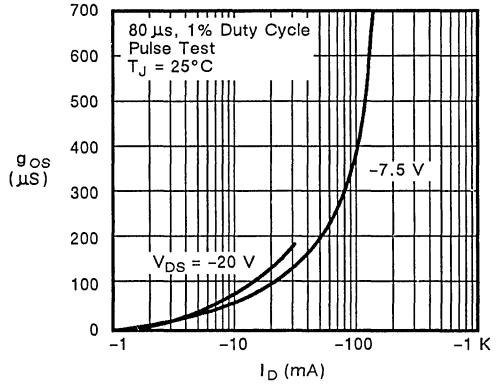
Equivalent Input Noise Voltage vs. Frequency



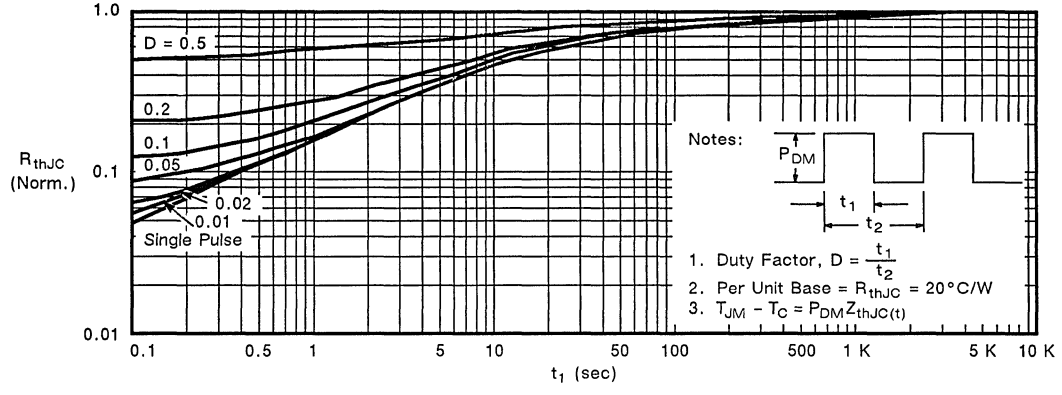
Body Drain Leakage Current



Output Conductance vs. Drain Current



Transient Thermal Response (TO-205AD)



P-Channel Enhancement-Mode MOSFET

DESIGNED FOR:

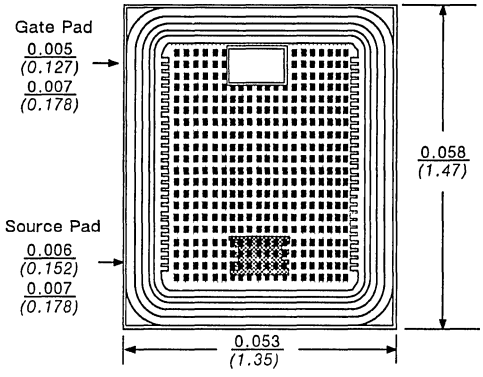
- Switching
- Amplification

FEATURES

- High Breakdown > 240 V
- Low $r_{DS(on)}$ < 10 Ω

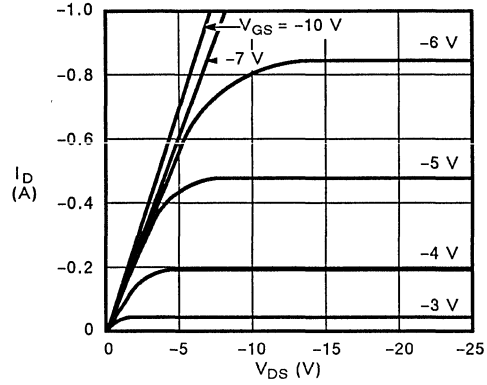
TYPE	PACKAGE	DEVICE
Single	TO-205AD	• VP2410B
	TO-92	• VP2410L BS208
	Chip	• Available as above specifications

GEOMETRY DIAGRAM

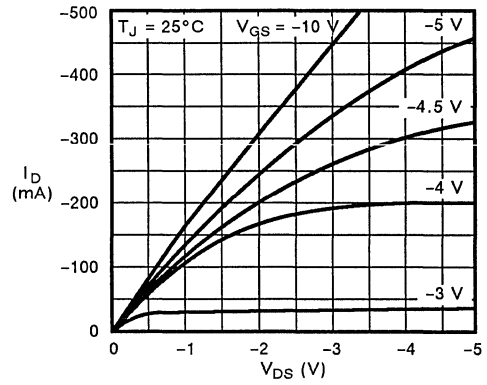


TYPICAL CHARACTERISTICS

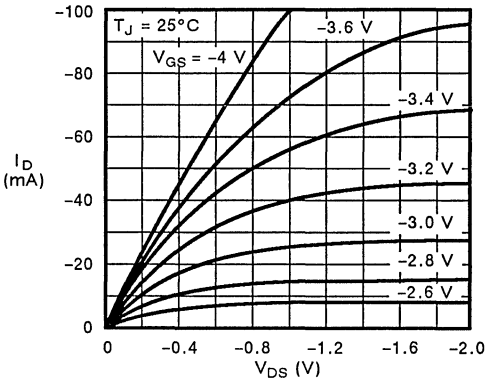
Output Characteristics



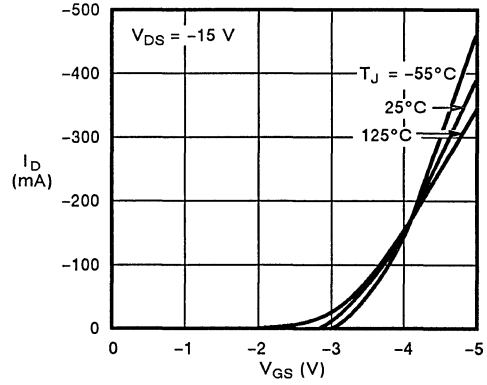
Ohmic Region Characteristics



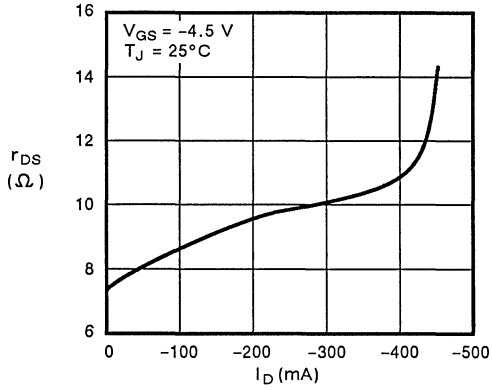
Output Characteristics for Low Gate Drive



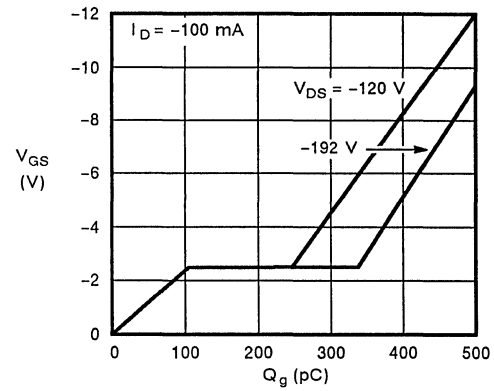
Transfer Characteristics



On-Resistance

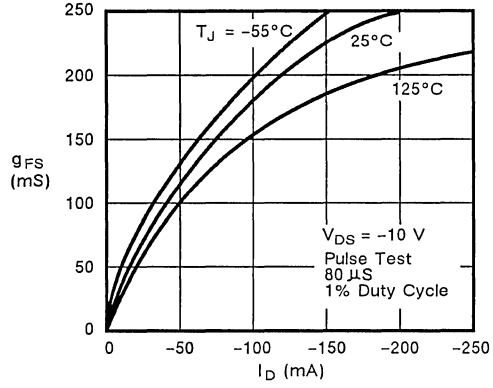


Gate Charge

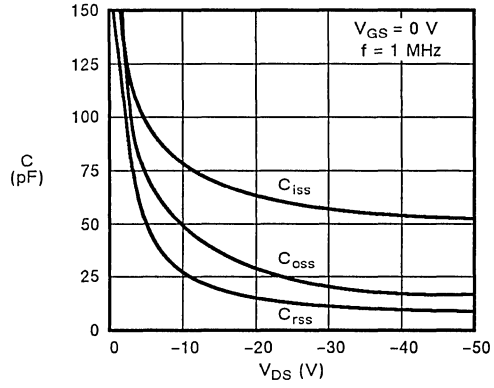


TYPICAL CHARACTERISTICS

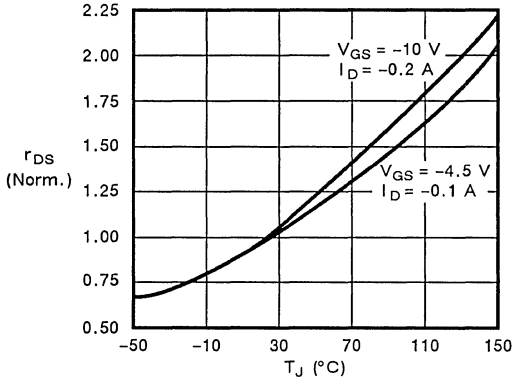
Transconductance



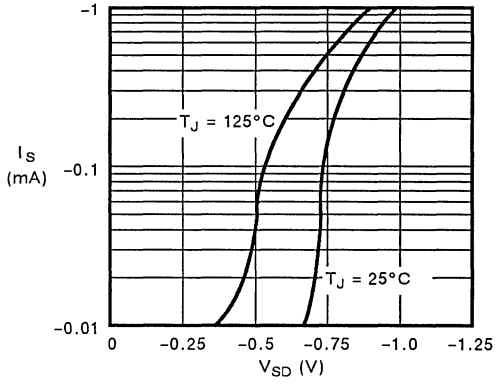
Capacitance



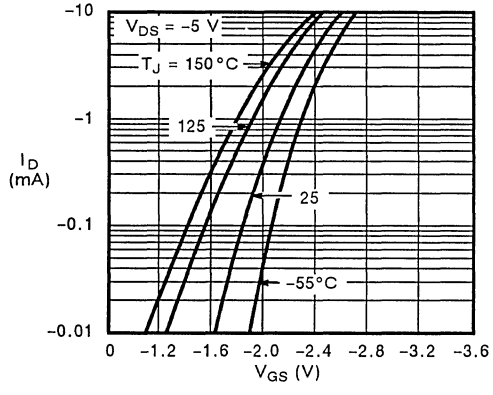
On-Resistance vs. Junction Temperature



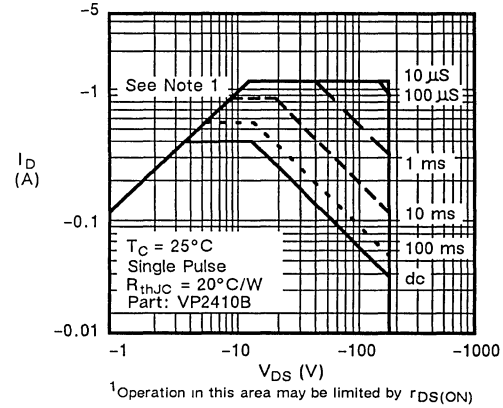
Source-Drain Diode Forward Voltage



Threshold Region



Safe Operating Area

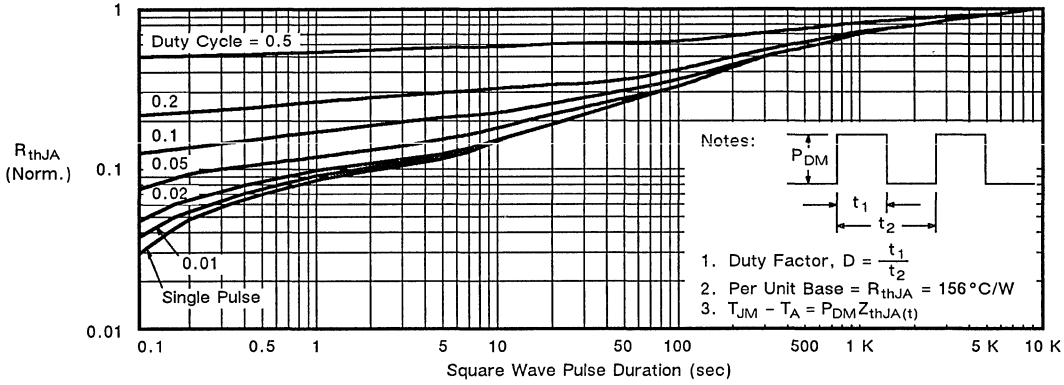


[1]Operation in this area may be limited by $r_{DS(ON)}$

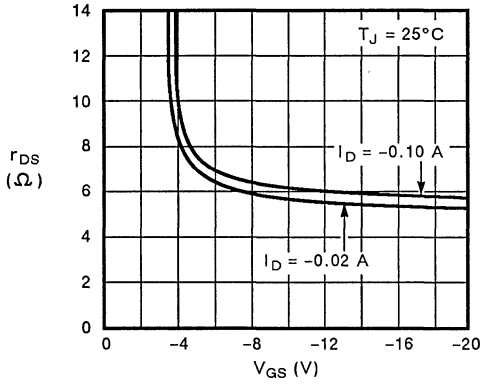
7

TYPICAL CHARACTERISTICS

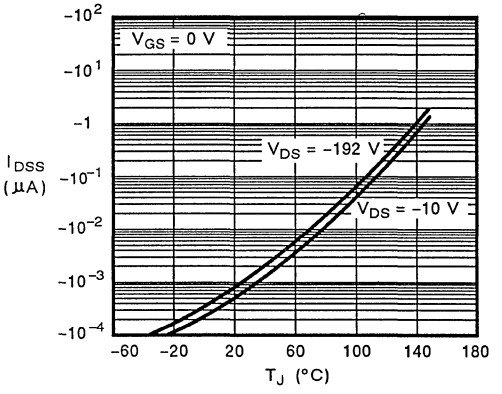
Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



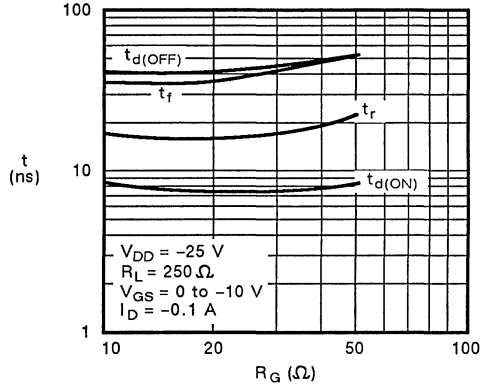
On-Resistance vs. Gate to Source Voltage



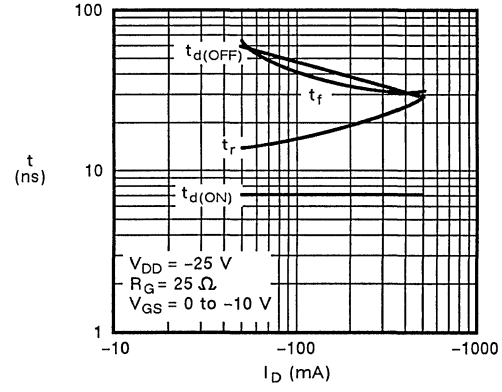
Off State Current



Drive Resistance Effects on Switching

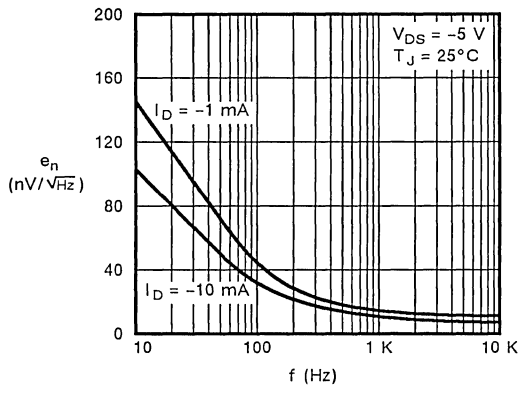


Load Condition Effects on Switching

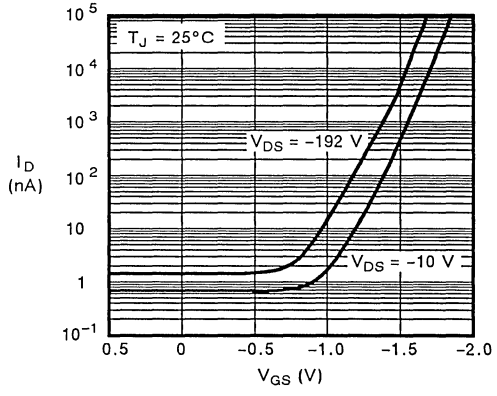


TYPICAL CHARACTERISTICS

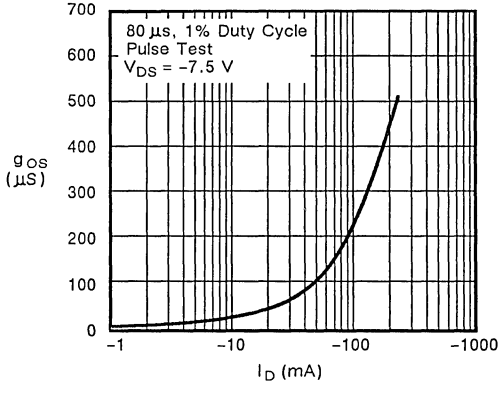
Equivalent Input Noise Voltage vs. Frequency



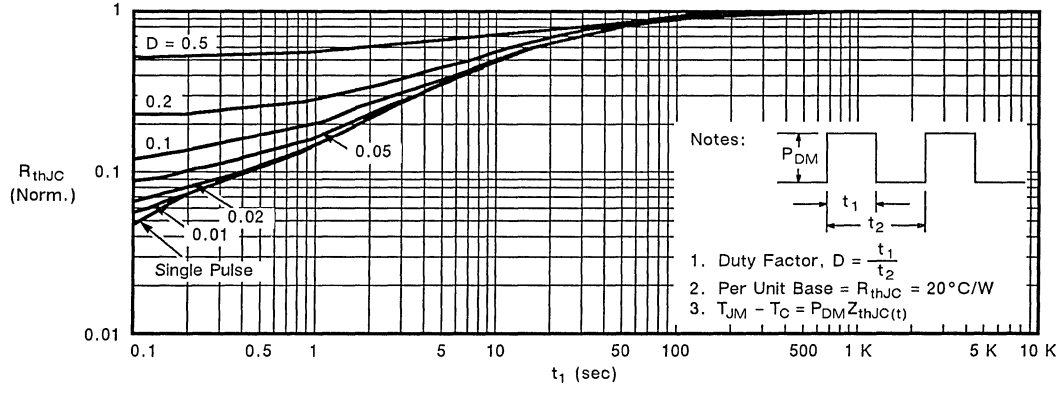
Body Drain Leakage Current



Output Conductance vs. Drain Current



Transient Thermal Response (TO-205AD)



7

Siliconix incorporated

P-Channel Enhancement-Mode MOSFET

DESIGNED FOR:

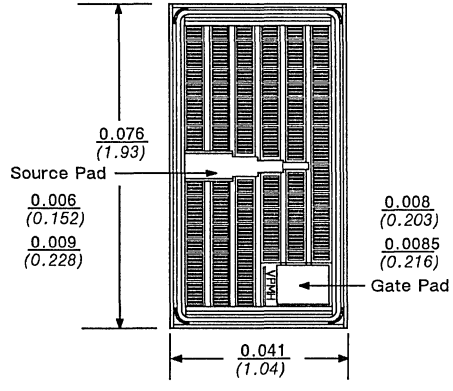
- Switching
- Amplification

FEATURES

- High Speed
- Low $r_{DS(on)}$ < 2.5 Ω

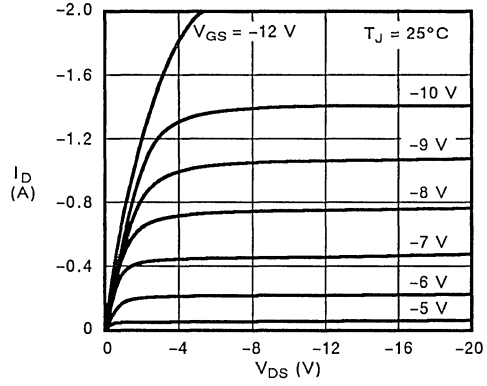
TYPE	PACKAGE	DEVICE
Single	TO-205AD	• VP0300B
	TO-92	• VP0300L
	TO-237	• VP0300M
Quad	14-Pin Plastic	• VQ2001J
	14-Pin Dual-In-Line	• VQ2001P
	Chip	• Available as above specifications

GEOMETRY DIAGRAM

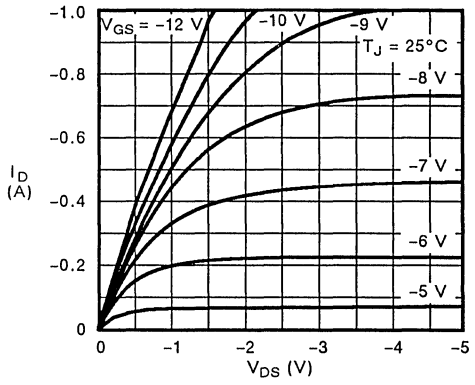


TYPICAL CHARACTERISTICS

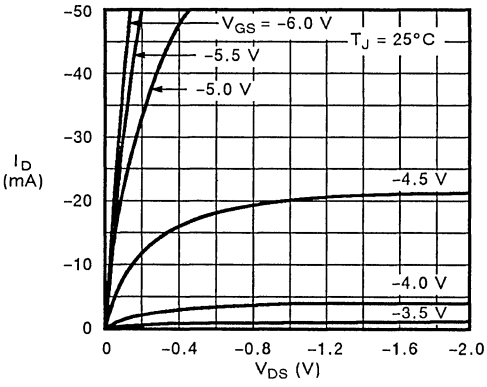
Output Characteristics



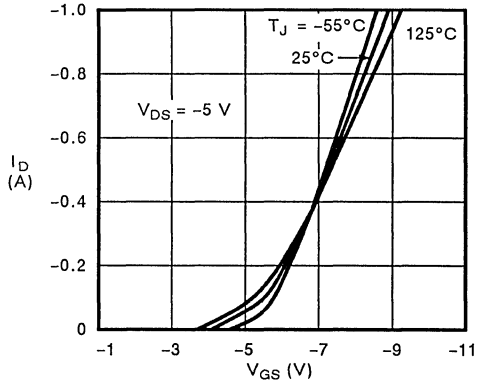
Ohmic Region Characteristics



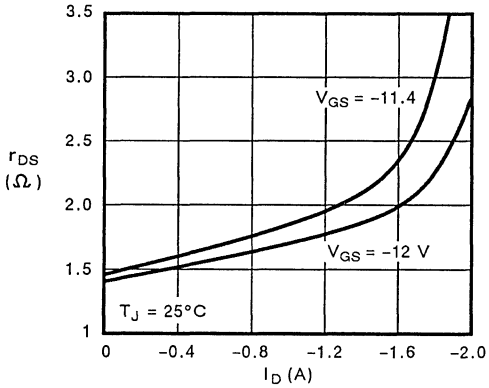
Output Characteristics for Low Gate Drive



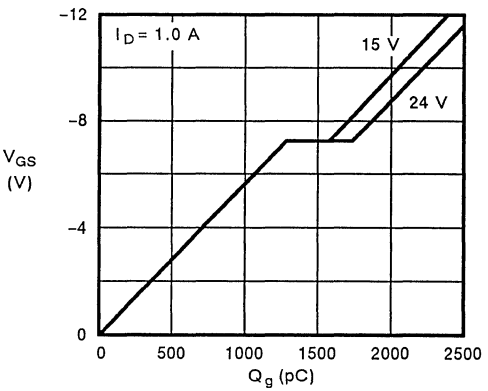
Transfer Characteristics



On-Resistance



Gate Charge



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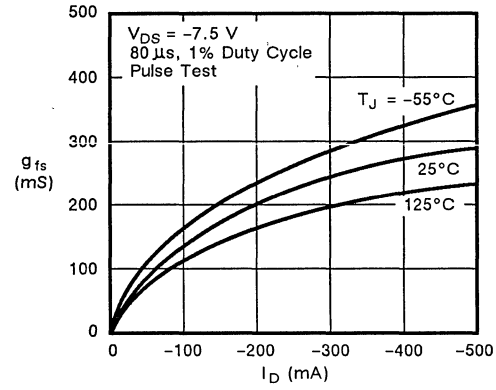
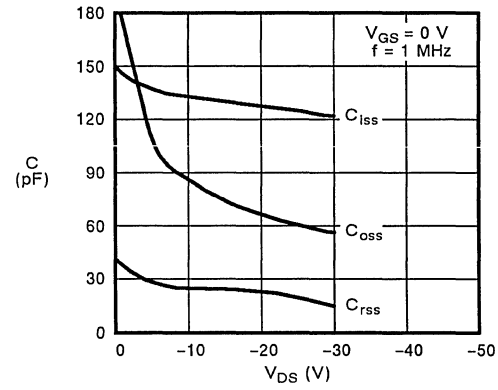
TYPICAL CHARACTERISTICS

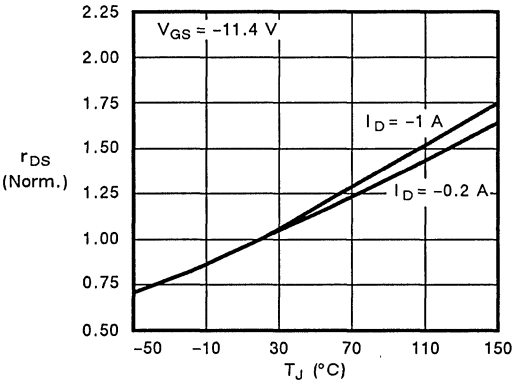
Transconductance



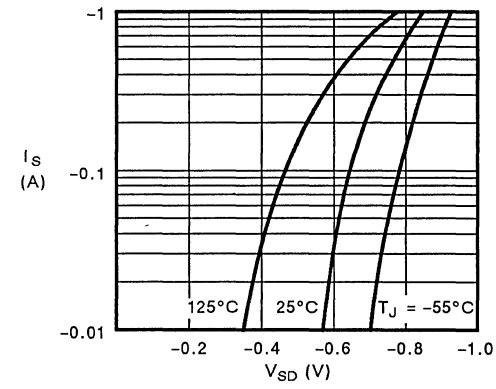
Capacitance



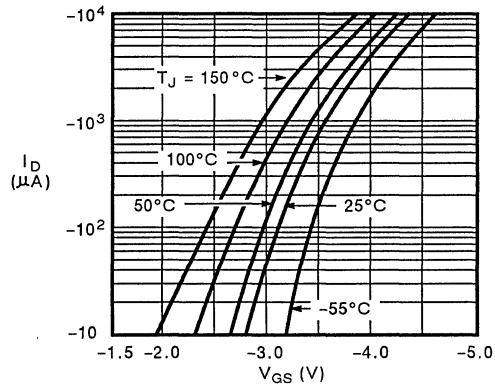
On-Resistance vs. Junction Temperature



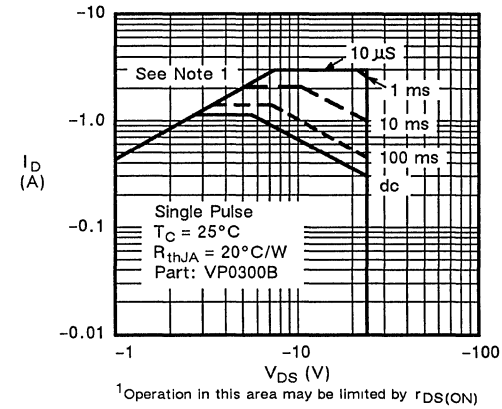
Source-Drain Diode Forward Voltage



Threshold Region



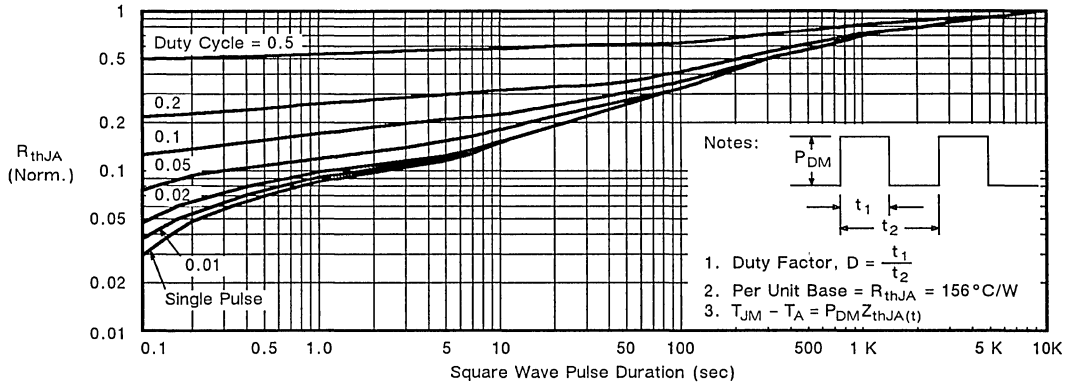
Safe Operating Area



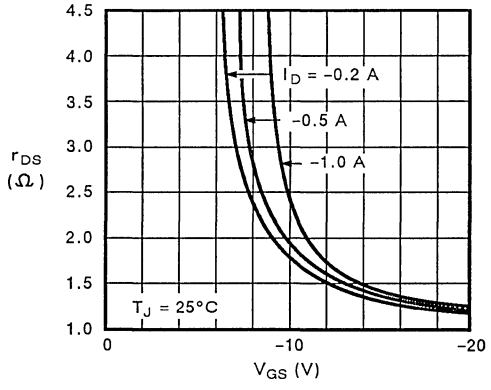
[1]Operation in this area may be limited by $r_{DS(ON)}$

TYPICAL CHARACTERISTICS

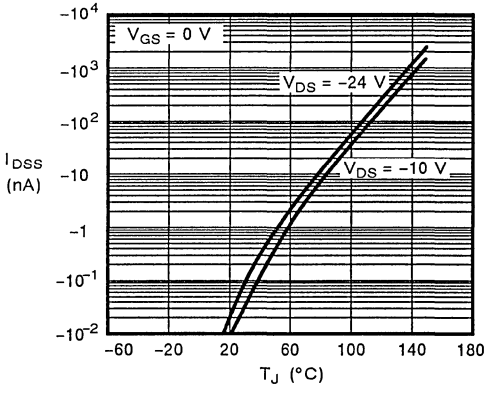
Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



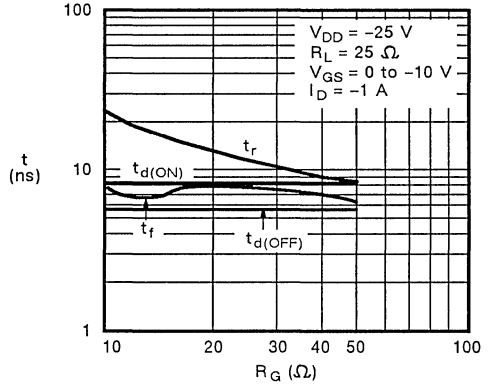
On-Resistance vs. Gate to Source Voltage



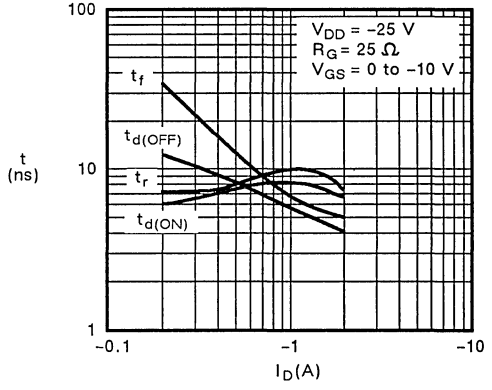
Off-State Current



Drive Resistance Effects on Switching



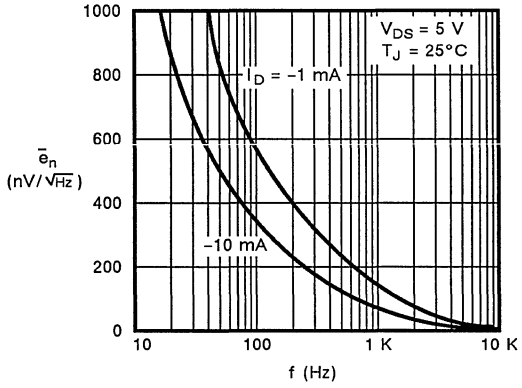
Load Condition Effects on Switching



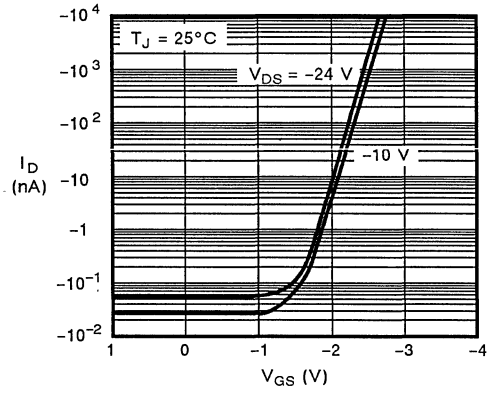
7

TYPICAL CHARACTERISTICS

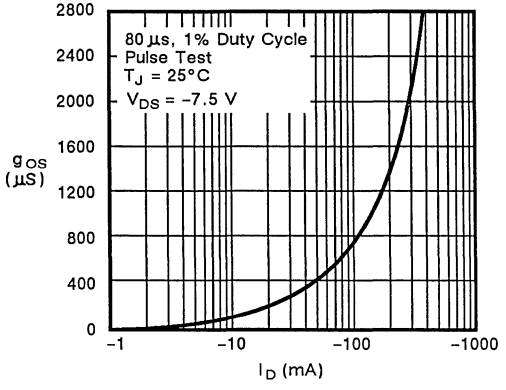
Equivalent Input Noise Voltage vs. Frequency



Body Drain Leakage Current



Output Conductance vs. Drain Current



N-Channel Enhancement-Mode MOSFET Protection Diode

DESIGNED FOR:

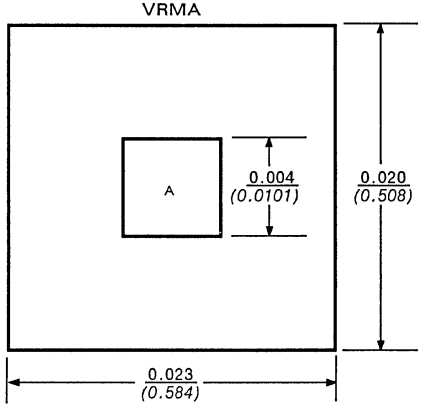
- Limiting Current
- Voltage Protection
- Voltage Decoupling

FEATURES

- Series Element
- Two Terminals
- High Breakdown > 240 V (JR240V)
- Low Cost, Simple to Use

TYPE	PACKAGE	DEVICE
Single	TO-92	• JR135V, JR170V JR200V, JR220V, JR240V
	Chip	• Available as above specifications

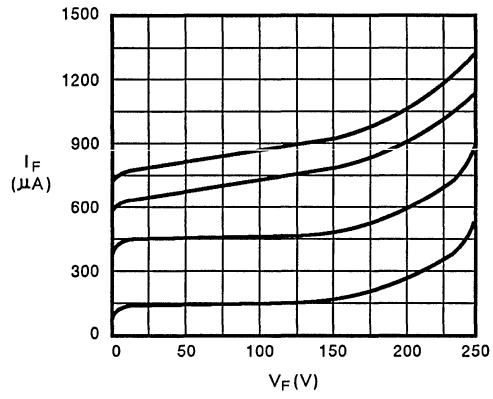
GEOMETRY DIAGRAM



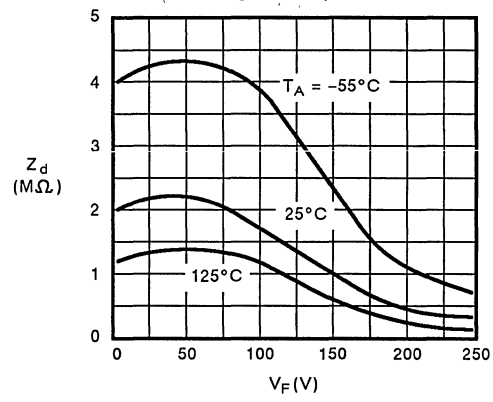
Cathode is backside contact

TYPICAL CHARACTERISTICS

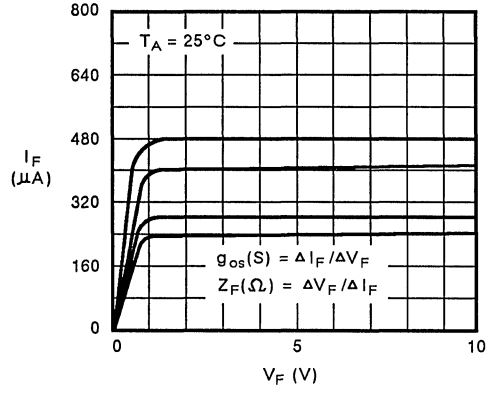
Output Characteristics



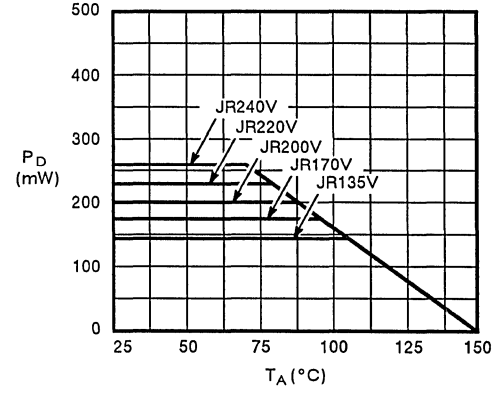
Dynamic Impedance vs. Forward Voltage at Temperature



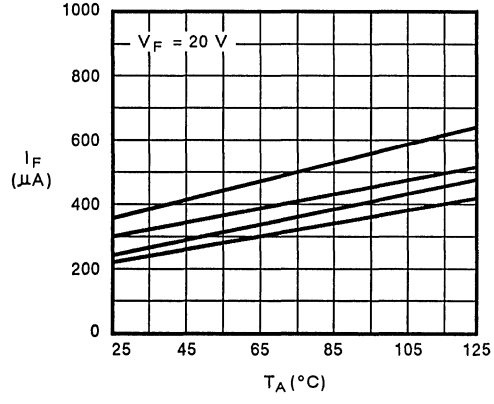
Current vs. Forward Voltage



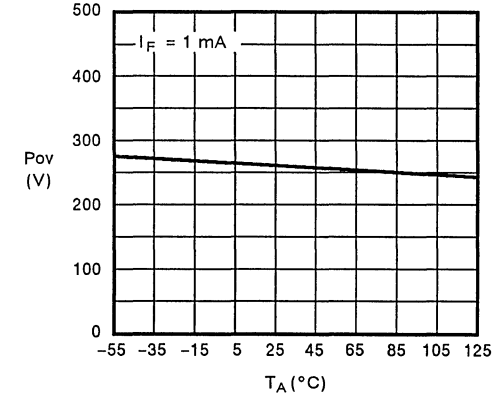
Dissipation Derating Curve

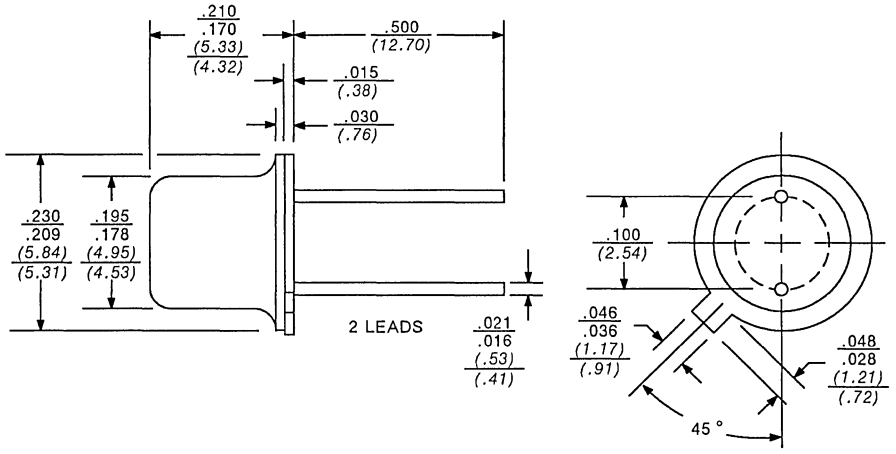


I_F vs. Temperature

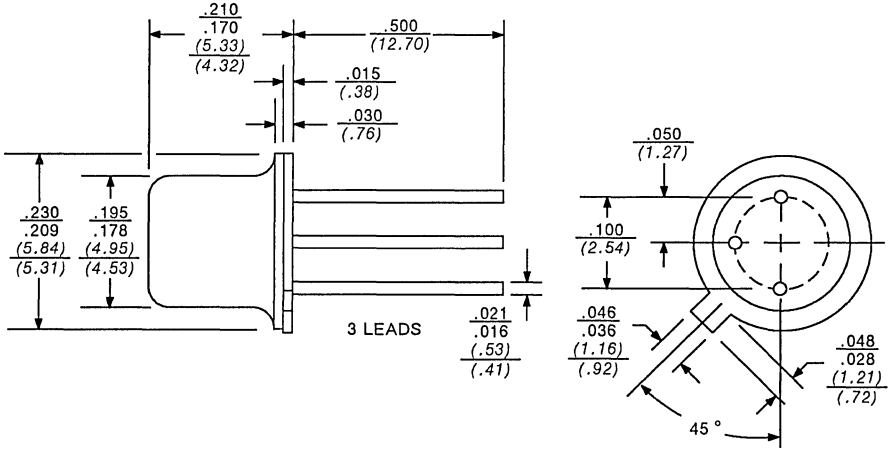


Peak Operating Voltage vs. Temperature





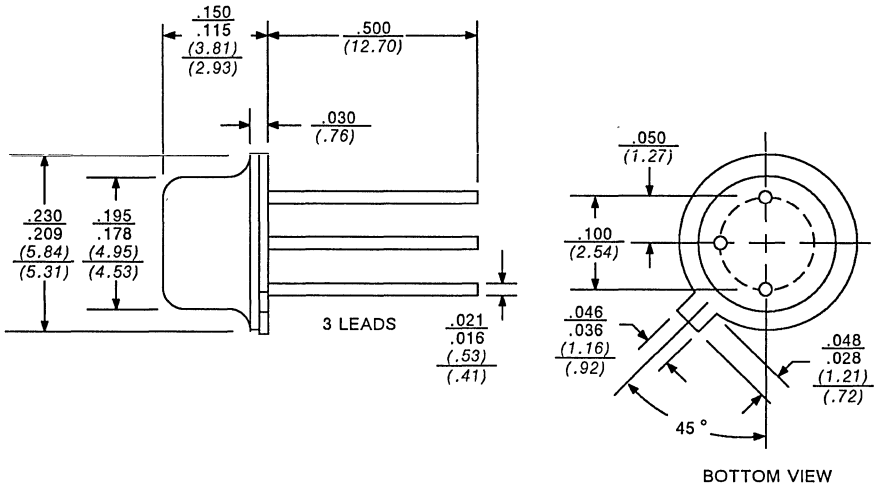
TO-18
(2-PIN)



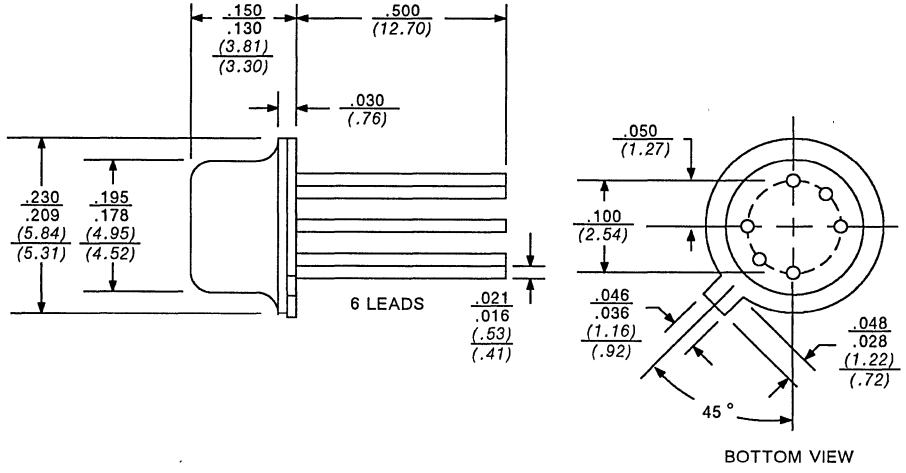
TO-206AA
(TO-18)

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

8

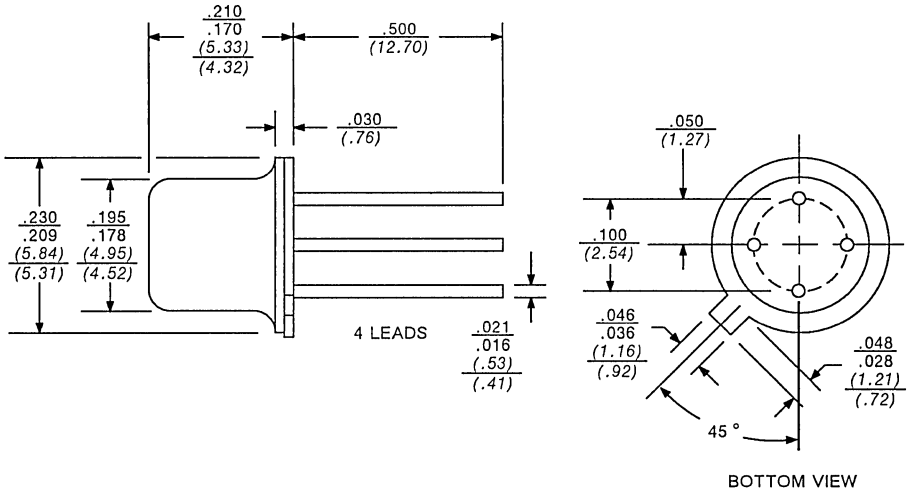


TO-206AC
(TO-52)

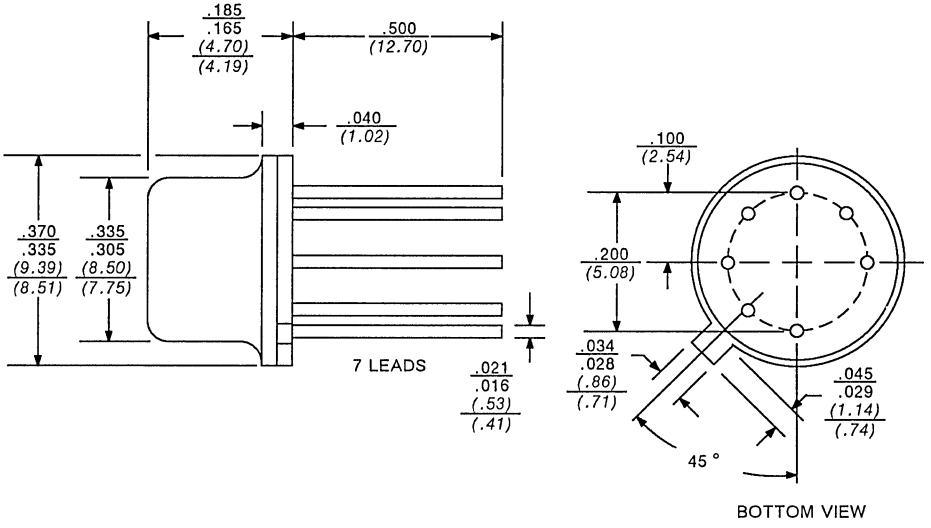


TO-71

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)



TO-206AF
(TO-72)

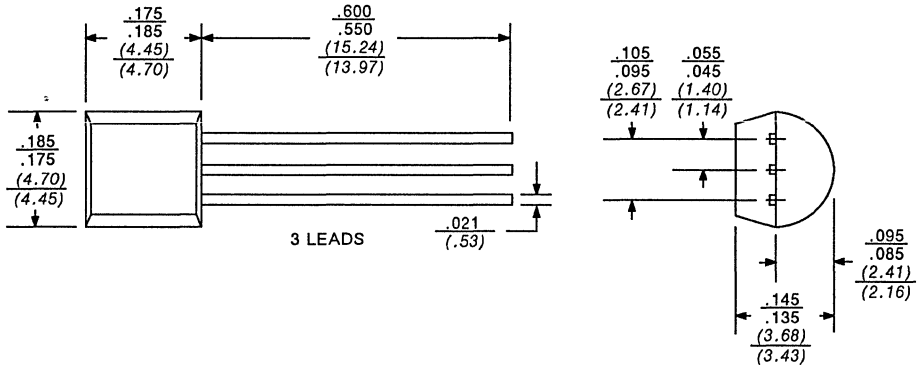


MO-002AG
(TO-78)

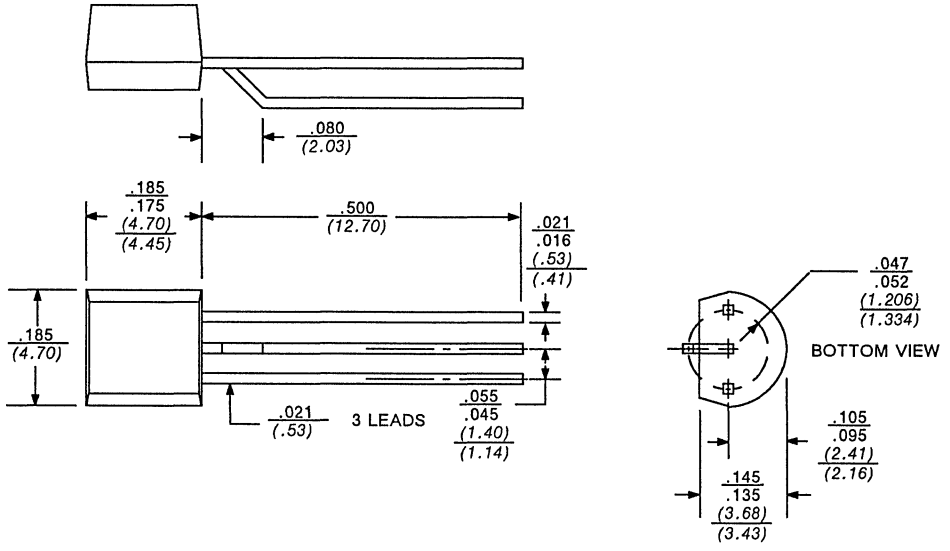
ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

8

PACKAGE OUTLINES

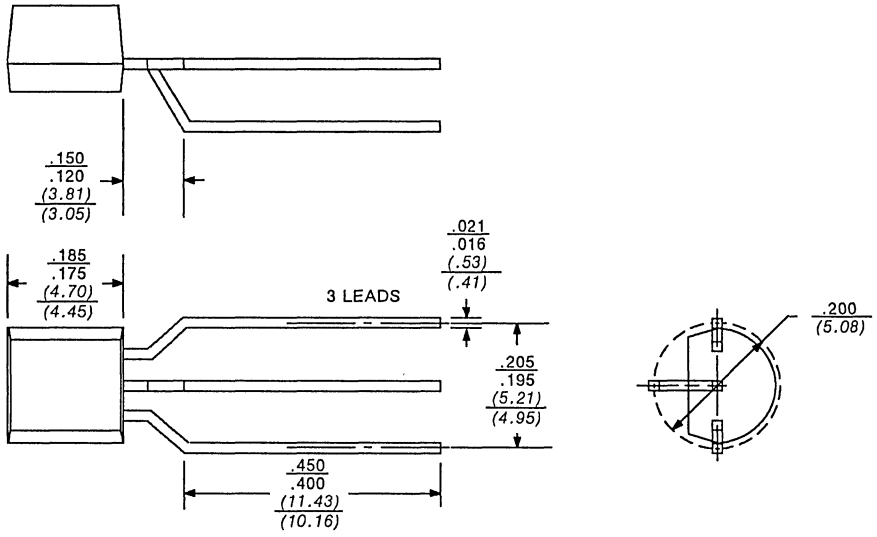


TO-226AA
(TO-92)

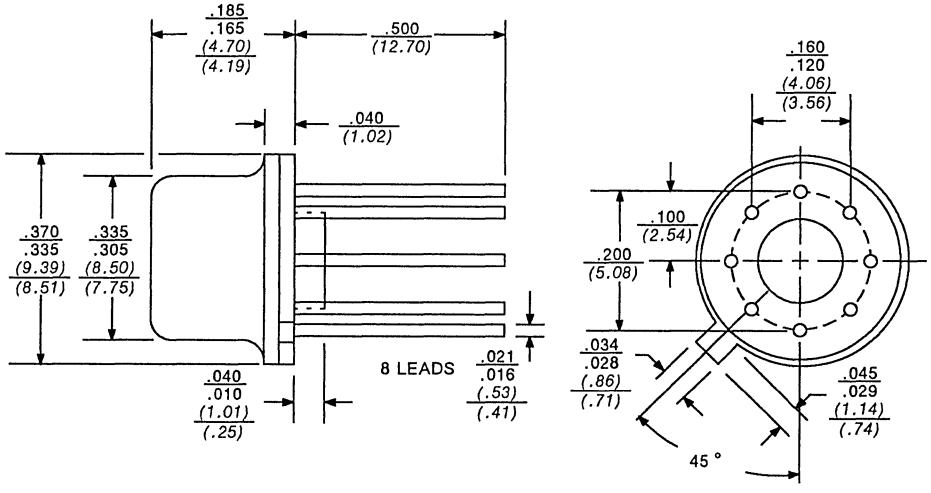


TO-226AA
(TO-92 LEAD FORM)
-18

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)



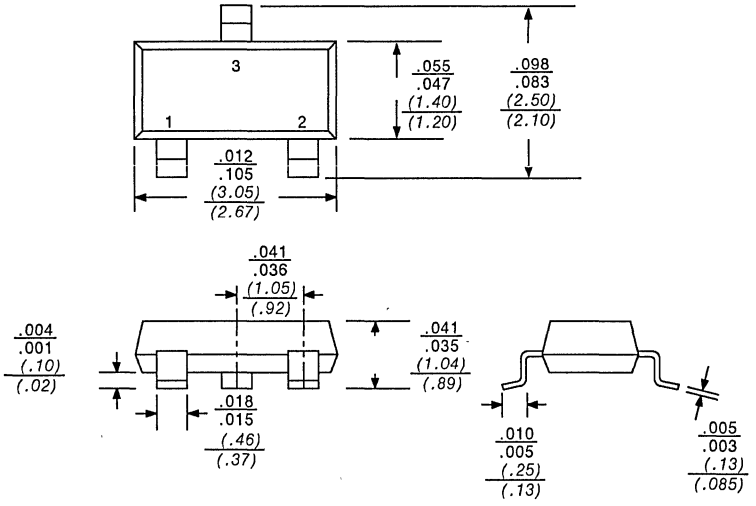
TO-226AA
TO-92 DEVICE to TO-5 PIN CIRCLE



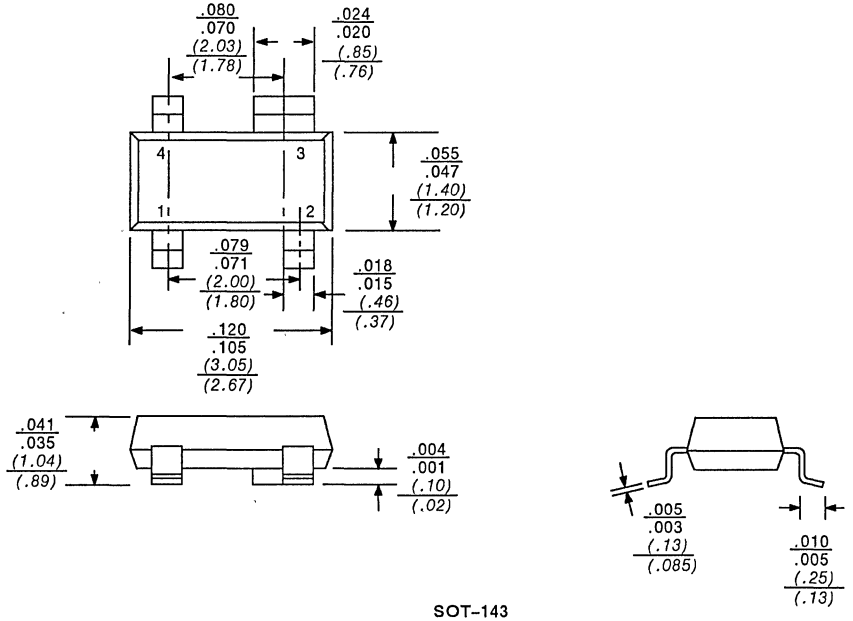
MO-002AK
(TO-99)

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

8

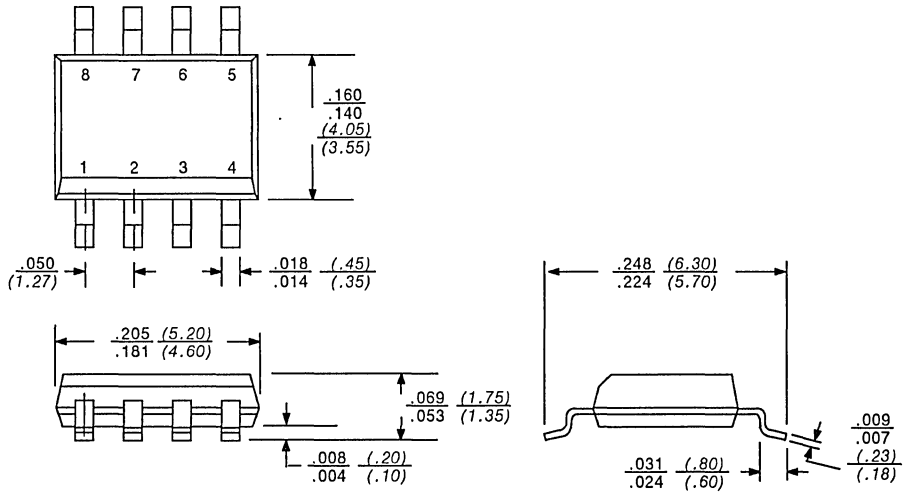


SOT-23

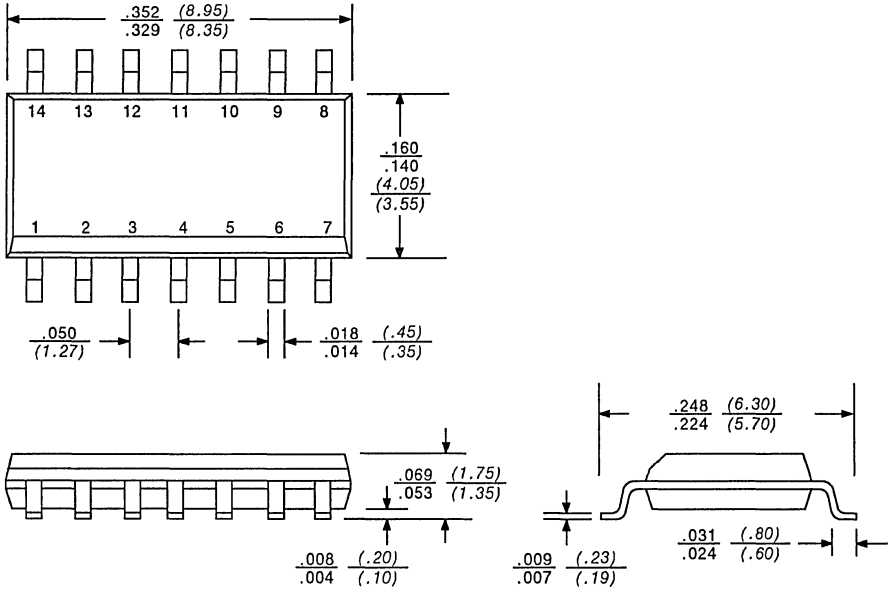


SOT-143

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)



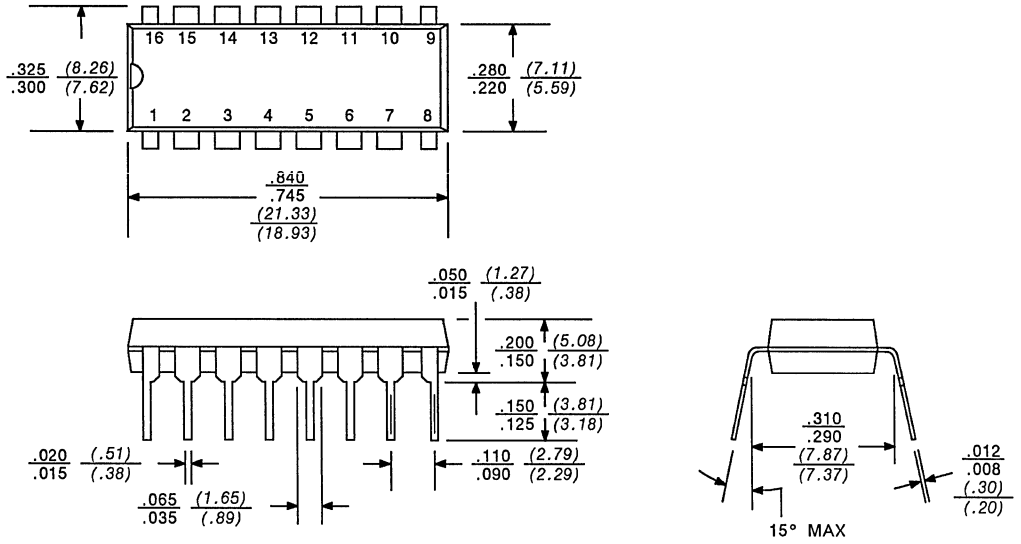
8-LEAD SOIC



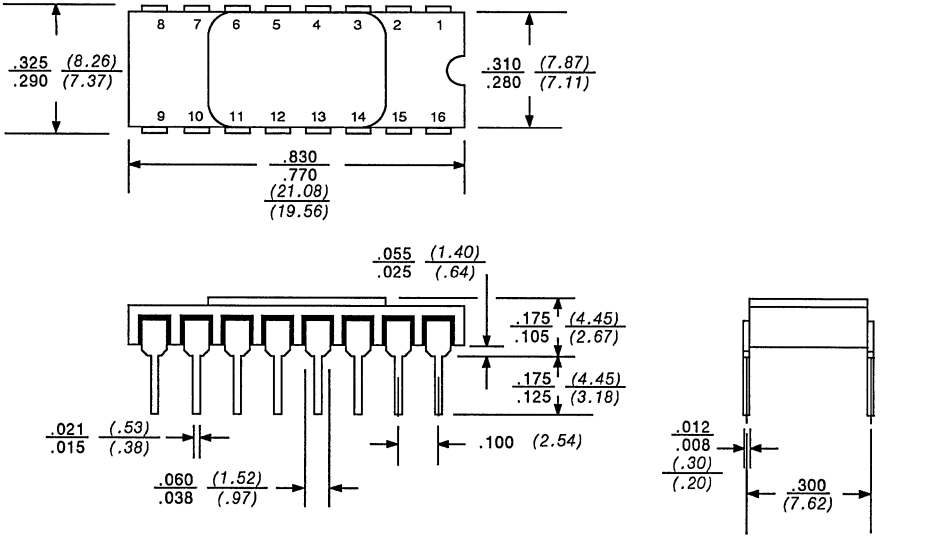
14-LEAD (NARROW) SOIC

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

PACKAGE OUTLINES

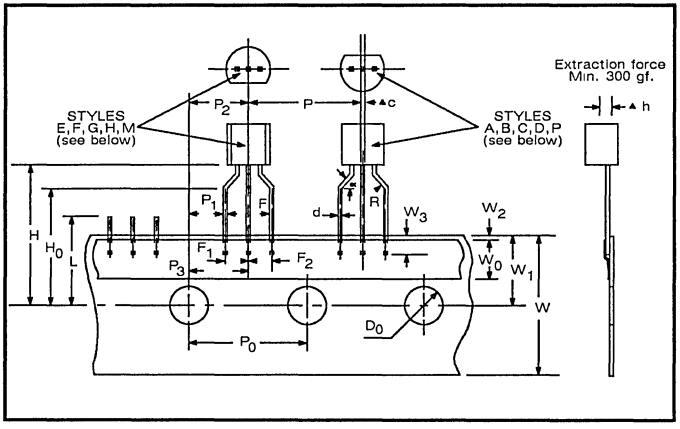


16-LEAD DUAL IN LINE PACKAGE
(PLASTIC)



16-LEAD DUAL IN LINE PACKAGE
(SIDE BRAZE)

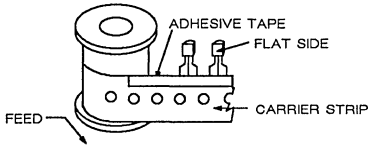
ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)



P	12.7 ± 1.0	F	$5 \pm^{0.8}_{0.2}$
P_0	12.7 ± 0.2	$F_1 - F_2$	± 0.3
P_1	3.85 ± 0.5	D_0	4 ± 0.2
P_2	6.35 ± 0.5	t	1.4
P_3	6.35	▲h	0 ± 1
W	$18 \pm^{0.5}_{0.5}$	d	$0.50 \pm^{0.6}_{0.5}$ dia.
W_0	6 ± 3	R	0.8
W_1	9 ± 0.5	∝	45° - 60°
W_2	MAX. 0.5	L	MIN. 11
W_3	MIN. 4.5	▲c	0 ± 0.5
H	$18.5 \pm^{3.0}_{0.75}$		

OPTION 1

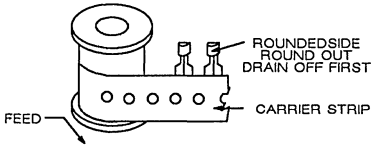
STYLE IS A PREFERED STYLE



STANDARD TAPE & REEL FLAT OUT GATE OFF FIRST

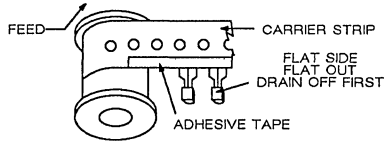
OPTION 3

STYLE A IS PREFERED



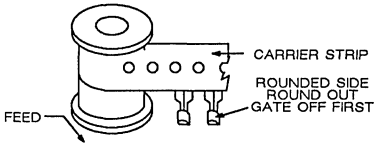
ROUNDED SIDE TRANSISTER AND ADHESIVE TAPE NOT VISIBLE

OPTION 2



FLAT SIDE OF TRANSISTER AND ADHESIVE TAPE VISIBLE

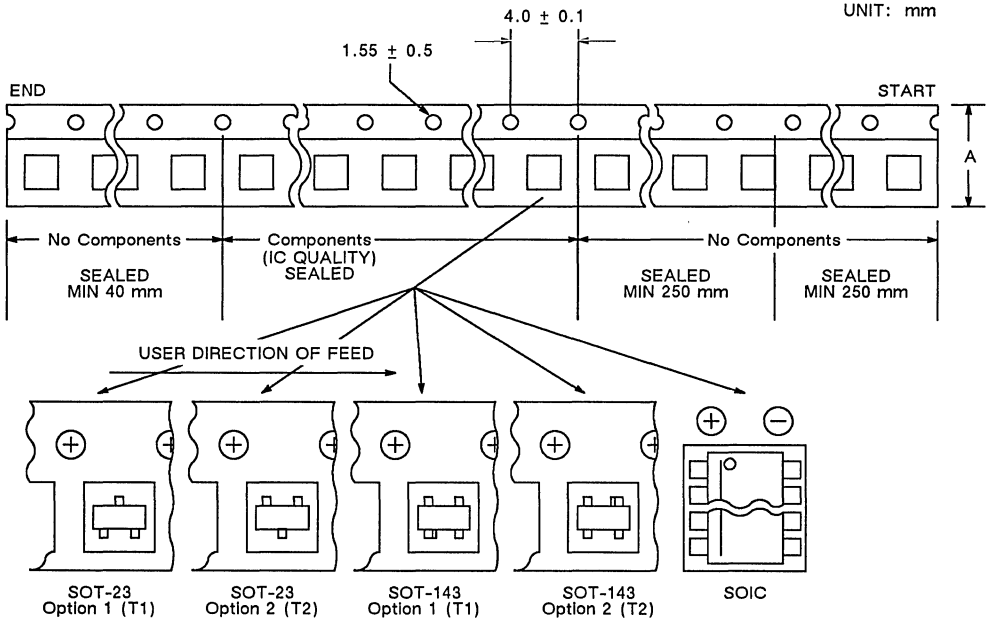
OPTION 4

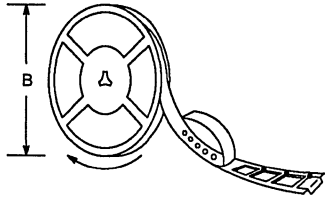


ROUNDED SIDE TRANSISTER AND ADHESIVE TAPE NOT VISIBLE

TO-92 TAPING SPECIFICATIONS AND WINDING STYLES

(ALL DIMENSIONS IN MILLIMETERS)





	A	B	C
SOT-23/SOT-143	8.0 ± 0.3 MIN	178 MIN	2500 EA
SOIC-8	12.0 ± 0.3	330	2500 EA
SOIC-14/SOIC-16	16.0 ± 0.3	330	2500 EA

SOT-23/143/SOIC TAPE AND REEL

AN INTRODUCTION TO FETS

INTRODUCTION

The basic principle of the field-effect transistor (FET) has been known since J. E. Lilenfeld's patent of 1925. The theoretical description of a FET made by Schockley in 1952 paved the way for development of a classic electronic device which provides the designer the means to accomplish nearly every circuit function. At one time, the field-effect transistor was known as a "unipolar" transistor. The term refers to the fact that current is transported by carriers of one polarity (majority), whereas in the conventional bipolar transistor carriers of both polarities (majority and minority) are involved.

This Application Note provides an insight into the nature of the FET, and touches briefly on its basic characteristics, terminology, parameters, and typical applications.

The following list of FET applications indicates the versatility of the FET family:

Amplifiers

- Small Signal
- Low Distortion
- High Gain
- Low Noise
- Selective
- D.C.
- High-Frequency

Switches

- Chopper-type
- Analog Gate
- Commutator

Protection Diodes

- Low-Leakage

Current Limiters

Voltage-Controlled Resistors

Mixers

Oscillators

This very wide range of FET applications by no means implies that the device will replace the more widely-known bipolar transistor in every case. The simple fact is that FET characteristics – which are very different from those of bipolar devices – can often make possible the design of technically superior (and sometimes cheaper) circuits.

The family tree of FET devices (Figure 1) may be divided into two main branches, Junction FETs (JFETs) and Insulated Gate FETs (or MOSFETs, metal-oxide-silicon field-effect transistors). Junction FETs are inherently depletion-mode devices, and are available in both n- and p-channel configurations. MOSFETs are available in both enhancement and depletion modes, and also exist as both n- and p-channel devices. The two main FET groups depend on different phenomena for their operation, and will be discussed separately.

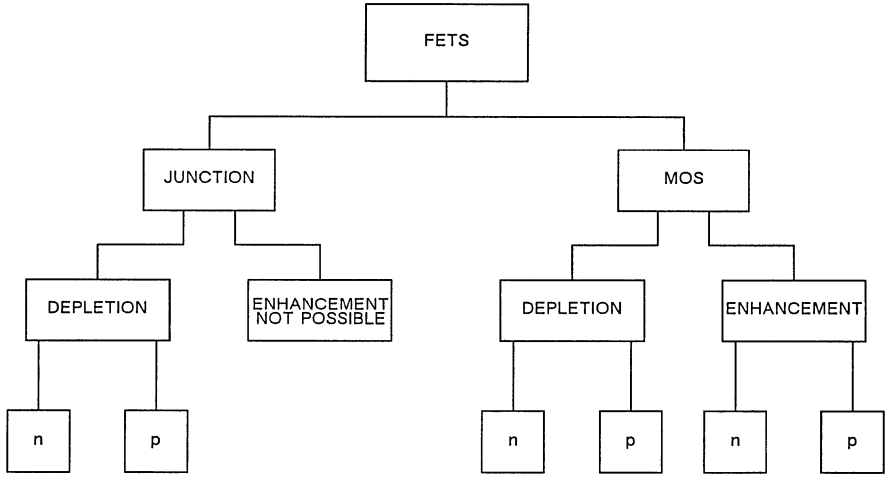


Figure 1. FET Family Tree

Junction FETs

In its most elementary form, this transistor consists of a piece of high-resistivity semiconductor material (usually silicon) which constitutes a channel for the majority carrier flow. The magnitude of this current is controlled by a voltage applied to a gate, which is a reverse-biased pn junction formed along the channel. Implicit in this description is the fundamental difference betwee JFET and bipolar devices: when the JFET junction is reverse-biased the gate current is practically zero, whereas the base current of the bipolar transistor is always some value greater than zero. The JFET is a high-input resistance device, while the input resistance of the bipolar transistor is comparatively low. If the channel is doped with a donor impurity, n-type material is formed and the channel current will consist of electrons. If the channel is doped with an acceptor impurity, p-type material will be formed and the channel current will consist of holes. N-channel devices have greater conductivity than p-channel types, since electrons have higher mobility than do holes; thus n-channel JFETs tend to be more efficient conductors than their p-channel counterparts.

Junction FETs are particularly suited to manufacture by modern planar epitaxial processes. Figure 2 shows this process in an idealized manner. First, n-type silicon is deposited epitaxially (single-crystal condensation surface) onto monocrystalline p-type silicon, so that crystal integrity is maintained. Then, a layer of silicon dioxide is grown on the surface of the n-type layer, and the surface is etched so that an acceptor-type impurity can be diffused through into the silicon. The resulting cross-section is shown in Figure 2C, and demonstrates how a p-type annulus has been formed in the layer on n-type silicon. Figure 2D shows how a further sequence of oxide growth, etching, and diffusion can produce a channel of n-type material within the substrate.

In addition to the channel material, a JFET contains two ohmic (non-rectifying) contacts: the source and the drain. These are shown in Figure 2E. Since a symmetrical geometry is shown in the idealized JFET chip, it is immaterial which contact is called the source and which is called the drain; the JFET will conduct current equally well in either direction and the source and drain leads are usually interchangeable.

(For certain JFET applications, such as amplifiers, an asymmetrical geometry is preferred for lower capacitance and improved frequency response. In these cases, the source and drain leads should not be interchanged).

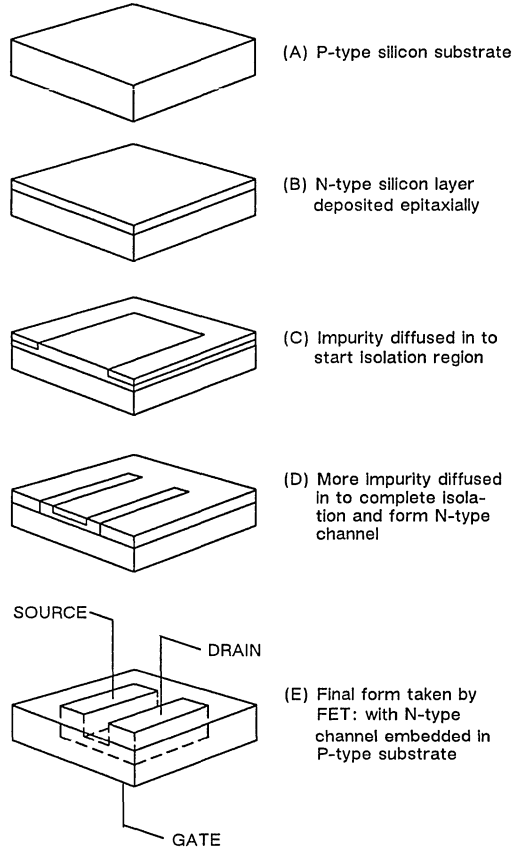


Figure 2. Idealized Manufacture of an N-Channel Junction FET

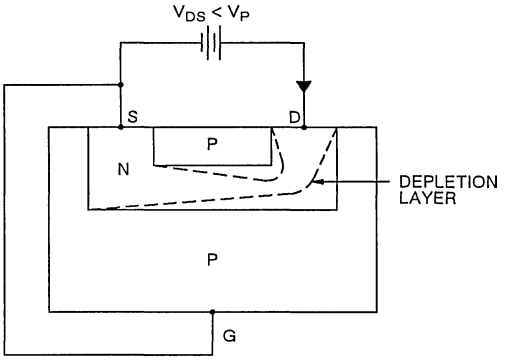
Figure 2E also shows how the n-channel is embedded in the p-type silicon substrate, so that the gate above the channel becomes part of this substrate. Figure 3 shows how the JFET functions. If the gate is connected to the source, then the applied voltage (V_{DS}) will appear between the gate and the drain. Since the pn junction is reverse-biased, little current will flow in the gate connection. The potential gradient established will form a depletion layer, where almost all the electrons present in the n-type channel will be swept away. The most depleted portion is in

the high field between the gate and the drain, and the least-depleted area is between the gate and the source. Because the flow of current along the channel from the (positive) drain to the (negative) source is really a flow of free electrons from source to drain in the n-type silicon, the magnitude of this current will fall as more silicon becomes depleted of free electrons. There is a limit to the drain current (I_D) which increased V_{DS} can drive through the channel. This limiting current is known as I_{DSS} (Drain-to-Source current with the gate shorted to the source). Figure 3B shows the almost complete depletion of the channel under these conditions.

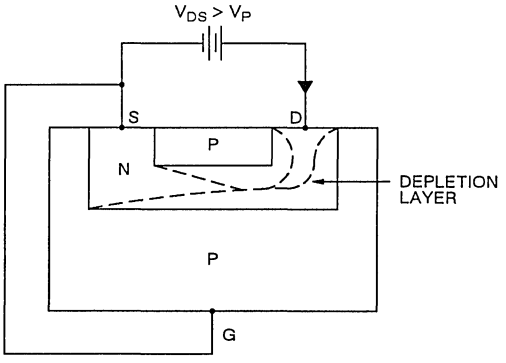
Figure 3C shows the output characteristics of an n-channel JFET with the gate short-circuited to the source. The initial rise in I_D is related to the buildup of the depletion layer as V_{DS} increases. The curve approaches the level of the limiting current I_{DSS} when I_D begins to be pinched off. The physical meaning of this term leads to one definition of pinch-off voltage, V_p, which is the value of V_{DS} at which the maximum I_{DSS} flows.

In Figure 4, consider the case where V_{DS} = 0 and where a negative voltage V_{GS} is applied to the gate. Again, a depletion layer has built up. If a small value of V_{DS} were now applied, this depletion layer would limit the resultant channel current to a value lower than would be the case for V_{GS} = 0. In fact, at a value of $V_{GS} > V_p$ the channel current would be almost entirely cut off. This cutoff voltage is referred to as the gate cutoff voltage, and may be expressed by the symbol V_p or by $V_{GS(off)}$. V_p has been widely used in the past, but $V_{GS(off)}$ is now more commonly accepted since it eliminates the ambiguity between gate cut-off and drain pinch-off. $V_{GS(off)}$ and V_p, strictly speaking are generally equal in magnitude but opposite in polarity.

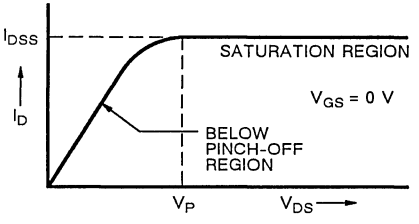
The mechanisms of Figures 3 and 4 react together to provide the family of output characteristics shown in Figure 5A. The area below the pinch-off voltage locus is known as the triode or "below pinch-off" region: the area above pinch-off is often referred to as the pentode or saturation region. JFET behavior in these regions is comparable to that of a power-grid vacuum tube, and for this reason JFETs operating in the saturation region make excellent amplifiers. Note that in the "below pinchoff" region both V_{GS} and V_{DS} control the channel current, while in the saturation region V_{DS} has little effect and V_{GS} essentially controls I_D.



(A) N-channel FET working below saturation (V_{GS} = 0). (Depletion shown only in channel region).



(B) N-channel FET working in saturation region (V_{GS} = 0).



(C) Idealized output characteristic for V_{GS} = 0.

Figure 3.

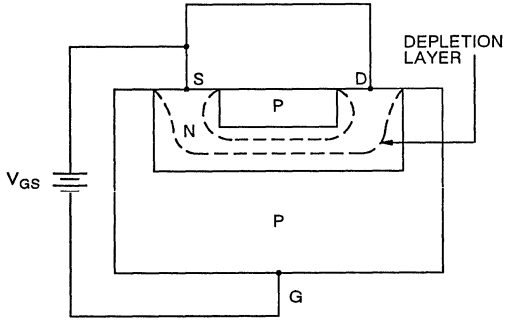
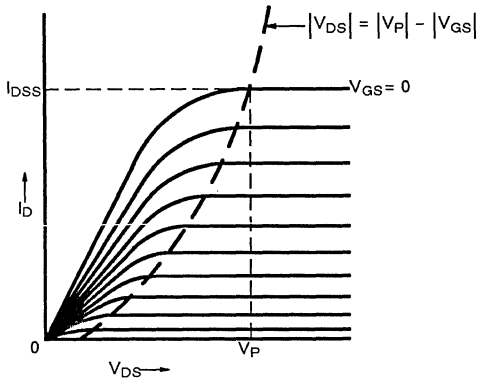
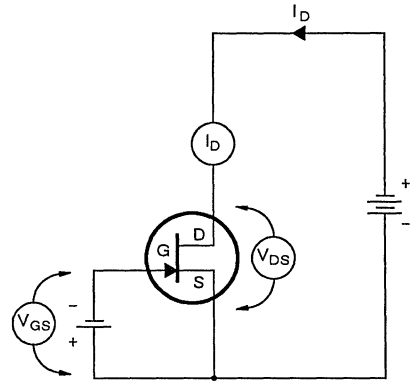


Figure 4. N-Channel FET Showing Depletion Due To Gate-Source Voltage (V_{DS} = 0).



(A) Family of output characteristics for n-channel FET



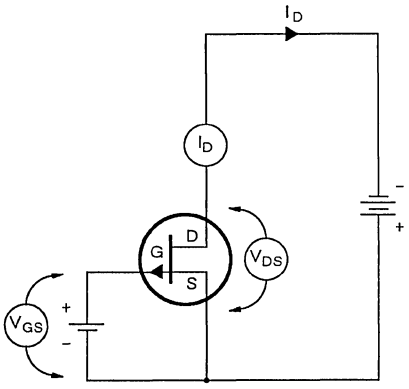
(B) Circuit arrangement for n-channel FET

Figure 5.

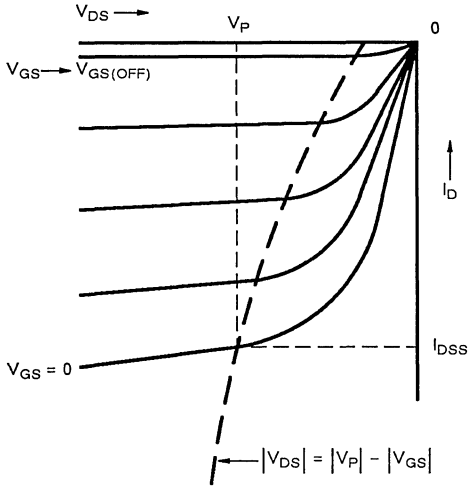
Figure 5B relates the curves in Figure 5A to the actual circuit arrangement, and shows the number of meters which may be connected to display the conditions relevant to any combination of V_{DS} and V_{GS}. Note that the direction of the arrow at the gate gives the direction of current flow for the forward-bias condition of the junction. In practice, however, it is always reverse-biased.

The p-channel JFET works in precisely the same way as does the n-channel JFET. In manufacture, the planar process is essentially reversed, with the acceptor impurity diffused first onto n-type silicon, and the donor impurity diffused later to form a second n-type region and leave a p-type channel. In the p-channel JFET, the channel current is due to hole movement, rather than to electron mobility. Consequently, all the applied polarities are reversed, along with their directions and the direction of current flow. Figure 6A shows the circuit arrangement for a p-channel JFET, and Figure 6B shows the output characteristics of the device. Note that the curves are shown in another quadrant than those of the n-channel JFET, in order to stress the current directions and polarities involved.

In summary, a junction FET consists essentially of a channel of semiconductor material along which a current may flow whose magnitude is a function of two voltages, V_{DS} and V_{GS}. When V_{DS} is greater than V_p, the channel current is controlled largely by V_{GS} alone, because V_{GS} is applied to a reverse-biased junction. The resulting gate current is extremely small.



(A) Circuit Arrangement for p-channel JFET



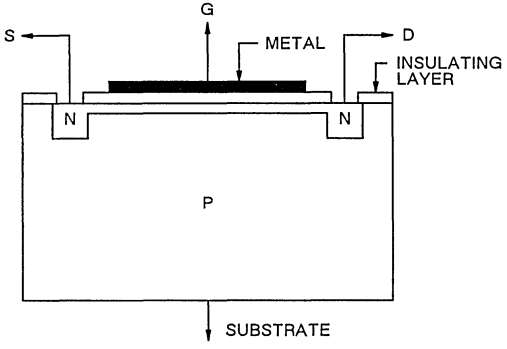
(B) Family of output characteristics for p-channel JFET

Figure 6.

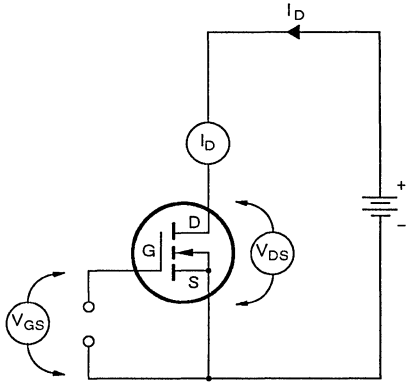
MOSFETS

The metal-oxide-silcon FET (MOSFET) depends on the fact that it is not actually necessary to form a semiconductor junction on the channel of a FET in order to achieve gate control of the channel current. Unlike the junction FET (JFET) a metallic or polysilicon gate may be simply isolated from the channel by a thin layer of silicon dioxide, as shown in Figure 7A. Although the bottom of the insulating layer is in contact with the p-type silicon substrate, the physical processes which occur at this interface dictate that free electrons will accumulate in the interface, inverting the p-type material and spontaneously forming an n-type channel. Thus, a conduction path exists between the diffused n-type channel source and drain regions.

There are, however, some fundamental performance differences between MOSFETs and JFETS. JFETs, by nature, operate only in the depletion mode. That is, a reverse gate bias depletes, or pinches off the flow of channel current. A MOSFET, by virtue of its electrically-insulated gate, can be fabricated to perform as either a depletion-mode or enhancement-mode FET. Quite unlike the JFET, a depletion-mode MOSFET will also perform as an enhancement-mode FET.

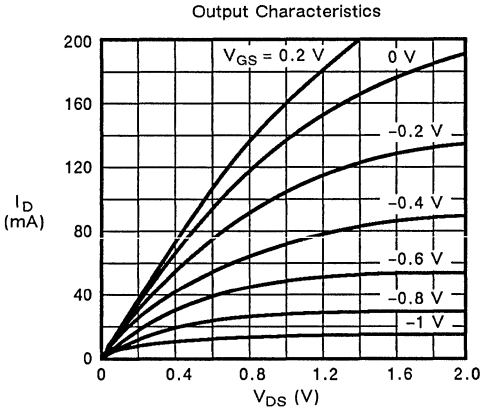


(A) Idealized cross-section through an n-channel depletion-type MOSFET



(B) Circuit arrangement for n-channel depletion MOSFET.

Figure 7.



(C) Family of output characteristics for an N-channel depletion MOSFET

Figure 7.

Where the greater majority of JFETs are fabricated similar to that shown in Figure 2, and operate in a fashion described in Figures 3 and 4, the MOSFET can assume several forms and operate in either the depletion/enhancement-mode or enhancement-mode only.

There are, today, three popular styles of small-signal MOSFETs. First, we have the planar, lateral MOSFET, similar to that shown in Figure 7A. By virtue of the n-doped channel spanning from source to drain, it performs as an n-channel depletion-mode MOSFET in a fashion not unlike that of the depletion-mode JFET when a voltage of the correct polarity is appliled to the gate, as in Figure 7B. However, if we forward-bias the gate (that is, place a gate voltage whose polarity equals the drain voltage polarity) additional electrons will be attracted to the region beneath the gate, further enhancing – and inverting (from p to n) the region. As the channel region thickens, the channel resistance will further decrease, allowing greater channel current to flow beyond that identified as I_{DSS}, as we see in the family of output characteristics in Figure 7C.

This MOSFET also can be constructed for enhancement-mode-only performance, as shown in Figure 8. Unlike the depletion-mode device, the enhancement-mode MOSFET offers no channel between the source and drain. Not until a forward bias on the gate enhances a channel by attracting electrons beneath the gate oxide will current begin to flow.

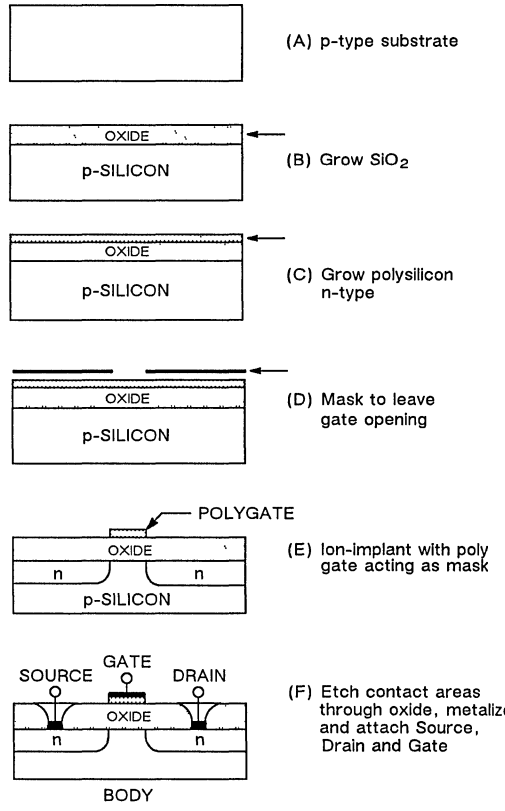


Figure 8. Fabrication of Planar Enhancement-Mode MOS

A newer MOSFET offering superior performance is the lateral double-diffused or DMOS FET. Because of the limitations of photo-lithographic masking, the earlier, older-style MOSFET was severely limited in performance. Some of these former limitations involved switching speeds, channel conductivity (too high an r_{DS}), and current handling in general. The lateral DMOS FET removed these limitations, offering a viable alternative between the JFET and the GaAs FET for video and high-speed switching applications.

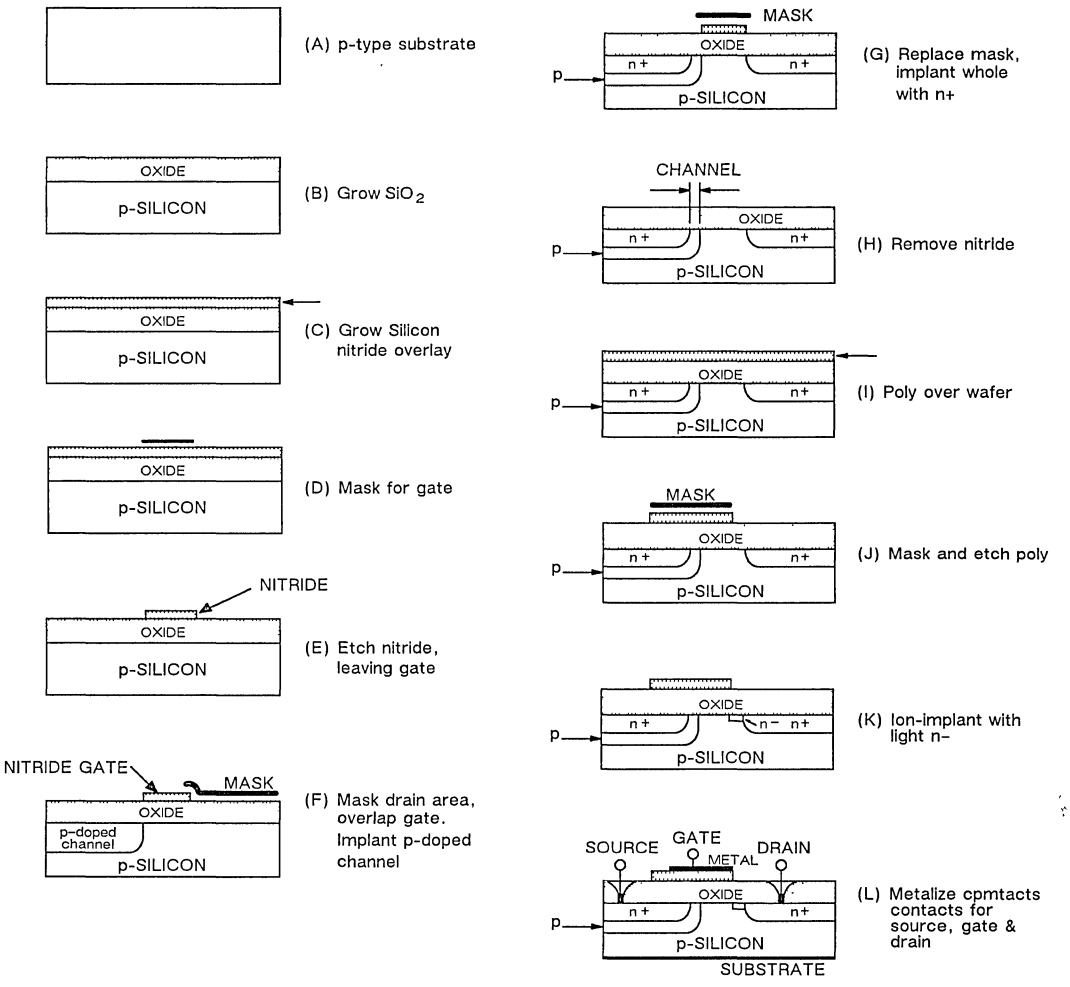


Figure 9. Fabrication of Planar Enhancement-mode DMOS

The lateral DMOS FET differs radically in its channel construction when compared with the older planar MOSFET. A self-explanatory series of construction views of an n-channel, enhancement-mode device is offered in Figure 9. Note the double-diffused source implant into the implanted p-doped channel region, shown in Figures 9 (f) and (g). The novelty that improves the performance of DMOS is both the precisely-defined short channel that results and the "drift region" resulting from the remaining p-doped silicon body and light n-doped ion implant, shown if Figures 9 (k) and (1).

Although Figures 8 and 9 illustrate the fabrication sequences for n-channel enhancement-mode DMOS FETs, by reversing the doping sequences, p-channel DMOS FETs could easily be fabricated. Furthermore, by lightly doping across the short channel and drift region, depletion-mode DMOS FETs could be constructed.

The combination of the short channel and the drift region allows the MOSFET to operate in "velocity saturation" (as a result of the short channel) and to offer higher operating drain voltages (as a result of the drift region). Together, both offer low on-resistance and low interlectrode capacitances, expecially gate-to-drain, V_{GD}.

Velocity saturation coupled with low interelectrode capacitance offers us high-speed and high-frequency performance.

The novelty of the short-channel DMOS FET led to the evolution of a yet more advanced, higher-voltage, higher-current MOSFET: the Vertical Double-Diffused MOSFET, shown in Figure 10. Where this vertical MOSFET offers improved power-handling capabilities, its fundamental shortcoming is that, because of its construction and to a lesser extent because of its size, it fails to challenge the high-speed performance of the lateral DMOS FET. Consequently, the vertical and lateral DMOS FETs complement each other in a wide selection of applications.

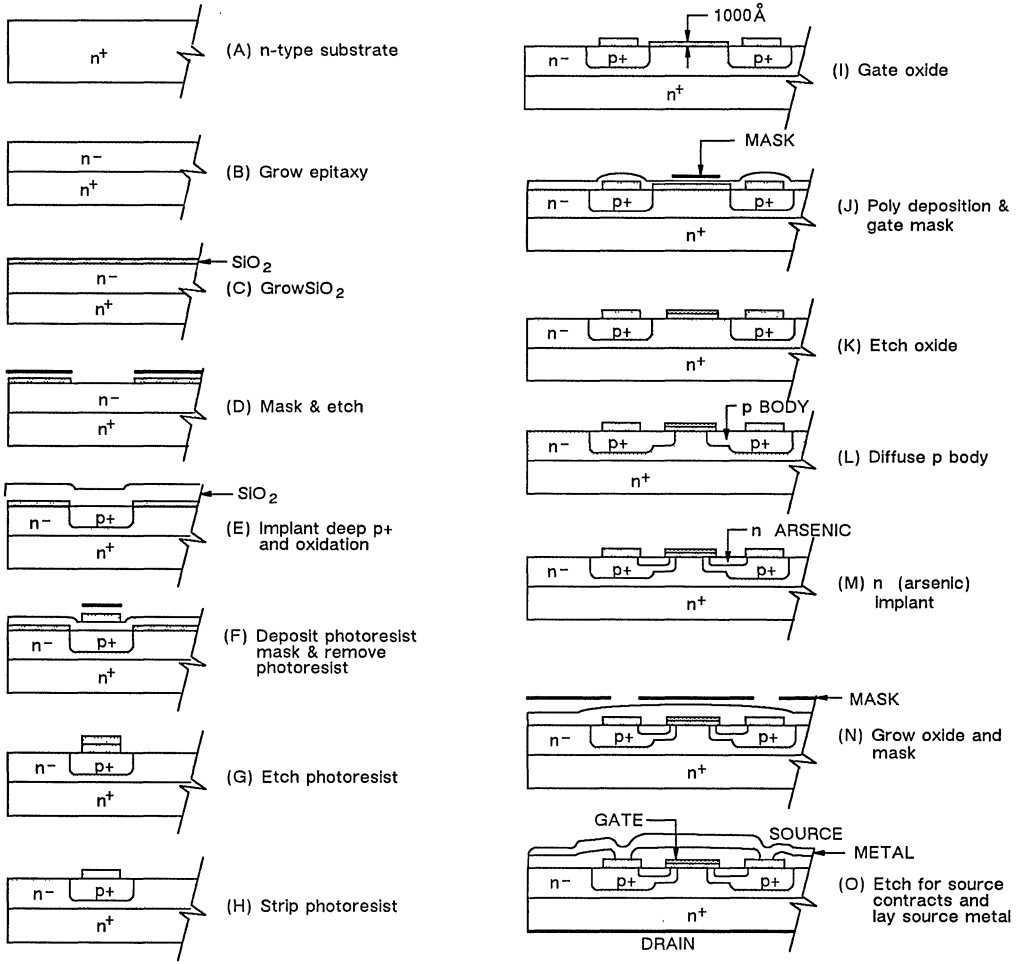


Figure 10. Vertical n-channel, enhancement-mode DMOS FET

UNDERSTANDING JFET PARAMETERS

Bob Landon

JFET Characteristics

The JFET enjoys certain inherent advantages over bipolar transistors because of the unique construction and method of operation of the field-effect device. These characteristics include:

- Low noise
- "Zero offset" On-resistance
- No thermal runaway
- Low distortion and negligible intermodulation products
- High input impedance at low frequencies
- Very high dynamic range (>100 dB)
- Zero temperature coefficient Q point
- Junction capacitance independent of device current

The transfer function of a JFET approximates to a square-law response, and the second and higher-order derivatives of g_{fs} are near zero; thus, strong second and negligible higher-order harmonics are produced. Intermodulation products are extremely low.

The input impedance of a JFET is simply the impedance of a reverse-biased pn junction, which is on the order of 10^{10} to $10^{13}\ \Omega$. In practice, the input impedance is limited by the value of the shunt gate resistor used in a self-bias common-source circuit configuration. At RF frequencies, the input impedance drop is proportional to the square of the frequency. In a 2N4416 JFET, for example, the input impedance would be 22 kΩ at 100 MHz. Also, the input susceptance increases linearly with frequency, since it is a simple parasitic capacitance.

The JFET has a very high dynamic range in excess of 100 dB. Thus it can amplify very small signals because it produces very little noise, or it can amplify very large signals because it has negligible intermodulation distortion products. It also has a zero temperature coefficient bias point (zero TC point) at which changes in temperature do not change the quiescent operating point.

Junction FET capacitances are more constant over wide current variation than are the same parameters in a bipolar device. This inherent stability allows high-frequency (VHF through L-band) oscillators to be built which are far more stable than oscillators using low-frequency crystals and multiplier stages.

JFET Terminology and Parameters

Any introduction to the nature, behavior, and applications of field-effect transistors requires that certain questions be answered on JFET electrical quantities and parameters, in particular the most important parameters, and the means by which they can be measured. The following discussion will define specific JFET parameters and their associated subscript notations, and present basic test circuits and results.

Major parameters include:

- I_{DSS} – Drain current with the gate shorted to the source
- $V_{GS(off)}$ – Gate-source cutoff voltage
- I_{GSS} – Gate-to-source current with the drain shorted to the source
- $V_{(BR)GSS}$ – Gate-to-source breakdown voltage with the drain shorted to the source
- g_{fs} – Common-source forward transconductance
- C_{gs} – Gate-source capacitance
- C_{gd} – Gate-drain capacitance

Special attention should be given to the subscript "s" because it has two different meanings and three possible uses. In JFET notations, an "s" for the first or second subscript identifies the source terminal as a node point for voltage reference or current flow. However, when using triple subscript notation, an "s" for the third subscript is an abbreviation for "shorted", and signifies that all terminals not designated by the first two subscripts must be tied together and shorted to the common terminal, which is always the second subscript. Therefore, the term I_{GSS} refers to the gate-source current with the drain tied to the source.

Because of the typical low input and output admittance of the JFET, four-pole admittance equations are commonly used to describe electrical characteristics of the JFET:

$$I_1 = Y_{11}\ V_{11} + Y_{21}\ V_{22} \qquad (1)$$

When Y_{11}, Y_{21}, Y_{12} and Y_{22} are defined as the input, reverse transfer, forward transconductance, and output admittance respectively, Equation 1 reduces to

$$i_1 = y_i v_{11} + y_r v_{22}$$
$$i_2 = y_f v_{11} + y_o v_{22} \quad (2)$$

For a three-lead JFET, 11 usually corresponds to the gate-source terminal and 22 corresponds to the drain-source terminal (i.e., the device is connected in the common-source mode). Thus

$$i_i = y_{is} v_{gs} + y_{rs} v_{ds}$$
$$i_o = y_{fs} v_{gs} + y_{os} v_{ds} \quad (3)$$

Here, the second subscript for the y parameters designates the source lead as the common or ground terminal.

I_{DSS} – Drain Current at Zero Gate Voltage (I_D at V_{GS} = 0)

By itself, I_{DSS} merely refers to the drain current that will flow for any applied V_{DS} with the gate shorted to the source. However, when a particular value for V_{DS} is given, equal to or greater than V_p (see Figure 1), I_{DSS} indicates the drain saturation current at zero gate voltage. Some JFET data sheets label I_{DSS} for V_{DS} greater than V_p as $I_{D(ON)}$.

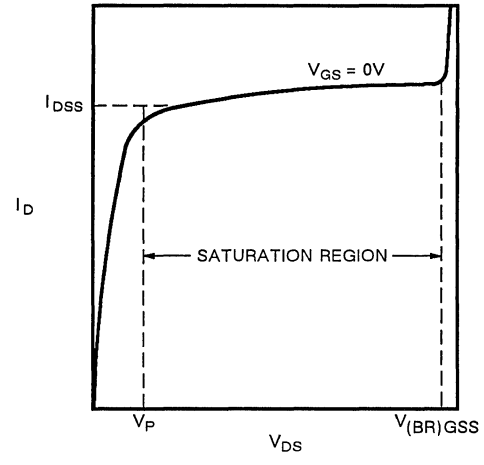


Figure 1. JFET Characteristic at V_{GS} = 0 V

$V_{GS(off)}$ – Gate-Source Cutoff Voltage

The resistance of a semiconductor channel is related to its physical dimensions by R = ρL/A, where

ρ = resistivity
L = length of the channel
A = W x T = cross-sectional area of channel

In the usual JFET structure, L and W are fixed by device geometry, while channel thickness T is the distance between the depletion layers. The position of the depletion layer can be varied either by the gate-source bias voltage or by the drain-source voltage. When T is reduced to zero by any combination of V_{GS} and V_{DS}, the depletion layers from the opposite sides come into contact, and the a-c or incremental channel resistance r_{DS}, approaches infinity. As earlier noted, this condition is referred to as "pinch-off" or "cutoff" because the channel current has been reduced to a very thin sheet, and current will no longer be conducted. Further increases in V_{DS} (up to the junction reverse-bias breakdown) will cause little change in I_D. Accordingly, the pinch-off region is also referred to as the pentode or "constant-current" region.

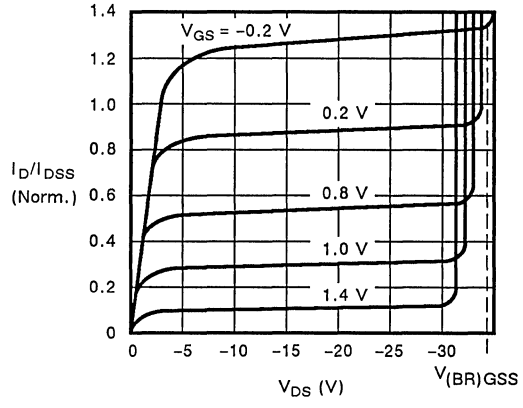


Figure 2. JFET Output Characteristics

In Figure 1, pinch-off occurs when V_{GS} = 0. In Figure 2, V_{GS} controls the magnitude of the saturated I_D, with increases in V_{GS} resulting in lower values of constant I_D and smaller values of V_{DS} necessary to reach the "knee" of the curve. The current scale in Figure 2 has been normalized to a specific value of I_{DSS}.

The knee of the curve is important to the circuit designer because he must know what minimum V_{DS} is needed to reach the pinch-off region with V_{GS} = 0 V. When appropriate bias voltage is applied to the gate, it will pinch off the channel so that no drain current can flow; V_{DS} has no effect until breakdown occurs. the specific amount of V_{GS} that produces pinch-off is known as the gate-source cutoff voltage, $V_{GS(off)}$.

$V_{GS(off)}$ Test Procedure

Although the magnitude of $V_{GS(off)}$ is equal to the pinch-off voltage, V_p, defined by the pinch-off knee in Figure 1, rapid curvature in the area makes it difficult to define any precise point as V_p. Taking a second derivative of V_{DS}/I_D would yield a peak corresponding to the inflection point at the knee which approximates V_p. However, this is not a simple measurement for production quantities of devices. A better measure is to approach the cutoff point of the I_D versus V_{GS} characteristic. This is easier than trying to specify the location of the knee of the I_D versus V_{DS} output characteristic.

A typical transfer characteristic I_D versus V_{GS} is shown in Figure 3. The curve can be closely approximated by

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 \qquad (4)$$

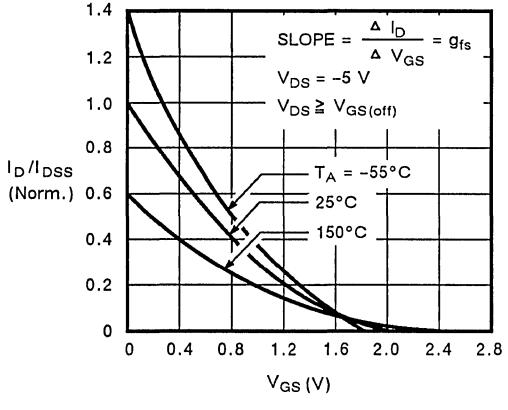


Figure 3. Typical I_D vs V_{GS} Transfer Characteristic

Equation 4 and Figure 3 indicate that at $V_{GS} = V_{GS(off)}$, I_D = 0. In a practical device, this cannot be true because of leakage currents. If I_D is reduced to less than 1 percent of I_{DSS}, V_{GS} will be within 10 percent of the $V_{GS(off)}$ value indicated by Equation 4. If I_D is reduced to 0.1 percent of I_{DSS} the indicated $V_{GS(off)}$ error will be reduced to about 3 percent. For a true indication of $V_{GS(off)}$, and a realistic picture of the parameters of Figure 3, care must be taken that leakage currents do not result in an error in the $V_{GS(off)}$ reading. Typically, at room temperature, 1 percent of I_{DSS} is still well above leakage currents but is low enough to give a fairly accurate value of $V_{GS(off)}$.

A typical circuit for measuring $V_{GS(off)}$ is shown in Figure 4. At V_{GS} = 0 V, the value of I_{DSS} can be measured. Then by increasing V_{GS} until I_D is 0.01 percent of I_D at some fixed value (such as 1 nA), rather than as a certain percentage of I_{DSS}. Thus a pinch-off voltage specification may be given as indicated in Table I.

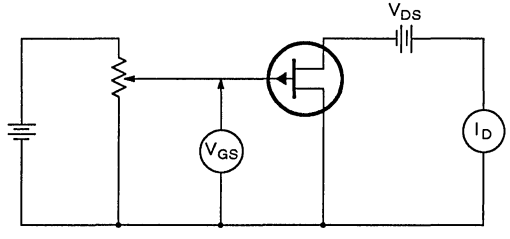


Figure 4. Circuit for Measuring $V_{GS(off)}$

Another method which provides an indirect indication of the maximum value of $V_{GS(off)}$ is shown in Table II. The characteristic specified is $I_{D(off)}$, where the parameter of interest is V_{GS} = 8 volts. The specification does say that the maximum $V_{GS(off)}$ is approximately 8 V, but no provision is made for stating a minimum $V_{GS(off)}$, as was done in Table I. Therefore, another test must be made if $V_{GS(off)(min)}$ is to be specified.

9

Table I. Typical Pich-Off Voltage Specification

Characteristics		Test Conditions	Min	Max	Unit
$V_{GS(off)}$	Gate-Source pinch-off voltage	V_{DS} = -5 V, I_D = -1 µA	1	4	V

Table II. Indication of Maximum $V_{GS(off)}$

Characteristics		Test Conditions	Min	Max	Unit
$I_{D(OFF)}$	Pinch-off drain current	V_{DS} = -12 V, V_{GS} = 8 V		-10	nA

I_{GSS} - Gate-Source Cutoff Current

The input gate of a p-channel JFET appears as a simple pn junction; thus the dc input characteristic is analogous to a diode V-I curve, as shown in Figure 5.

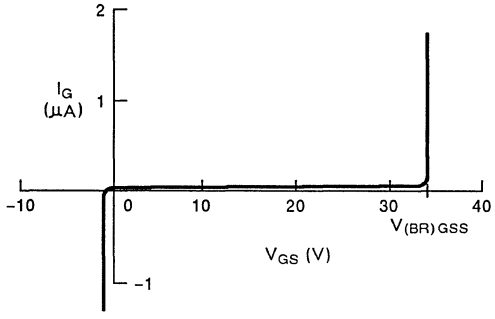


Figure 5. P-Channel JFET Input Gate Characteristic

In the normal operating mode, with V_{GS} positive for a p-channel device, the gate is reverse-biased to a voltage between zero and $V_{GS(off)}$. This results in a dc gate-source resistance which is typically more than 1000 MΩ. The gate current is both voltage and temperature sensitive. Figure 6 shows this relationship for I_{GSS} versus temperature and V_{GS}.

If the gate-source junction becomes forward-biased, (negative voltage in a p-channel device) or if V_{GS} exceeds the reverse-bias breakdown of the junction, the input resistance will then become very low.

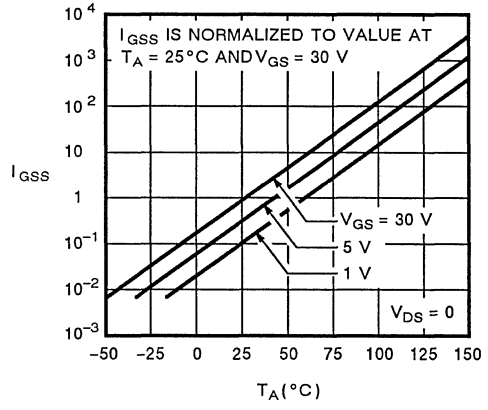


Figure 6. I_{GSS} vs. Temperature

The JFET is normally operated with a slight reverse bias applied to the gate-source; hence, a good measure of the dc input characteristic is to check the gate current at a value of gate-channel voltage that is below the junction breakdown rating. In device evaluation, there are the common measurements of gate current: I_{GDO}, I_{GSO}, and the combined measurement I_{GSS}. These measurement circuits are shown in Figure 7.

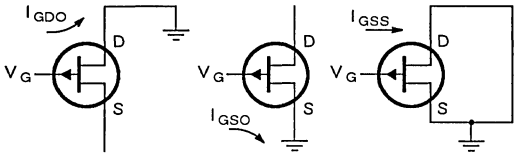


Figure 7. Three Common Measurements of Gate Current

The question is, should I_{GDO} and I_{GSO} be measured separately, or will one measurement of I_{GSS} suffice? One thing is certain: $I_{GSO}+I_{GDO}>I_{GSS}$, because the drain and the source are not completely isolated. They are, in fact, electrically connected via channel resistance. For most JFETs, if V_G is greater than $V_{GS(off)}$, the difference between (I_{GSO} + I_{GDO} and I_{GSS} is small; therefore, the measurement of I_{GSS} is a realistic means of controlling both I_{GDO} and I_{GSO}.

In a circuit, V_{GD} may be biased between zero and $V_{(BR)GSS}$, while V_{GS} will be between zero and $V_{GS(off)}$: therefore, I_G is not necessarily the same as I_{GSS}.

$V_{(BR)GSS}$ - Gate-Source Breakdown Voltage

JFET input terminals have been previously described as having np or pn junctions, depending on the channel material. As such, the junction breakdown voltage is a necessary parameter.

A useful equivalent circuit for a JFET is the distributed constant network shown in Figure 8, for a p-channel JFET. If an n-channel device is being evaluated, the diodes would be reversed. In most applications, the gate-drain voltage is greater than the gate-source voltage; thus, the gate-drain breakdown rating is most important. However, it is also possible to consider the gate-source junction breakdown and the apparent drain-source breakdown (i.e., in Figure 8, when a high negative voltage is applied from drain to source, CR_1 will break down while CR_n becomes forward-biased).

Some device manufacturers use a BV_{GDO} rating, which means they are only checking diode CR_1. A better method is to use a $V_{(BR)GSS}$ rating (gate-source breakdown with the drain shorted to the source), because it checks both CR_1 and CR_n, in addition to exposing the weakest breakdown path along the entire gate-channel junction. The $V_{(BR)GSS}$ test also allows the user to interchange source and drain lead connections without worry about device breakdown ratings.

Admittedly, a $V_{(BR)GSS}$ test will reject some units which might pass a BV_{GDO} test; the number rejected, however, will be insignificant compared to the advantage of providing symmetrical operation.

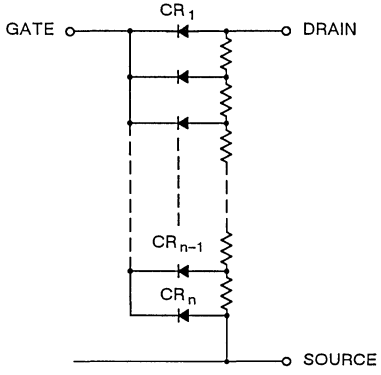


Figure 8. A Useful JFET Equivalent Circuit

Test Procedures for $V_{(BR)GSS}$

Junctions may break down softly or sharply; junctions with soft knee breakdown are undesirable. Without examining each individual unit on a curve tracer, devices with a soft knee may be eliminated by selecting a low current level for breakdown measurement (see Figure 9).

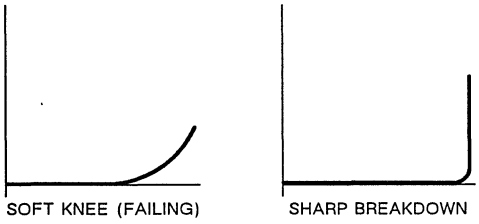


Figure 9. Example of Soft Knee and Sharp Knee Breakdown

g_{fs} – Transconductance

Transconductance, g_{fs}, is a measure of the effect of gate voltage upon drain current:

$$g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} \; ; \; V_{DS} = \text{constant} \qquad (5)$$

The interrelation of g_{fs} to the parameters I_{DSS} and $V_{GS(off)}$ should be noted. Equations 4, 6, and 7 describe the value of I_D and g_{fs} in a JFET for any value of V_{GS} between zero and $V_{GS(off)}$.

$$g_{fs} = g_{fso}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right) \qquad (6)$$

$$g_{fso} = -\frac{I_{DSS}}{V_{GS(off)}} \qquad (7)$$

where g_{fso} is the value of g_{fs} at V_{GS} = 0 V and I_{DSS} is the value of I_D at V_{GS} = 0 V. With these equations, the value of g_{fs} can be calculated with a fair degree of accuracy (20 percent) if I_{DSS} and $V_{GS(off)}$ are known.

Figure 10 shows normalized curves for I_D and g_{fs} as functions of V_{GS} in a P-Channel JFET. These curves were obtained from actual measurements on typical diffused channel JFETs. The curves agree very well with Equation 4 and 6 until $V_{GS(off)}$ is approached. For these curves, $V_{GS(off)}$ was assumed to be the value of V_{GS} where I_D/I_{DSS} = 0.001.

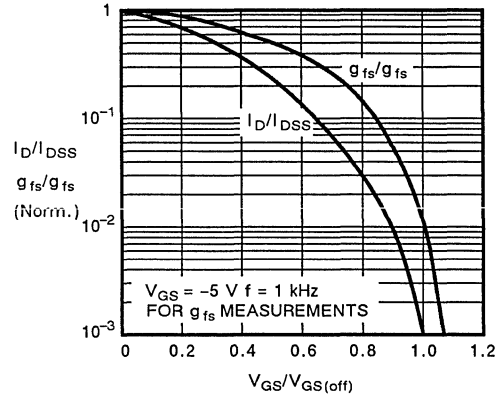


Figure 10. Normalized Curves for I_D and g_{fs} as Functions of V_{GS}

The drain current of a JFET operating in the triode (below pinch-off) region can be accurately predicted by using Equation 8, where

$$I_D \text{ / triode} = I_{DSS}\left(\frac{V_{DS}}{V_{GS(off)}}\right)^{1/2} \qquad (8)$$

Specifications for g_{fs} are shown in Tables III and IV. Note that there is a difference in the test conditions specified for the n-channel and the p-channel devices. The gate voltage for the n-channel is established as zero. This means that g_{fs} is measured at $I_D = I_{DSS}$, as in Table III.

The test conditions shown in Table IV specify a certain value for I_D (–200 μA). This means that for each unit tested, V_{GS} is adjusted until I_D equals the specified value. The conditions specified in Table II simplify testing of the g_{fs} parameter by eliminating the necessity of adjusting V_{GS}. Figures 11 and 12 show typical test systems for the two methods.

Table III.

Characteristics		Test Conditions	Min	Max	Unit
g_{fs}	Small-signal common-source forward transconductance	V_{DS} = 15 V, V_{GS} = 0, f = 1 kHz	4,500	7,500	μS

Table IV.

	Characteristics	Test Conditions	Min	Max	Unit
g_{fs}	Common-source forward transconductance	V_{DS} = 20 V, I_D = 200 µA f = 1 kHz	700	1,600	µS

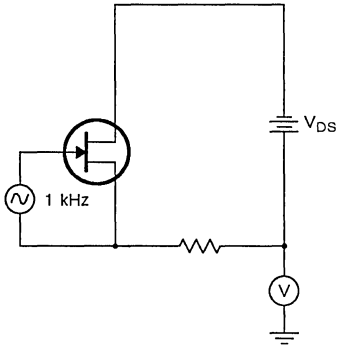


Figure 11. Test Circuit for g_{fs} with V_{GS} = 0V

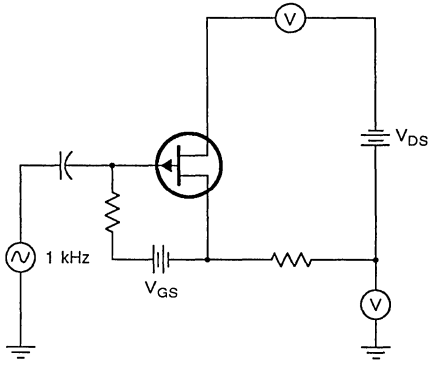


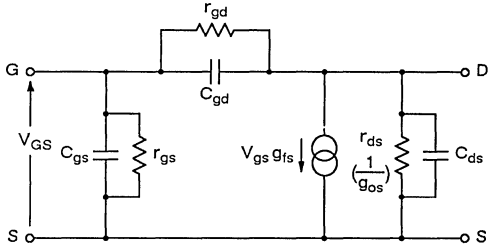
Figure 12. Test Circuit for g_{fs} with I_D Specified

Junction FET Capacitances

Associated with the junction between the gate and the channel of a JFET is a capacitance whose value and geometric distribution are functions of the applied voltages V_{GS} and V_{DS}. Because of the complexity of dealing with such a distributed capacitance, a simplification is made so that two lumped capacitances, C_{gs} and C_{gd}, exist between the gate and the source and drain, respectively. (A much smaller capacitance, C_{ds}, also exists between the drain and the source, stemming mainly from the device package; this header capacitance is small enough so that it can be ignored for most purposes.)

Data sheets quote C_{gs} and C_{gd} (or other capacitances from which they may be derived) for specified operating conditions. Occasionally, graphs are included which show the variations of C_{gs} and C_{gd} as the result of changing conditions of V_{DS}, V_{GS} and temperature. If this data is not presented, an estimate of interelectrode capacitance values may be made by assuming that these values vary inversely with the square root of the bias voltage. The temperature variations will be very small, because they depend on the -2.2 mV° C change in junction potential difference.

Assuming that the JFET is properly biased – that is the dc conditions are met by the external circuitry – it is possible to construct an incremental equivalent circuit from which the small-signal or ac performance may be predicted. Such an equivalent circuit is shown in Figure 13.



NOTE: $C_{gss} = C_{iss} = C_{gs} + C_{gd}$
$C_{oss} = C_{gd} + C_{ds} \geq C_{gd} = C_{rss}$

Figure 13. Incremental Equivalent Circuit for the Junction FET

9

The equivalent capacitance from the gate to the source, C_{gs}, is shunted by a very large input resistance, r_{gs}, with both of these parameters being characteristic of a reverse-biased junction. Similarly, the equivalent capacitance from the gate to the drain is shunted by the very large resistance r_{gd}. (For most purposes, r_{gs} and r_{gd} may be neglected, and the gate impedance of the JFET treated as pure capacitance). At the drain side of the equivalent circuit the small capacitance C_{ds} – which stems from the header material – is shunted by the incremental channel resistance, r_{ds}. This resistance is capable of wide variations, depending on bias conditions. since the equivalent circuit is fundamentally relevant to the pinch-off or saturated condition, r_{ds} will be on the order of megohms.

The incremental channel current is given by the transconductance, g_{fs}, multiplied by the incremental gate voltage. For the small signal, v_{gs}, this is manifested in the equivalent circuit by the current generator $g_{fs}v_{gs}$. Notice that the conventional direction of flow of this current is such that i_d flows into the JFET, in a "positive" direction.

Many circuits can be designed around the equivalent circuit for the junction FET. The actual values of g_{fs} and r_{ds} can be measured as previously mentioned; there remains only the requirement to establish the methods of determining C_{gs} and C_{gd}.

First, assume that the JFET is in operation and that the drain is connected to the source via a large capacitor, i.e., the drain and source are short-circuited to ac. Under these circumstances, a capacitance measurement between the gate and the source will give

$$C_{dss}\,(\text{or } C_{oss}) \sim C_{gs} + C_{gd} \qquad (9)$$

Second, assume that the gate and source are short-circuited to ac in a similar manner. A capacitance measurement between the drain and the source will now give

$$C_{dss}\,(\text{or } C_{oss}) \sim C_{gd} \qquad (10)$$

The alternative symbols C_{iss} and C_{oss} simply refer to measurements made at the input (gate) and the output (drain) respectively. An alternative symbol for C_{gs} is C_{rss}, which refers to the "reverse" capacitance.

In data sheets, it is customary to state $C_{gss}(= C_{lss})$ and C_{dss} $(= C_{oss})$. C_{rss} is often given in place of C_{oss} because if $C_{ds} << C_{oss}$, which is usually the case, then $C_{rss} \sim C_{oss}$ Equations (9) and (10) can be used in those instances where it is necessary to extract C_{gs} and C_{gd}, as in

$$C_{gs} = C_{iss} - C_{gd} = C_{iss} - C_{rss} \qquad (11)$$

and

$$C_{gd} = C_{rss} \qquad (12)$$

Remember that all capacitance measurements should be made at the same bias levels, since the capacitances are functions of applied voltages. To indicate the order of the capacitances to be found in a junction FET, consider the following typical values given in a data sheet.

$$C_{iss}\begin{pmatrix}\text{at } V_{DS} = 15\text{ V, f = 1 MHz,}\\ V_{GS} = 0\end{pmatrix} = 7\text{ pF Max.}$$

and

$$C_{rss}\begin{pmatrix}\text{at } V_{DS} = 15\text{ V, f = 1 MHz,}\\ V_{GS} = 0\end{pmatrix} = 3\text{ pF Max.}$$

Hence, at a drain-source voltage of 15 V and a frequency of 1 MHz, $C_{gs} = 7 - 3 = 4$ pF maximum. Even though the JFET is physically symmetrical, bias conditions have forced the capacitances to be unequal.

FET BIASING

INTRODUCTION

Engineers often design FET amplifiers that are unnecessarily sensitive to device characteristics because they may not be familiar with proper biasing methods.

One way to obtain consistent circuit performance, in spite of device variations is to use a combination of constant voltage and self biasing. The combined circuit configuration turns out to be the same as that generally used with bipolar transistors, but its operation and design are quite different.

Three Basic Circuits

Let's examine three basic common-source circuits that can be used to establish a FET's operating point (Q-point) and then see how two of them can be combined to provide greatly improved performance. The three basic biasing schemes are:

- Constant-voltage bias, which is most useful for rf and video amplifiers employing small dc drain resistors.
- Constant-current bias, which is best suited to low-drift dc amplifier applications such as source followers and source-coupled differential pairs.
- Self bias (also called source bias or automatic bias), which is a somewhat universal scheme, particularly valuable for ac amplifiers.

The Q-point established by the intersection of the load line and the V_{GS} = −0.4 V output characteristic of Figure 1 provides a convenient starting point for the circuit comparison. The load line shows that a drain supply voltage, V_{DD}, of 30 V and a drain resistance, R_D, of 39 kΩ are being used.

The quiescent drain-to-source voltage, V_{DSQ}, is 15 V, allowing large signal excursions at the drain. Maximum input signal variations of ±0.2 V will produce output voltage swings of ±7.0 V, a voltage gain of 35.

The constant-voltage bias circuit (Figure 2) is analyzed by superimposing a line for V_{GG} = constant on the transfer characteristic of the FET.

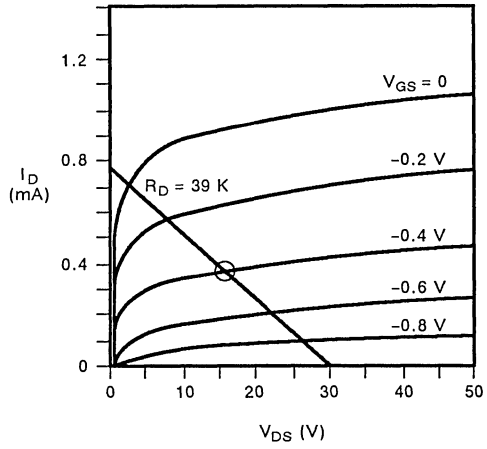


Figure 1. A large dynamic range is provided by the operating point at V_{DSQ} = 15 V, I_{DQ} = 0.39 mA and V_{GSQ} = −0.4 V.

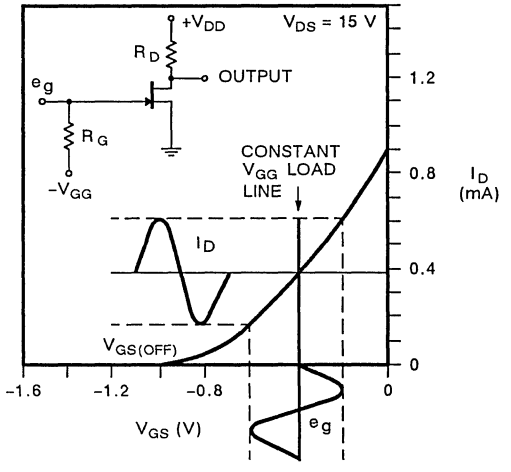


Figure 2. Constant-voltage bias is maintained by the V_{GG} supply as shown on this typical transfer curve. Input signal e_g moves the load line horizontally.

The transfer characteristic is a plot of I_D vs. V_{GS} for constant V_{DS}. Since the curve doesn't change much with changes in V_{DS}, it is useful in establishing operating bias points. In fact, it is probably more useful than the output characteristics because its curvature clearly warns of the distortion to be expected with large input signals. Furthermore, when a bias load line is superimposed, allowable signal excursions become evident, and input voltage, gate-source signal voltage, and output signal current calculations may be made graphically.

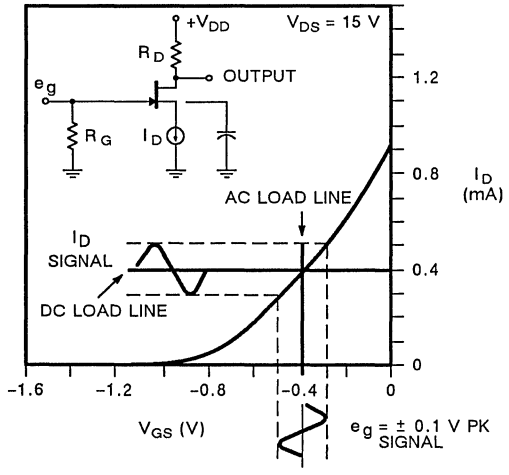


Figure 3. Constant-current bias fixes the output voltage for any R_D. Hence, input signals cannot affect the output unless the current source is bypassed.

The constant-current bias approach (Figure 3) for establishing the Q-point of Figure 1 requires a 0.39-mA current source. for an ideal constant-current generator, input signal excursions merely shift the bias line horizontally and produce no resultant gate-source voltage excursion. This bias technique is therefore limited to source followers, source coupled differential amplifiers, and ac amplifiers where the source terminal is bypassed to ground at the signal frequency.

If an ac ground is provided by a bypass capacitor across the current source, a vertical ac bias line will be established. Input signal variations will then translate the ac bias line horizontally, and signal development will proceed as with constant-voltage biasing (Figure 3).

The heavy vertical line at V_{GS} = -0.4 V establishes the Q-point of Figure 1. No voltage is dropped across resistor R_G because the gate current is essentially zero. R_G serves mainly to isolate the input signal from the V_{GG} supply.

Excursions of the input signal, e_g, combine in series with V_{GS} so that they add algebraically to the fixed value of -0.4 V. The effect of signal variation is to instantaneously shift the bias line horizontally without changing its slope. The shifting bias line then develops the output signal current as shown in Figure 2.

Should the bypass capacitor not provide a sufficiently low reactance at the signal frequency, the ac bias line will not be be vertical. It will still intersect the transfer curve at the Q-point but with a slope equal to $-(1/X_C) = -\omega C$ (Figure 4).

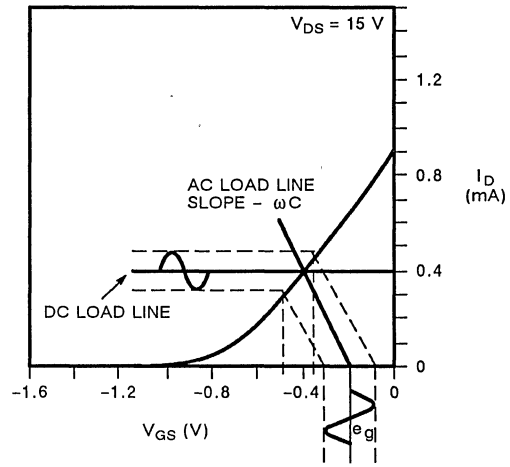


Figure 4. Partial bypassing of the current source (Figure 3) lowers the circuit gain by tilting the ac load line from the vertical. The capacitor drop subtracts from e_g.

This will lower the gain of the amplifier because of signal degeneration at the source. The input signal, e_g, is reduced by the drop across the capacitor:

$$V_{GS} = e_g - V_S = e_g - i_S X_C \qquad (1)$$

It is clear from Figure 4 that the input signal only shifts the operating point by an amount equal to V_{GS}, the effective input signal. As the signal frequency is decreased, the slope of the ac bias line decreases, causing the effective input signal to approach zero.

Self Bias Needs No Extra Supply

The self-bias circuit (Figure 5) establishes the Q-point by applying the voltage dropped across the source resistor, R_S, to the gate. Since no voltage is dropped across R_S when $I_D = 0$, the self-bias load line passes through the origin. Its slope is given by $-1/R_S = I_{DQ} / V_{GSQ}$.

Signal development is the same as in the case of the partially bypassed constant-current scheme except that the load line is a dc bias line. Signal degeneration is described by Equation 1 with X_C replaced by R_S. The ac gain of the circuit can be increased by shunting R_S with a bypass capacitor, as in the constant-current case. The ac load line then passes through the Q-point with a slope $-(1/Z_S) = -(\omega C + 1/R_S)$.

The circuit is biased automatically at the desired Q-point, requiring no extra power supply, and providing a degree of current stabilization not possible with constant-voltage biasing.

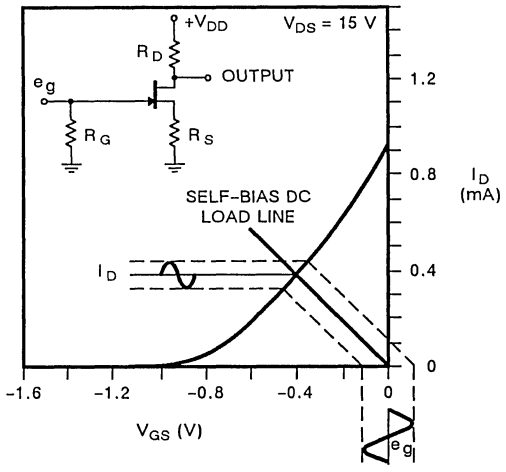


Figure 5. The self-bias load line passes through the origin with a slope $-1/R_S$. Bypassing R_S will steepen the slope and increase the gain of the circuit.

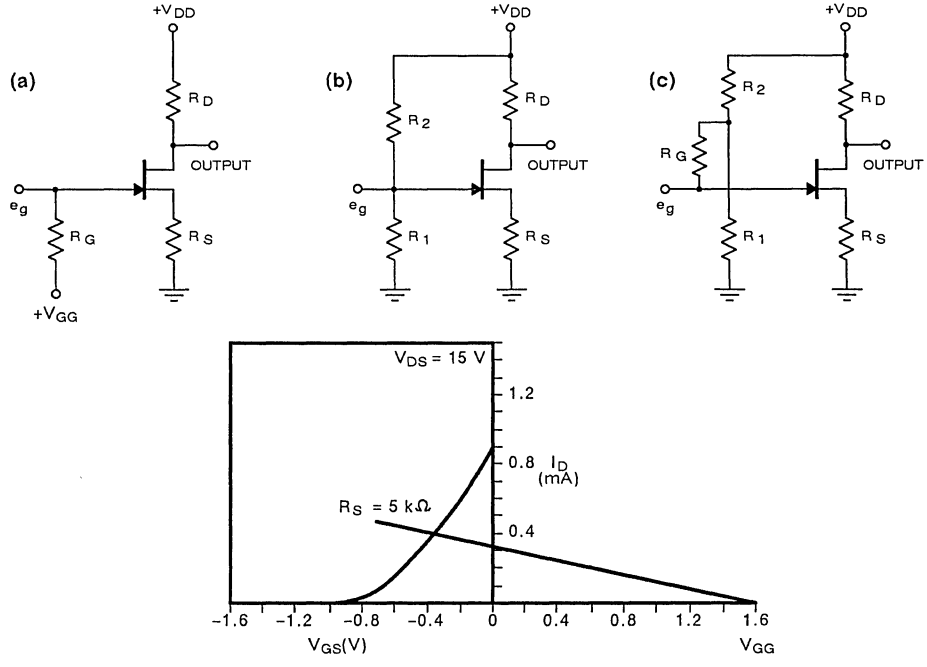


Figure 6. All three combination-bias circuits are equivalent. They add constant-voltage biasing to the self-bias circuit to establish a reasonably flat load line without sacrificing dynamic range.

A fourth biasing method, combining the advantages of constant-current biasing and self biasing, is obtained by combining the constant-voltage circuit with the self-bias circuit (Figure 6). A principal advantage of this configuration is that an approximation may be made to constant-current bias without any additional power supply. The bias load line may be drawn through the selected Q-point and given any desired slope by properly choosing V_{GG}. (The bias line intercepts the V_{GS} axis at V_{GG}.) The larger V_{GG} is made, the larger R_S will be and the better will be the approximation to constant-current biasing.

All three circuits in Figure 6 are equivalent. Circuit 6(a) requires an extra power supply. The need for an additional supply is avoided in 6(b) by deriving V_{GG} from the drain supply. R_1 and R_2 are simply a voltage divider. To maintain the high input impedance of the FET, R_1 and R_2 must both be very large.

Very large resistors cannot always be found in the exact ratio needed to derive the desired V_{GG} in every circuit application. Circuit 6(c) overcomes this problem by placing a large R_G between the center point of the divider and the gate. This allows R_1 and R_2 to be small, without lowering the input impedance.

One point of caution worth remembering is that as V_{GG} is increased, V_S increases, and V_{DS} decreases. Therefore, with low V_{DD}, there may be a significant decrease in the allowable output voltage swing.

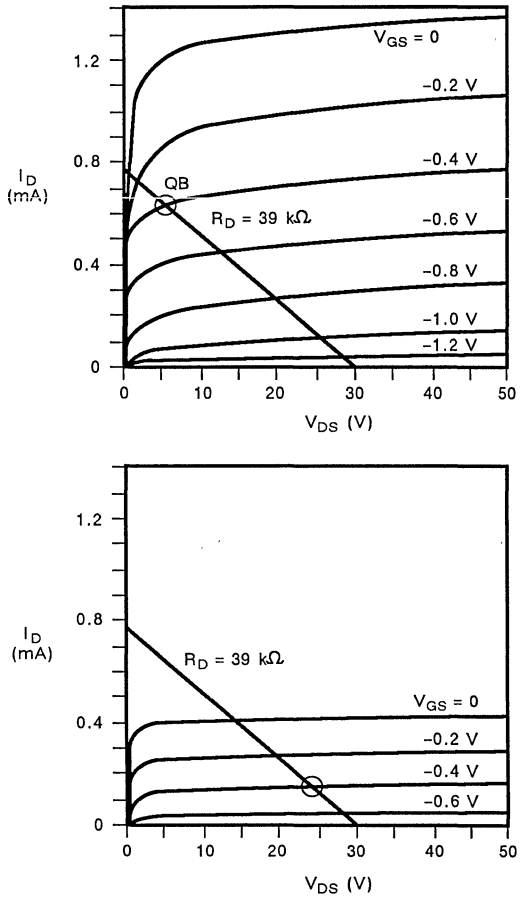


Figure 7. The wide variations in device performance shown by this pair of output characteristics make clear the disadvantages of constant-voltage biasing.

Biasing for Device Variations

The value of the combination-bias technique becomes apparent when one considers the normal production spread of device characteristics. The problem is illustrated in Figure 7 where two limiting sets of output characteristics are presented. Limiting characteristics like these are not normally available. Even if they were, however, they'd be of little help in establishing operating points suitable for all devices with output characteristics lying between the two extremes. The problem is much more easily approached by using the set of limiting transfer characteristics of Figure 8.

Attempting to establish suitable constant-voltage bias conditions for a production spread of devices is practical only for circuits with very small values of dc drain resistance – for example, circuits with inductive loads. As the constant-voltage bias plot of Figure 8 reveals, constant gate bias causes a significant difference in operating I_{DQ} for the extreme limit devices. At V_{GS} = –0.4 V, the range of I_{DQ} is 0.13 to 0.69 mA, and V_{GSQ} for a given R_D will vary greatly for most resistance-loaded circuits. For the example of Figure 1, with R_D = 39 kΩ and V_{DD} = 30 V, V_{GSQ} varies from near saturation (5 V) to 25 V.

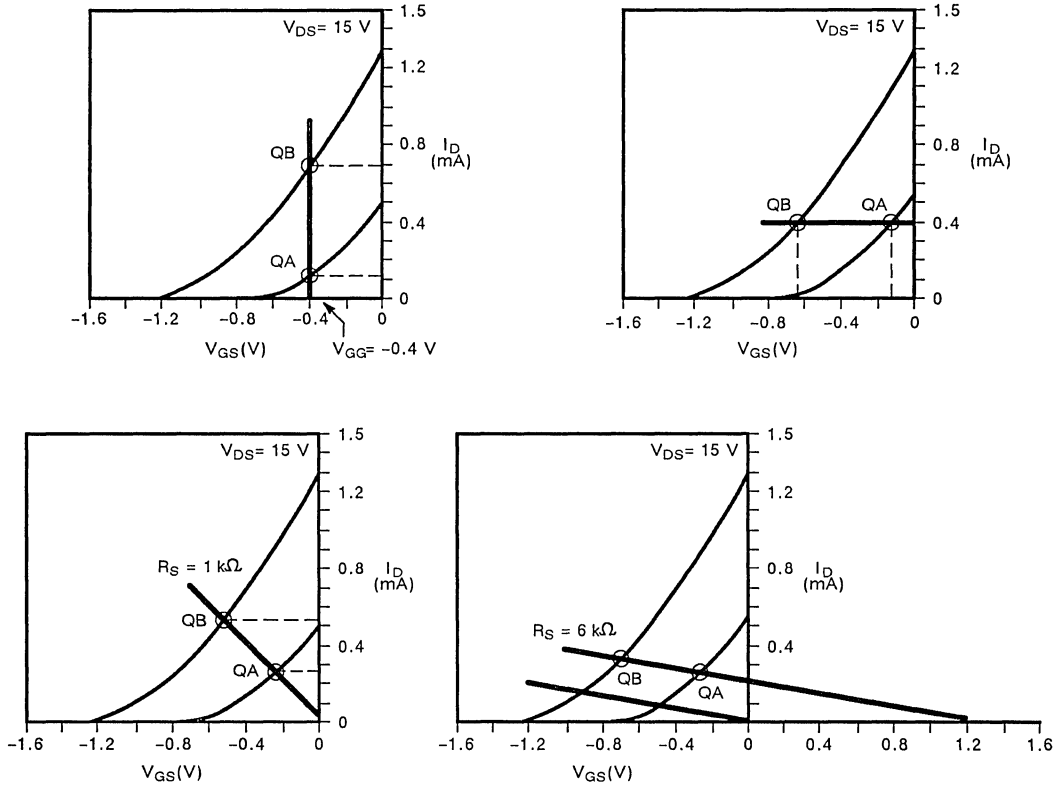


Figure 8. The advantages of combination biasing, when one is working with a spread of device characteristics, are made obvious by plotting the load lines for the various types of biasing on a pair of limiting transfer curves.

An excellent method of biasing is the constant-current method of Figure 3. Biasing in this manner fixes the operating drain current for all devices and sets V_{DSQ} to $V_{DD} - I_{DQ}R_L$ for any device in the production spread. V_{GS} automatically finds a value to set the appropriate I_{DQ} = constant for all devices. For the constant-current bias plot of Figure 8, with I_{DQ} = 0.39 mA, V_{GS} would range from -0.11 to -0.67 V.

Output characteristics are not needed as long as I_{DQ} is chosen to be below the minimum I_{DSS}. With R_D = 39 kΩ and V_{DD} = 30 V, V_{DSQ} is 14.8 V for all devices.

The disadvantages of the constant-current method are that it allows no signal to be developed unless the current source is bypasssed and, as we shall see, it lacks the flexibility to provide constant gain despite variations in the forward transconductance, g_{fs}, of the devices.

The self-bias scheme is a reasonable choice for single-ended dc amplifiers and for ac amplifiers. In unbypassed or dc circuits, some compromise must be made between the gain loss due to current feedback degeneration and the advantage of current stabilization achieved with high R_S.

An appropriate choice of I_{DQ} limits can be made by using the pair of limiting transfer curves. For example, for R_S = 1 kΩ, the load line shown on the self-bias curve of Figure 8 is established. The maximum I_D is 0.52 mA, and the minimum I_D is 0.24 mA. The operating range of V_{DSQ} may be calculated for any value of V_{DD} and R_D. Clearly, for R_D = 39 kΩ, the maximum-limit device (device B) would operate with V_{DSQ} = 9.8 V and the minimum-limit device (device A) would operate with V_{DSQ}= 20.6 V. This results in fairly satisfactory operation for all devices. However, such a variation in I_{DQ} imposes severe limitations on the circuit design.

A better approach is illustrated by the combination-bias curve of Figure 8 with V_{GG} = 1.2 V. The range of I_{DQ} for the bias condition is 0.25 mA to 0.32 mA. A similiar minimum difference in I_{DQ} could be achieved with R_S = 6 kΩ and V_{GG} = 0, (a self-bias condition) but the operating points would be pushed toward the toe of the transfer characteristics and allowable signal input would be reduced.

The upper load line allows g_{fs} = +1.8 V (limited by I_{DSSA}), while the lower line allows a V_{GS} of only +0.7 V (limited by $V_{GS(off)}$ A). (The subscript letters A and B refer to the minimum and maximum devices, respectively.) The combination circuit allows almost ideal operation over the full production spread of devices. Even with R_D = 6 kΩ, the V_{DSQ} would range only between 10 and 15 V.

For this circuit, R_D should be chosen to allow the largest output signal swing for I_{DQ} midway between the two extremes of 0.25 and 0.32 mA; namely 0.285 mA. Setting the voltage drop across R_D at one-half of (V_{DD} – 2$V_{GS(off)typ}$) or 14 V, yields R_D = (14 V/0.285 mA) = 49 kΩ .

It is helpful, in any design, to know the effect of temperature variations on the transfer curves and transconductance characteristics. Ideally, minimum and maximum transfer characteristics would be plotted at three temperatures: above, below, and at room temperature. Then the design would take all types of variation into account.

Minimize The Gain Variations

Leaving R_S unbypassed helps reduce gain variations from device to device by providing degenerative current feedback. However, this method for minimizing gain variations is only effective when a substantial amount of gain is sacrificed.

A better approach is to use the combination-bias technique with the bias point selected from the transfer and transconductance curves (Figure 9).

As Figure 9 shows, it is possible to find an R_S and a V_{GG} that will set I_{DQA} and I_{DQB} to values so that g_{fsQ} will be the same for both devices. The g_{fsQ} of all intermediate devices will be approximately equal to the limiting values. Thus, a constant, or nearly constant, stage gain is obtained even with a bypass capacitor.

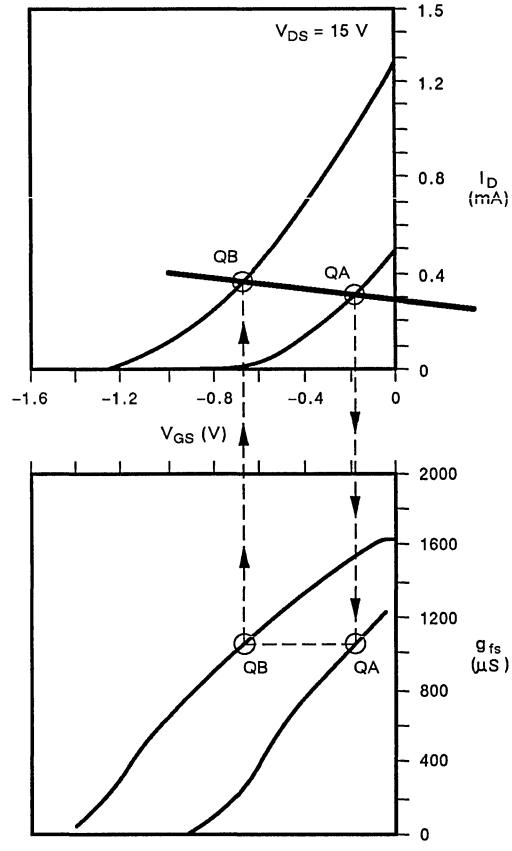


Figure 9. Gain variations are minimized when the load line is designed to intersect the pair of limiting transfer curves (top) at points of equal g_{fs} (bottom).

The design procedure is as follows:

Step 1. Select a desired I_{DQA} below I_{DSSA}. A good value, allowing for temperature variations, is 60% of I_{DSSA}. This will allow for decreasing I_{DSS} due to temperature variation and for reasonable signal excursions in load current.

Step 2. Enter the transfer curves at $I_{DQA} \sim 0.6\ I_{DSSA}$ (0.3 mA) to find V_{GSQA}. Thus $V_{GSQA} \sim -0.2$.

Step 3. Drop vertically at V_{GSQA} to the minmum limit transconductance curve to find g_{fsQA}. The value as read from the plot is approximately 1000 μS.

Step 4. Travel across the g_{fs} plot to the maximum curve to find V_{GSQB} at the same value of g_{fs}. This is $V_{GSQB} \sim -0.7$ V.

Step 5. Travel vertically up to the maximum limit transfer curve to find I_{DQB} at V_{GSQB}. This is $I_{DQB} \sim 0.36$ mA.

Step 6. Construct an R_S bias line through points Q_A and Q_B on the transfer curves. The slope of the line is $1/R_S$, and the intercept with the V_{GS} axis is the required V_{GG}.

As Figure 9 demonstrates, it may be somewhat inconvenient to perform Step 6 graphically. An algebraic solution can then be employed instead. The source resistance is given by

$$R_S = (V_{GSQA} - V_{GSQB}) / (I_{DQB} - I_{DQA}) \quad (2)$$

and the bias voltage is

$$V_{GG} = R_S I_{DQB} + V_{GSQB} \quad (3)$$

Care should be taken to maintain the proper algebraic signs in Equations 2 and 3. (For n-channel FETs, V_{GS} is negative and I_D is positive. For p-channel units, the signs are reversed.)

If the transconductance curves of Figure 9 are not available, g_{fs} can be determined by simply measuring the slope of the transfer curve at the desired operating point. Just place a straight-edge tangent to the curve at the Q-point and note the points at which it intercepts the I_D and V_{GS} axes. The slope and g_{fs} are given by:

$$\text{slope} = g_{fs} = I_{D(\text{intercept})} / -V_{GS(\text{intercept})} \quad (4)$$

In designing a constant-gain circuit, simply set the straight-edge tangent to the transfer curve of device A at point Q_A and slide it, without changing its slope, until it is tangent to the curve of device B. The tangency point is Q_B.

Designing Without Output Curves

Although the transfer characteristic has been seen to be extremely valuable in designing a bias circuit, it cannot be used to graphically establish V_{DSQ}. However, if a set of output curves is not available, V_{DSQ} can be determined or selected from the transfer curve by using the following procedure:

Step 1. Establish R_S and limiting values of I_{DQ}, V_{GSQ} and g_{fsQ} from the transfer curve.

Step 2. Establish V_{DD} as available, but in no case greater than BV_{GSS} nor less than several times $V_{GS(off)}$. There are special cases where V_{DD} will be below this limit, but in no case should instantaneous V_{DG} be allowed to fall below $2 \times V_{GS(off)}$ if minimum distortion is to be achieved.

Step 3. Set V_{DSQ} approximately midway between V_{DD} and $2 \times V_{GS(off)}$; lower if large output signals will not be handled.

Step 4. Select R_D to give the appropriate V_{DSQ}. The formula is:

$$R_D = [(V_{DD} - V_{DSQ})/0.5 (I_{DQA} + I_{DQB})] - R_S \quad (5)$$

In the example of Figure 8, this procedure would have yielded $V_{DSQ} = (30 - 3)/2 = 13.5$ V and $R_D = (30 - 13.5)/0.5\ (0.52 + 0.24)$ mA $- 1$ kΩ $= 42.5$ kΩ.

Step 5. Check to ensure that with this R_D, device B is not in a saturated condition, i.e. $V_{DQB} = V_{DD} - I_{DQB} R_D > 2 V_{GS(off)} + R_S I_{DQB}$.

An alternate method, that selects R_D to provide a specified voltage gain, follows Steps 1 and 2 above and then proceeds as follows:

Step 3 Determine required stage gain, A_V, and set $R_D = A_V/g_{fsQ}$.

Step 4. Calculate V_{DSQ} to ensure that the criteria of Step 2 are not violated:

$$V_{DSQ} = V_{DD} - (R_D + R_S) I_{DQ} \quad (6)$$

Step 5. If necessary, change I_{DQ}, V_{DD}, A_V and/or R_D to obtain an optimum compromise.

9

FET SOURCE-FOLLOWER CIRCUITS

The common-drain amplifier, or source follower, is a particularly valuable configuration; its high input impedance and low output impedance make it very useful for impedance transformations between FETs and bipolar transistors. By considering ten circuits (Figure 10), which represent virtually every source-follower configuration, the designer can obtain consistent circuit performance despite wide device variations.

There are two basic connections for source followers: with and without gate feedback. Each connection comes in several variations (Figure 10). Circuits 10(a) through 10(e) have no gate feedback; their input impedances, therefore, are equal to R_G. Circuits 10(f) through 10(k) employ feedback to their gates to increase the input impedance above R_G.

Before getting into the details of bias-circuit design, note several general observations that can be made about the circuits of Figure 10:

- Circuits a, c, d, f, h, and j can accept only positive and small negative signals, because these circuits have their source resistors connected to ground. The other circuits can handle large positive and negative signals limited only by the available supply voltages and device breakdown voltage.
- Circuits c, d, e, h, j, and k employ current sources to improve drain-current (I_D) stability and increase gain.
- Circuits d, e, and k employ FETs as current sources. In circuit d, Q_2 must have a lower cutoff voltage, $V_{GS(off)}$, and a lower zero gate-voltage drain current, I_{DSS}, than Q_1.
- Circuits e, g, and k employ a source resistor, R_S, which may be selected to set the quiescent output voltage equal to zero.
- Circuits e and k use matched FETs. R_S is selected to set I_D near the specified low-drift operating current. The input-output offset is zero.

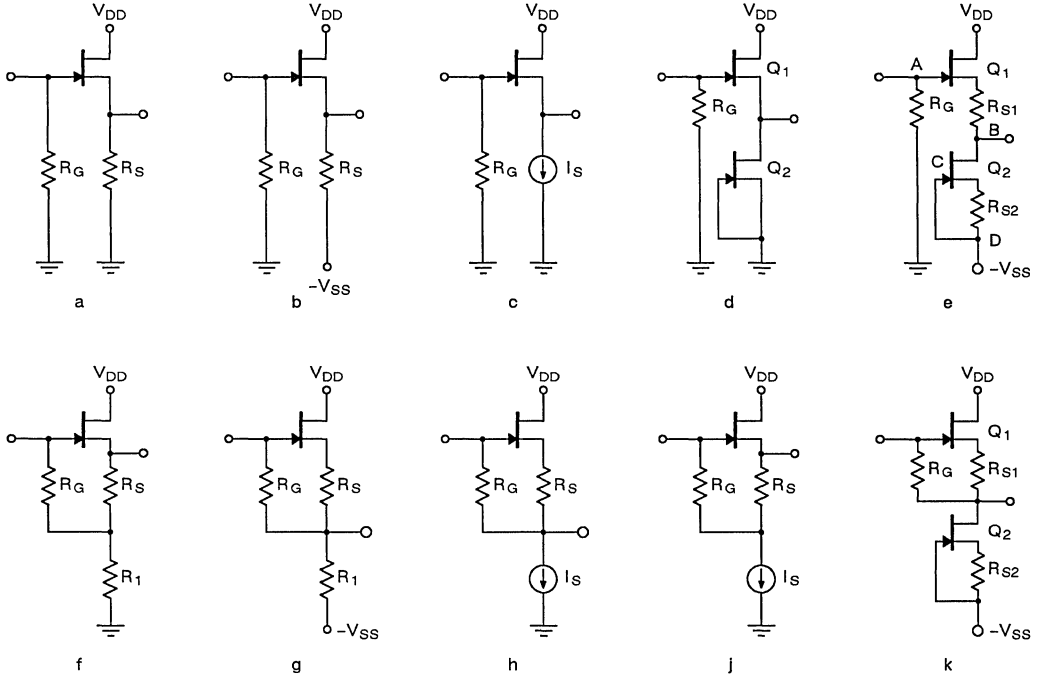


Figure 10. Virtually every practical source-follower configuration is represented in this collection of ten circuits. The configurations in the top row do not employ gate feedback; the corresponding ones in the bottom row do.

Biasing Without Feedback Is Simple

The no-feedback circuits of Figure 10 (circuits 10(a) through 10(e) use simple biasing techniques (see the earlier article). Circuit 10(a) is a self-bias configuration; the voltage drop across R_S biases the gate (which draws essentially zero current) through resistor R_G. Since no gate-to-source voltage, V_{GS}, can be developed when $I_D = 0$, the self-bias load line passes through the origin (Figure 11). The quiescent drain current is seen to lie between about 0.25 and 0.55 mA when a 1 kΩ source resistor is used. The quiescent output voltage lies between 0.25 and 0.55 V.

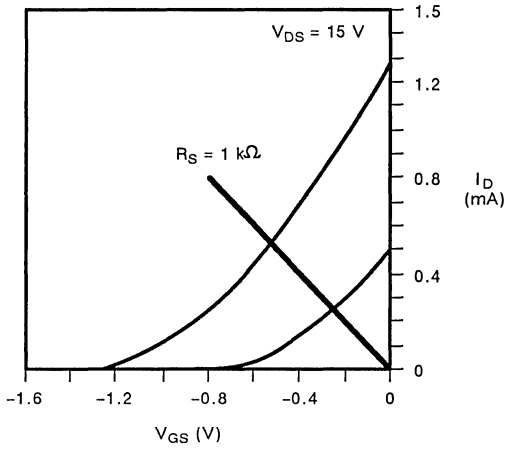


Figure 11. Self biasing (Figure 10a) uses the voltage dropped across the source resistor, R_S to bias the gate. The load line passes through the origin and has a slope of $-1/R_S$.

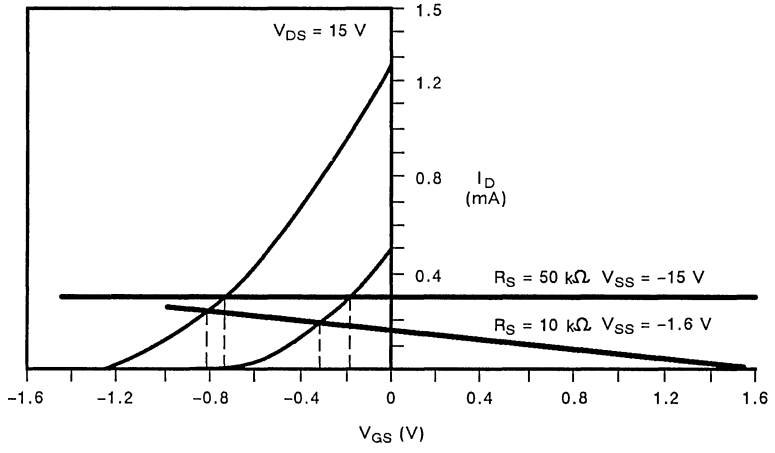


Figure 12. Adding a V_{SS} supply to the self-bias circuit (Figure 10b) allows it to handle large negative signals. The load line's intercept with the V_{GS} axis is at $V_{GS} = V_{SS}$. Bias lines are shown for V_{SS} = -15 V and V_{SS} = -1.6 V.

Circuit 10(b) is another example of source-resistor biasing with a $-V_{SS}$ supply added. The advantage over circuit 10(a) is that the signal voltage can swing negative to approximately $-V_{SS}$. Two bias lines are shown in Figure 12, one for V_{SS} = -15 V and the other V_{SS} = -1.6 V. For the first case, the quiescent output voltage lies between 0.18 and 0.74 V. For the second, it lies between 0.3 and 0.82 V.

The bias load line for circuit 10(c) is just a horizontal line (I_D = constant). The quiescent output voltage is between 0.15 and 0.7 for I_D = 0.3 mA.

Circuit 10(d) is similar to 10(c) except that the V_{GS} = 0 output characteristic of FET Q_2 is used as a current source. As seen in Figure 13, Q_2 does not supply constant current when its V_{DS} gets very small. This technique should therefore be used only to bias FETs whose $V_{GS(off)}$ is significantly higher than the equivalent $V_{GS(off)}$ of the current-source FET diode.

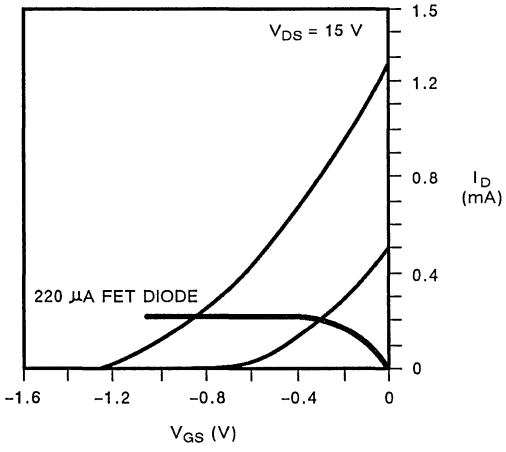


Figure 13. FET Q_2 doesn't behave like an ideal current source when its V_{DS} gets very small (Figure 10d). Therefore, Q_1 should have a significantly larger $V_{GS(off)}$ than the Q_2 does.

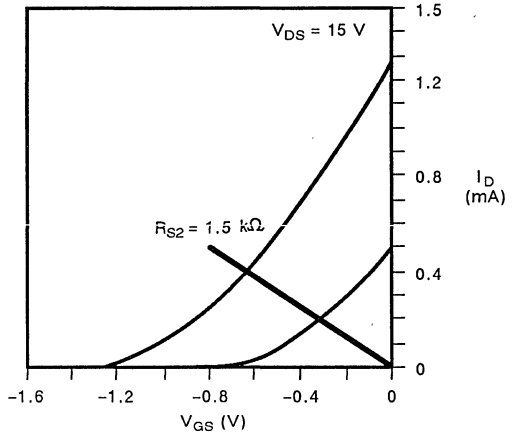


Figure 14. This load line is set by R_{S2} and Q_2 which acts as a current source (Figure 10e). This source follower, therefore, exhibits zero or near-zero offset. If the FETs are temperature-matched at the operating I_D, the source follower will exhibit zero or near-zero temperature drift.

A pair of matched FETs is used in the circuit of Figure 10(e), one as a source follower and the other as a current source. The operating drain current (I_{DQ}) is set by R_{S2}, as indicated by the load line of Figure 14. The drain current may be anywhere from 0.2 to 0.42 mA, as shown by the limiting transfer characteristic intercepts; however, $V_{GS1} = V_{GS2}$ because the FETs are matched.

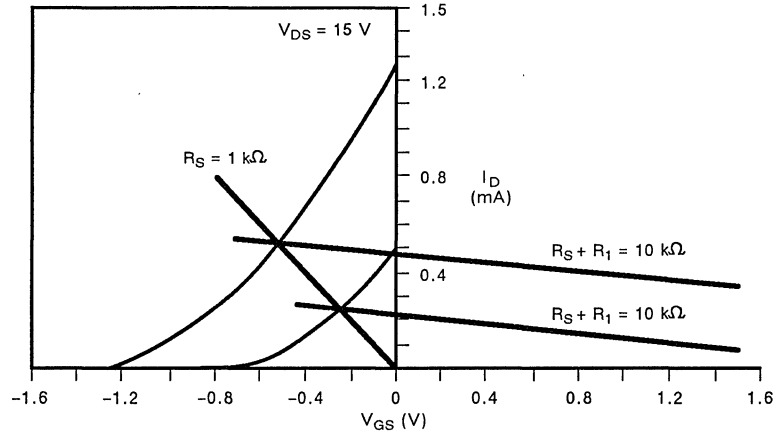


Figure 15. The bias load line is set by R_S but the output load line is determined by $R_S + R_1$ when gate feedback is employed (Figure 10f). The feedback V_{FB} is determined by the intercept of the $R_S + R_1$ load line and the V_{GS} axis.

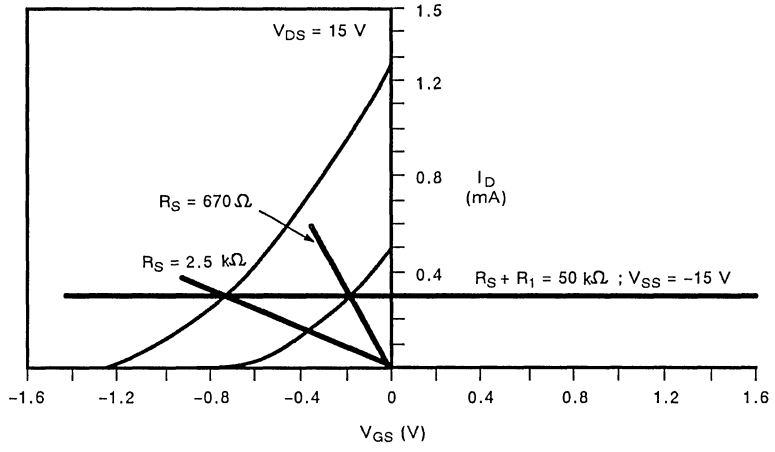


Figure 16. R_S can be trimmed to provide zero offset at some point between 670 Ω and 2.5 kΩ (Figure 10g). The source load line intercepts the V_{GS} axis at $V_{SS} = V_{GG} = -15$ V. Note that this load line is not perfectly flat. It has a slope of −1/50 kΩ, because the current source is not perfect; it has a finite impedance.

Biasing With Feedback Increases z_{IN}

Each of the feedback-type source followers (Figure 10(f) through 10(k) is biased by a method similar to that used with the nonfeedback circuit above it. However, in each case, R_G is returned to a point in the source circuit that provides almost unity feedback to the lower end of R_G. If R_S is chosen so that R_G is returned to zero dc volts (except in circuit 10(f), then the input/output offset is zero. R_1 is usually much larger than R_S.

Circuit 10(f) is useful principally for ac-coupled circuits. R_S is usually much less than R_1 to provide near-unity feedback. The bias load line is set by R_S (Figure 15). The output load line, however is determined by the sum of $R_S + R_1$. The feedback voltage V_{FB}, measured at the junction of R_S and R_1, is determined by the intercept of the $R_S + R_1$ load line with the V_{GS} axis. The quiescent output voltage is $V_{FB} - V_{GS}$.

In the circuit of Figure 10(g), R_S can be trimmed to provide zero offset. As the curves show (Figure 16), R_S will be between 670 Ω and 2.5 kΩ. R_S is much less than R_1. The source load line intercepts the V_{GS} axis at $V_{SS} = -V_{GG} = -15$ V.

Circuit 10(h) is almost the same as 10(g); the difference is that resistor R_1 is replaced by a current source. Since an ideal current source has infinite impedance, the bias curve of circuit 1(h) differs from that of Figure 10(g) (Figure 16) in that the load line is perfectly flat. In Figure 16 the load line is almost, but not quite, flat; it has a slope of −1/50 kΩ.

Circuit 10(j) is similar to 10(h) except that the output is taken from the top of R_S to reduce the output impedance. R_S must be trimmed if the circuit is to work properly.

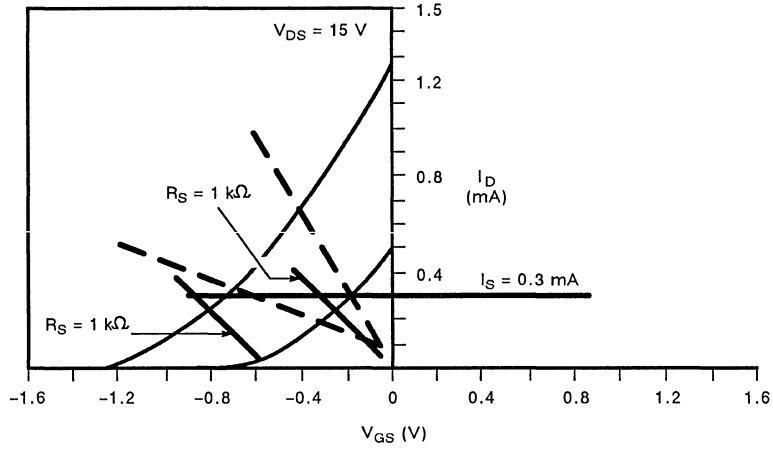


Figure 17. If R_S is not trimmed so that the load line passes through the origin, a voltage will appear at the gate causing a reduction in dc input impedance. The incremental input impedance will not be affected.

In Figure 17, the constant-current load line represents a 0.3 mA current source, and the effect of a 1 kΩ source resistor is shown. The offset voltage is seen to lie between 0.2 and 0.75 V. The intercept of the R_S load line and the V_{GS} axis sets the voltage at the junction of R_S and the current source (V_{FB}). For R_S = 1 kΩ, V_{FB} will be between -0.1 V and 0.45 V. Since V_{FB} appears at the gate, it must be zero if the dc input impedance of the circuit is to be preserved. This can be done by trimming R_S, as shown dashed in Figure 17. The biasing then becomes the same as for circuit 10(h).

Biasing for circuit 10(k) is identical to that for circuit 10(e) (Figure 14) except that feedback is added to raises the input impedance.

HIGH JFET GATE INPUT RESISTANCE SERVES WELL – IF YOU CAN UTILIZE IT

Ed Oxner
Reprinted from EDN, February 20, 1979

Many designers try to take advantage of high JFET input resistance, only to be disappointed with the results. Understanding the reasons for this characteristic can help you make the most of a useful JFET property.

One of the most widely known characteristics of JFETs – their high gate input resistance – is rarely specified on these devices' data sheets. But deriving this important parameter correctly from the information provided, and then applying it properly, are the keys to good JFET circuit design.

The sampling-probe circuit shown in Figure 1 is an example of a common JFET application. It utilizes as a source follower a 2N4868A n-channel device with a drain voltage of 30 V and a 1-mA drain current. Because this probe must sample 10 V-rms signals on a high-impedance line and must not load the circuit under test, it must also exhibit a very high input resistance. Assuming the data sheet for the JFET used in the probe lists a 40-V minimum breakdown voltage and a 250-pA maximum I_{GSS}, the probe circuit design does not provide the required high input resistance.

A MASTERY OF JFET CIRCUIT DESIGN BEGINS WITH THE DATA SHEET

To understand what's wrong with the circuit depicted in Figure 1 (and it isn't the JFET that's at fault), consider the roots of the problem. The JFET is used incorrectly here because of any or all of the following faults:

- An improperly characterized data sheet
- An improper interpretation of the data sheet
- A misunderstanding of why a JFET exhibits a high gate input resistance

You can't do much about the first fault except to make sure you know enough about these devices to recognize misleading data when you see it. For the most part, though, the latter two faults are the ones primarily responsible for incorrect JFET use.

If you design a circuit with at least 10 MΩ input resistance – such as the circuit in Figure 1 – and the JFET data sheet lacks an input-resistance specification, you can extract an indication of this important parameter from another specification: gate current, which is inversely proportional to gate input resistance. Thus, JFETs with a 1-mA gate current provide an input resistance orders of magnitude lower than those with a 1-nA gate current.

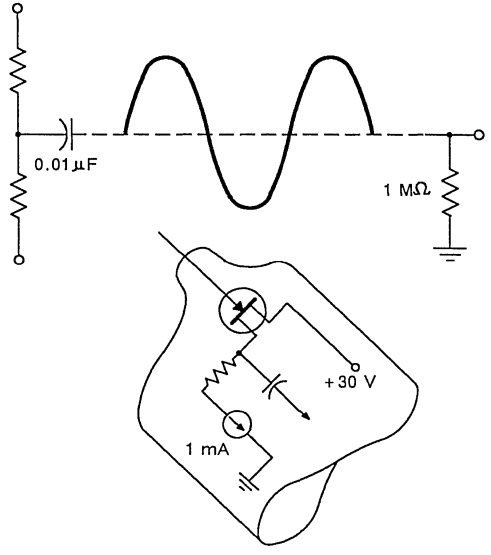


Figure 1. This JFET-input probe is designed for failure.

However, unwary designers can also fall into the trap of using I_{GSS} – gate current with the drain terminal shorted to the source – as an indicator of input resistance. But I_{GSS} does not characterize the operating gate current – clearly, the JFET's high input resistance is not utilized with the drain shorted to the source. Some years ago, the commonly accepted design procedure specified gate current at about 1/2 I_{GSS} for the desired drain-gate voltage. But this is a reasonable approximation only so long as the drain-gate voltage remains below the "I_G breakpoint."

The way out of this dilemma is to recognize that I_{GSS} represents nothing more than a measurement of reverse-bias diode current.

With source shorted to drain, the channel becomes a cathode and the gate becomes an anode, and their interaction can be considered to constitute a simple diode. In this diode model, the reverse current typically stays small until it increases abruptly at some finite voltage – termed the reverse (avalanche) breakdown voltage – because of a process called avalanche multiplication.

Reverse current itself originates principally from the thermal generation of electron/hole pairs within the JFET's junction space-charge region. Avalanche multiplication then occurs when an electron within this space-charge region develops so much energy, through increasing acceleration and subsequent collisions, that other electron/hole pairs are created, resulting in rapidly increasing reverse current and rapidly decreasing gate input resistance.

JFETs Act Differently In A Circuit

An operating JFET differs from the preceding diode model because its drain is not shorted to the source and some finite drain current passes through the channel. Designers, furthermore, often overlook this drain current's effects upon gate current.

Illustrating the drain-current effect, Figure 2 shows that gate current (I_G) increases linearly with drain current when the drain-gate voltage exceeds the I_G breakpoint; it also indicates that I_G increases exponentially with the drain-gate voltage (V_{DG}). (Raising the V_{DG} level increases impact ionization, thus increasing gate current.)

Replotting Figure 2 as Figure 3, this time using drain-gate voltage as the primary variable, exposes the critical relationship between these two parameters. The tremendous difference between the I_G curves and the superimposed I_{GSS} characteristic reveals the folly of using I_{GSS} values above the I_G breakpoint to determine gate input resistance.

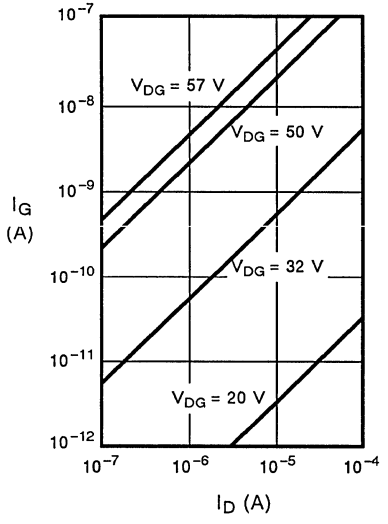


Figure 2. Gate current is a linear function of drain current in the 2N4868 JFET.

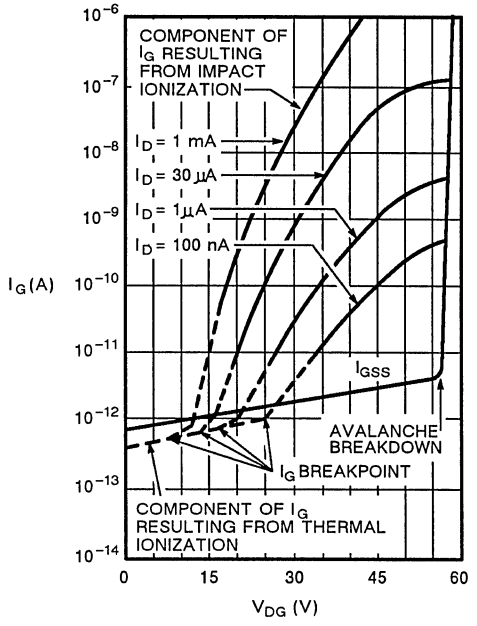


Figure 3. A plot of gate current versus drain gate voltage for the 2N4868 JFET shows why you can't use I_{GSS} values above the breakpoint to determine gate input resistance.

Yet another plot of the same JFET data yields additional information. Figure 4 shows a comparison of two ratios: gate current to drain current (I_G/I_D) versus drain-gate voltage to drain-gate breakdown voltage (V_{DG}/BV_{DGO}). Figure 2 provides data for the current ratio and Figure 3 furnishes voltage figures, with the drain-gate breakdown voltage established at the 57 V I_{GSS} breakpoint.)

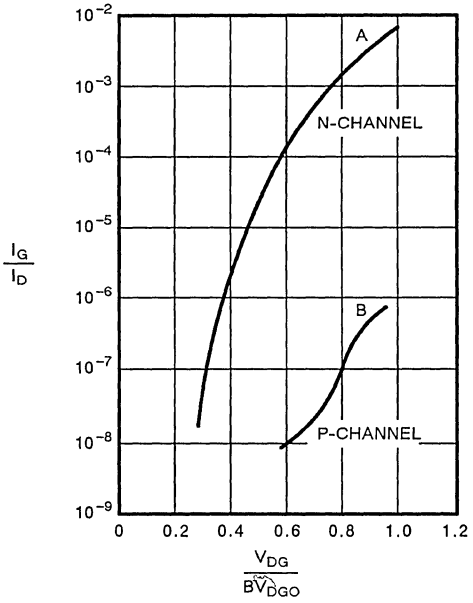


Figure 4. Normalized gate-current (leakage) variations depend upon drain-gate voltage, plotted here for n- and p-channel JFETs.

While Figure 4 illustrates the dependence of current-ratio (leakage) characteristics on drain-gate voltage, it also simultaneously shows this parameter's independence from the type of n-channel JFET – fabrication technique employed. Curve A represents ratios from both a short-channel JFET and a long-channel, high-frequency JFET.

The problem of gate-leakage dependence on drain-gate voltage, however, is a characteristic principally of n-channel devices. The p-channel JFET (represented by curve B in Figure 4) exhibits a response similar to that of the n-channel device, but because of this device's lower mobility and the resulting lower impact ionization, the p-channel curve is pushed out to a higher voltage and, therefore, presents less of a problem.

The Data Sheet's To Blame

Although high gate input resistance is important in many applications including differential and operational amplifiers (as well as in the probe example here), the spec sheets for many JFETs offer no hint of operating gate current.

If you have an application requiring high input resistance, you are thus confronted with something of a problem. If you don't care to tediously characterize selected JFETs yourself, you can only hope that the vendor has overridden the JEDEC format in its catalog and has included operating-gate-current figures. Alternatively, the vendor might offer a graphical presentation of gate-current data as in Figure 3. However this information is presented, be aware that the operating gate-current characteristic for a particular JFET type can vary among manufacturers. Thus, if you change vendors – watch out.

Referring back to the example presented at the beginning of this article, you should understand by now why the probe doesn't perform as expected. The drain-gate voltage is a combination of the +30-V bias supply and the peak negative potential of the 10-V_{RMS} signal appearing at the gate. The gate current, therefore, peaks to nearly 1 μA, and the input resistance falls short of the levels it could attain.

If you want to remedy this problem, one solution is to lower the bias voltage from +30 V to +20 V, thereby increasing the probe's input resistance to an acceptable level. You could, however, choose a better solution that permits high drain voltages and appreciable gate potentials without losing the JFET's unique high gate input resistance by using a cascade circuit similar to the one shown in Figure 5b. In this arrangement, the input JFET's drain potential remains low because of its interaction with the piggyback JFET. Figure 6 compares the gate currents (and thus the input-resistance performance) of the two circuits depicted in Figure 5 and demonstrates the advantage of the dual-JFET configuration.

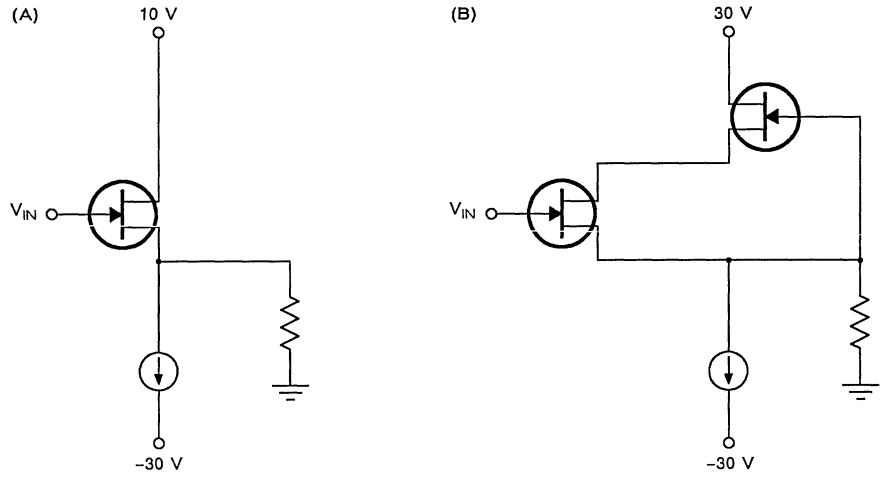


Figure 5. A single-JFET circuit (a) offers simplicity, but it might not provide the high input resistance you want. A cascode dual-JFET alternative (b) solves the input-resistance problem.

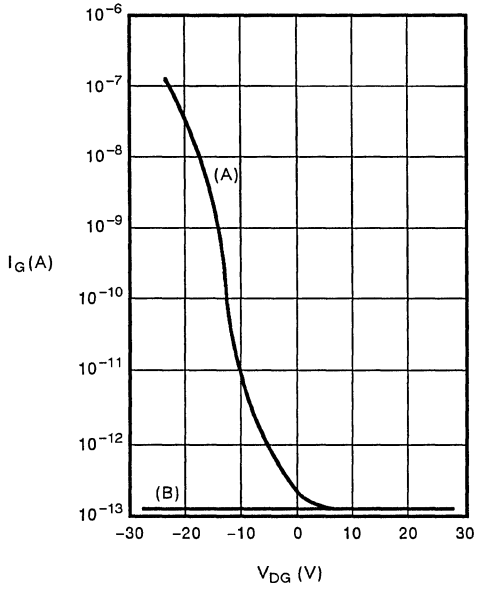


Figure 6. A plot of gate current for both circuits in Figure 5 reveals that the dual-JFET one maintains its low gate current over a much wider operating-voltage range.

AUDIO-FREQUENCY NOISE CHARACTERISTICS OF JUNCTION FETS

Bruce Watson

INTRODUCTION

The purpose of this application note is to identify and characterize audio frequency noise in junction field-effect transistors (JFETs). Emphasis is placed on basic device characteristics rather than on end applications, since it is important for the circuit designer to know the salient noise behavior of the JFET and how those characteristics may be specified by production-oriented test parameters.

Defining the FET Noise Figure

For analysis, it is convenient to represent noise in a FET by assuming that an ideal noise-free device has two external noise sources, $\bar{e}_n$ and $\bar{i}_n$. These noise sources are chosen to have the same output as an actually noisy FET. An equivalent circuit is shown in Figure 1.

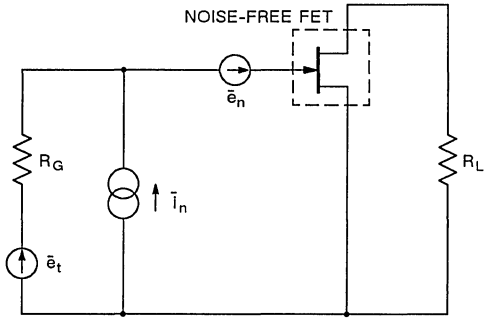


Figure 1. Representing Noise in an Ideal FET

A noise factor (F) is a Figure of Merit of a device with respect to the resistance of a generator. To calculate a noise factor, a source resistor, R_G, with a thermal noise voltage, $\bar{e}_T$, is added to the circuit.

A noise factor (F) may be defined as

$$F = \frac{\text{Total available output noise power}}{\text{Noise power at output due to thermal noise of } R_G}$$

or

$$F = \frac{\text{Noise power output due to } R_G + \text{noise power output due to FET}}{\text{Noise power output due to } R_G}$$

or

$$F = 1 + \frac{\text{Noise power output due to FET}}{\text{Noise power output due to } R_G}$$

or

$$F = 1 + \frac{\text{Gain X noise power of FET referred to input}}{\text{Gain X noise power due to } R_G}$$

or

$$F = 1 + \frac{\text{Noise power of FET referred to input}}{\text{Noise power due to } R_G}$$

The thermal noise voltage across R_G is

$$\bar{e}_T = \sqrt{4kTR_GB} \qquad (1)$$

where $k = 1.380 \times 10^{-23}$ Joules/°K (Boltzmann's Constant), T = temperature in °K, and B = bandwidth in Hz. Therefore, noise power due to R_G is

$$\frac{\bar{e}_T^2}{R_G} = \frac{4kTR_GB}{R_G} = 4kTB \qquad (2)$$

The noise power of the FET referred to the input is

$$\frac{\bar{e}_n^2}{R_G} + \bar{i}_n^2 \cdot R_G \qquad (3)$$

When expressions for the noise power of both the FET and R_G are substituted, the noise factor becomes

$$F = 1 + \frac{\bar{e}_n^2 + \bar{i}_n^2 R_G^2}{4kTR_GB} \qquad (4)$$

A noise figure (NF) expressed in dB indicates the presence of added noise power from the FET or another active device. The noise figure is always given with reference to a standard, specifically the generator resistance R_G:

$$NF = 10 \log_{10} [F] \quad (5)$$

The noise figure of the FET is

$$NF = 10 \log_{10} \left[1 + \frac{\bar{e}_n^2 + \bar{i}_n^2 R_G^2}{4kTR_GB} \right] dB \quad (6)$$

When junction FET noise is expressed in terms of the noise figure (NF), an inherent disadvantage arises because the noise figure value is dependent upon the value of the generator resistance, R_G. Therefore, the $\bar{e}_n$, $\bar{i}_n$ method remains as the best way to quantitatively express the noise characteristics of the FET.

Describing Junction FET Noise Characteristics

Junction FET $\bar{e}_n$ and $\bar{i}_n$ characteristics are frequency-dependent within the audio noise spectrum and take the form as shown in Figure 2.

$\bar{e}_n$, the equivalent short circuit input noise voltage (with the exception of the $1/f^n$ region), is defined as

$$\bar{e}_n = \sqrt{4kTR_NB} \quad (7)$$

where $R_N \approx 0.67/g_{fs}$, the equivalent resistance for noise. The $\bar{e}_n$, except in the $1/f^n$ region, closely approximates the equivalent thermal noise voltage of the channel resistance.

In the so-called $1/f^n$ region, $\bar{e}_n$ is expressed as

$$\bar{e}_n = \sqrt{4kTR_NB\,(1 + f_1/f^n)} \quad (8)$$

where n varies between 1 and 2 and is device- and lot-oriented.

The characteristic bulge in $\bar{e}_n$ in the $1/f^n$ region has been observed to some extent in all junction FETs submitted for testing. The breakpoint or corner frequency shown as f_1 in Figure 2 is lot- and device design-oriented, and varies from about 100 Hz to 1 kHz.

As indicated in Equations (7) and (8), $\bar{e}_n$ is inversely proportional to the square root of the transconductance of the FET ($\bar{e}_n \propto 1/\sqrt{g_{fs}}$). $\bar{e}_n$ can be lowered by a factor of $1/\sqrt{N}$ if N devices with matched electrical characteristics are connected in parallel. For example, when

$$N = 2 \quad (9)$$

let

$$\bar{e}_{n1} = \bar{e}_{n2} \quad (10)$$

and let

$$g_{fs1} = g_{fs2} \quad (11)$$

Thus,

$$g_{fs}\ \text{TOTAL} = 2\,g_{fs1} \text{ or } 2\,g_{fs2} \quad (12)$$

From equation (7)

$$\bar{e}_{n1} = \sqrt{4kT\,(0.67/g_{fs1})\,B} \quad (13)$$

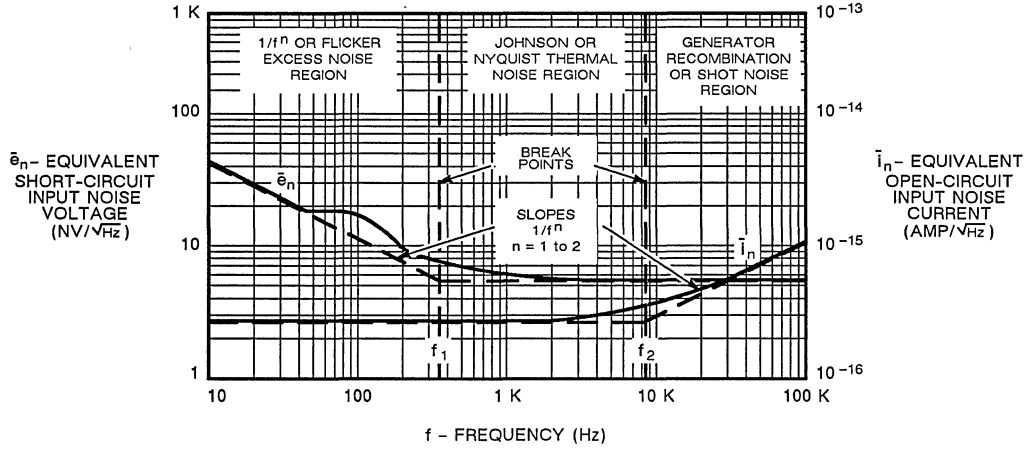


Figure 2. Characteristics of Junction FET Noise

and

$$\bar{e}_n \text{ TOTAL} = \sqrt{4kT\ (0.67/\ 2g_{fs1})\ B} \qquad (14)$$

Thus,

$$\bar{e}_n \text{ TOTAL} = \frac{1}{\sqrt{2}}\ \bar{e}_{n1} \qquad (15)$$

A second way to achieve low $\bar{e}_n$ is to use a device with a large gate area. Empirically, $\bar{e}_n$ is inversely proportional to the square of the gate area ($\bar{e}_n \propto 1/A_G^2$), independent of g_{fs} . This large gate area philosophy has been followed in the design of the Siliconix 2N4867A FET, and noise performance of the device is discussed later in this application note. A major advnatage of this design is that $\bar{e}_n$ is significantly lowered and $\bar{i}_n$ also remains at a low value.

The equivalent open-circuit input noise current, $\bar{i}_n$, with the exception of the shot noise region shown in Figure 2, is due to thermally-generated reverse current in the gate channel junction. It is defined as

$$\bar{i}_n = \sqrt{2\,q\,I_G B} \qquad (16)$$

where $q = 1.602 \times 10^{-19}$ coulomb (the magnitude of the electron charge), I_G is the measured dc operating gate current in amperes, and B is bandwidth in Hz. The expression is accurate only when the measured gate current is the result of bulk device conductance. It is possible for the measured gate current to be due to conductance stemming from contamination across the leads of the semiconductor package.

At higher frequencies, as in the shot noise region shown in Figure 2, $\bar{i}_n$ can be approximated as being equal to the Nyquist thermal noise current generated by a resistor:

$$\bar{i}_n = \sqrt{\frac{4kTB}{R_p}} \qquad (17)$$

where R_p is the real part of the gate-to-source input impedance. The breakpoint or corner frequency f_2 in Figure 2 is lot- and device design-oriented and can vary from 5 kHz to 50 kHz.

Another form of noise found in junction FETs is known as "popcorn" or burst noise; the term popcorn noise was originated in the hearing aid industry because of noise or level shifts which are present in input stages, and which resemble the sound of corn popping.

Popcorn noise is a form of random burst input noise current which remains at the same amplitude and which is confined to frequencies of 10 Hz or lower. The suitability of a FET device is dependent on the amplitude of the burst, its duration, and its repetition rate. The origins of popcorn noise are not completely identified, but are believed to be caused by intermittent contact in aluminum-silicon interfaces and by contamination in the oxidatin processes.

A test circuit to measure popcorn noise in differential junction FET amplifiers is shown in Figure 3. In practice, popcorn noise is evaluated on an engineering basis, not on a production-line basis. No correlation between $1/f^n$ noise at 10 Hz and popcorn noise has yet been found in junction FETs. However, if the amplitude of the burst is large and occurs frequently, then $1/f^n$ noise voltage ($\bar{e}_n$) is masked and difficult to evaluate at 10 Hz.

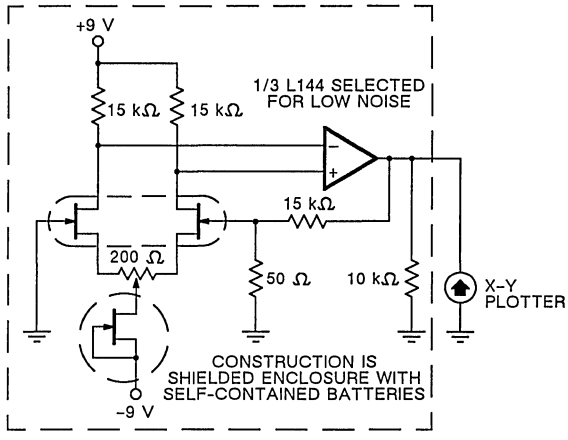


Figure 3. Test Circuit to Measure Popcorn Noise

The graph in Figure 4 shows "moderate" burst noise observed in a group of junction FET differential amplifiers which were measured in the test circuit.

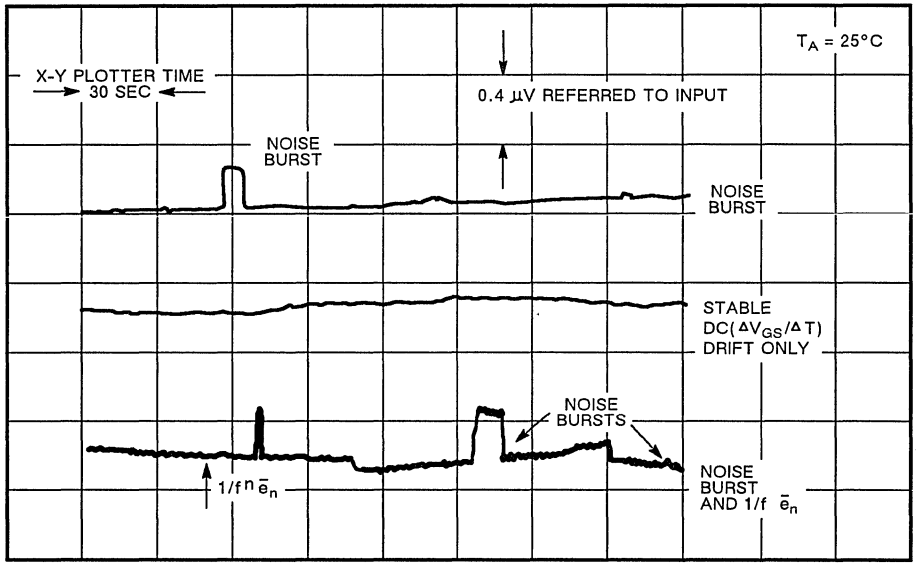


Figure 4. Popcorn Noise in Differential Amplifiers

Operating Point Considerations

Unlike bipolar transistors, where $\bar{e}_n$ and $\bar{i}_n$ characteristics vary directly with changes in the collector current (I_C), similar characteristics in junction FETs will vary only slightly as drain current (I_D) is varied. This is true as long as the FET is biased so that the drain-source voltage is greater than the pinch-off voltage ($V_{DS} > V_p$ or $V_{GS(off)}$).

The $\bar{e}_n$ in junction FETs will be lowest when the devices are operated at V_{GS} = 0 ($I_D = I_{DSS}$), where transconductance (g_{fs}) is at its highest value. This will be true only if device dissipation is maintained very low in relation to the total dissipation capability of the FET.

The curves shown in Figure 5 illustrate changes in $\bar{e}_n$ as the operating drain current (I_D) is varied. Note that the lowest $\bar{e}_n$ did not occur at V_{GS} = 0 because of high power dissipation and a resultant rise in junction temperature at the operating point.

The optimum (lowest) $\bar{i}_n$ in depletion-mode junction FETs should occur at V_{GS} = 0 ($I_D = I_{DSS}$). In practice, very little change will be seen in I_D when the operating point is changed, provided that the drain-gate voltage is maintained below the gate current (I_G) breakpoint and power dissipation is kept at a low level. The curves shown in Figure 6 illustrate $\bar{i}_n$ characteristics as a function of drain-gate voltage at points below, on, and above the I_G breakpoint voltage.

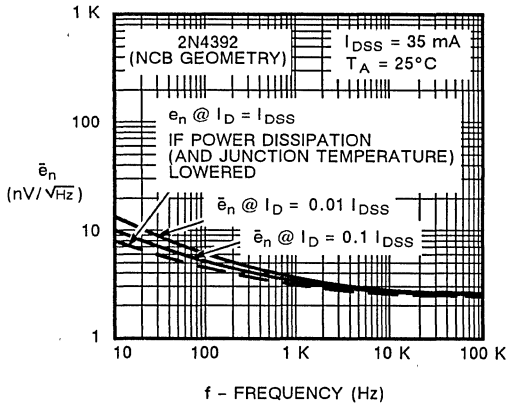


Figure 5. $\bar{e}_n$ Changes vs. I_D Variations

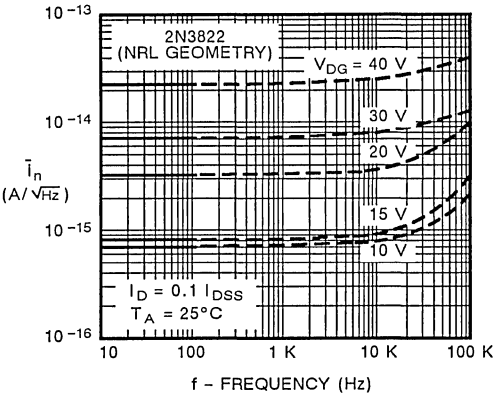


Figure 6. $\bar{i}_n$ Characteristics as Function of Drain-Gate Voltage

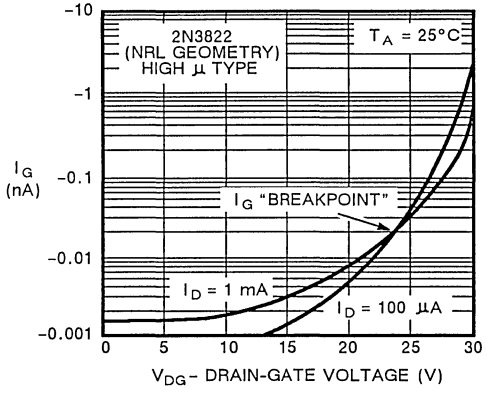


Figure 7. Gate Operating Current vs. Drain-Gate Voltage

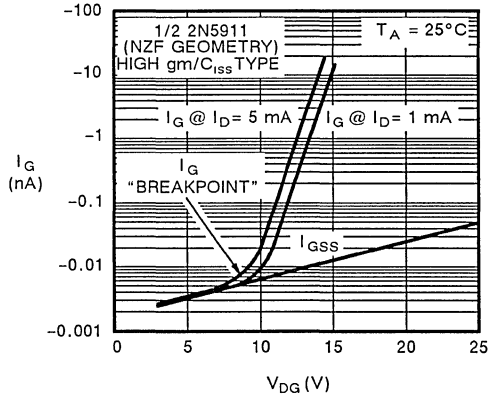


Figure 8. Gate Current vs. Drain-Gate Voltage

In circuit design, particular attention must be paid to drain-gate voltage (V_{DG}) to minimize gate current (I_G) under operating conditions. The critical drain-gate voltage (I_G breakpoint voltage) can be anywhere from 8 to 40 V, depending on device design. Gate operating current (I_G) should not be considered equal to gate reverse current (I_{GSS}) in linear amplifier applications. I_{GSS} is only an indication of reverse-biased junction leakage under non-operating conditions. The curves shown in Figures 7 and 8 reveal how the I_G breakpoint is related to basic device design. Device designs with a high g_{fs}/C_{iss} ratio have low breakpoint voltages, typically at V_{DSG} = 10 V; whereas, high μ devices ($\mu = r_{ds} \cdot g_{fs}$) have much higher I_G breakpoints, typically V_{DG} = 20 – 30 V.

Characteristics of $\bar{e}_n$ and $\bar{i}_n$ at Low Temperature

Three equations presented earlier [(7), (16) and (17)] show that $\bar{e}_n$ and $\bar{i}_n$ are temperature dependent. $\bar{e}_n$ and $\bar{i}_n$ are proportional to $\sqrt{T}$, and both will be reduced if the temperature is lowered. In Equation (16), $\bar{i}_n$ is proportional to $\sqrt{I_G}$; I_G will halve for each temperature drop of 10 to 11 °C. $\bar{e}_n$ is also proportional to $\sqrt{R_N}$, where $R_N \approx 0.67/g_{fs}$. Thus when g_{fs} is increased, which is typical of junction FETs operating at low temperature, $\bar{e}_n$ will also become lower.

In Figure 9, g_{fs} has been plotted vs. temperature for silicon junction FETs, and the low temperature limitation caused by a drop-off in g_{fs} is clearly shown.

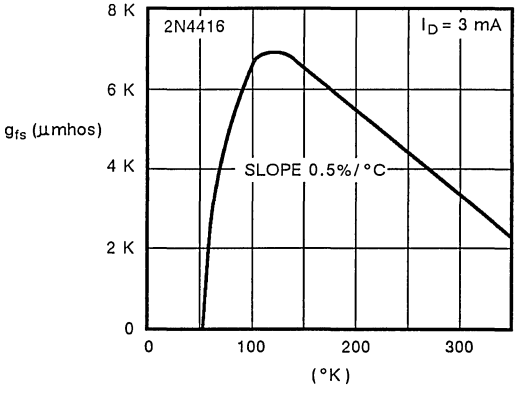


Figure 9. g_{fs} vs. Temperture

In connection with the plot of g_{fs} vs. temperature, note that the relationship can vary from approximately 0.2% to 1% per °C. The g_{fs} slope depends upon the basic design of the FET and upon the proximity of the drain current operating point to I_{DZ}, the zero temperature coefficient point.

The major application of junction FETs at low temperature is in charge-sensitive amplifiers. For best performance in this type of application, a high g_{fs}/C_{lss} ratio is required. Recommended Siliconix FET types for such applications are the 2N4416 and the U310.

Test Measurements

By definition, $\bar{e}_n$ and $\bar{i}_n$ are referred to the input of the device under test. To measure $\bar{e}_n$, the test circuit shown in Figure 10 will prove useful.

The following procedure should be used to make the $\bar{e}_n$ test:

1. Set the tunable filter to the required f_{low} and f_{high}. Adjust the oscillator to the mean center frequency [$f_{mean} = (f_{low} \bullet f_{high})^{1/2}$].

2. Set V_{OSC} to 100 mV with Switch 1 in position ①.

   Computer $V_{in1} = 10^{-1} \times \frac{10^2}{16^6} = 10^{-5}$ V = 10 μV.

3. Measure V_{OUT1}. Compute overall gain as

   $A_V = \frac{V_{OUT1}}{V_{in1}} = \frac{V_{OUT1}}{10\ \mu V}$.

4. Set Switch 1 to position ② and measure V_{OUT2}. Compute V_{in2}, the equivalent short-circuit input noise voltage ($\bar{e}_n$), using A_V from Step 3.

   $V_{in2} = \frac{V_{OUT2}}{Av} = \bar{e}_n$ in volts over band-

   band f_{low} to f_{high}.

An alternate method of performing the above test uses a Quan-Tech Transistor Noise Analyzer consisting of a Model 2173 Control Unit and a Model 2181 Filter. The analyzer has provision for measuring $\bar{e}_n$ and determining NF with various values of R_G in FET and bipolar devices with selectable test conditions. The measuring system has a constant gain of 10,000. The analyzer records output noise at selected frequencies between 10 Hz and 100 kHz in the device under test, with the scale shown as the actual output divided by 10,000. This is then the output noise referred to the input. The equivalent bandwidth for testing is 1 Hz.

There are certain instances where the test circuit or the Transistor Noise Analyzer are not adequate to measure $\bar{e}_n$ at certain frequencies over certain bandwidths in the $1/f^n$ region. The RMS noise over a bandwidth from f_{low} to f_{high}, where there is a $1/f^n$ characteristic over the entire range, can be computed as

$$\bar{e}_n = \left[\bar{e}_n \text{ known}\right] \bullet \left[f_{known} \bullet \ln\left(\frac{f_{high}}{f_{low}}\right)\right]^{1/2n} \quad (18)$$

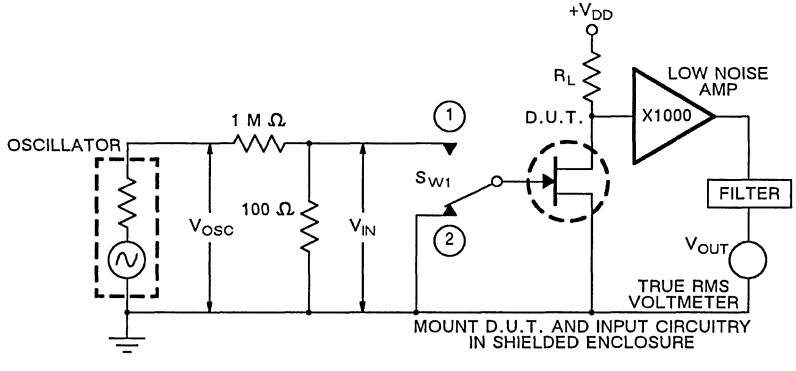


Figure 10. Test Circuit to Measure $\bar{e}_n$

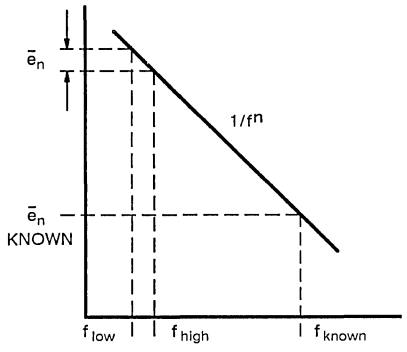


Figure 11. Computing rms Noise Over a Bandwidth

Figure 11 represents this equation graphically. For example, $\bar{e}_n$ known = 70 x 10^{-9} $V/\sqrt{Hz}$ at 10 Hz. How much noise is in the band from 4.5 to 5.5 Hz? The noise has a $1/f^1$ characteristic over the entire range. Thus

$$\bar{e}_n = \left[70 \times 10^{-9}\right] \cdot \left[10 \cdot 1n\left(\frac{5.5}{4.5}\right)\right]^{1/2} \text{Volts} \qquad (19)$$

or

$$\bar{e}_n = 99.16 \times 10^{-9}\ V/\sqrt{Hz} \ @\ 4.975\ Hz, \qquad (20)$$

4.975 Hz is the mean center frequency where $f_{mean} = (f_{low} \cdot f_{high})^{1/2}$.

$\bar{i}_n$ measurements are difficult to implement at best. At frequencies below f_2 in Figure 2, $\bar{i}_n$ is assumed to have a constant level or "white" noise characteristic which may be correlated to gate current, I_G. From Equation (16) I_G is established as the measured bulk gate current. Because measured gate current (I_G) is the result of all conductances at the gate, the resulting gate current and the computed $\bar{i}_n$ due to bulk material can be assumed to be this value or less.

The total equivalent input noise of the FET can be approximated by

$$\bar{e}_{ni}^2 = \bar{e}_T^2 + \bar{e}_n^2 + \bar{i}_n^2 \cdot R_G^2 \qquad (21)$$

where $\bar{e}_T^2$ is the thermal noise of the generator resistance R_G and $\bar{e}_{ni}^2$ is the total noise referred to the input. This approximation assumes that the equivalent noise voltage and the current generators vary independently. Equation (21) implies that $\bar{i}_n^2$ can be calculated if $\bar{e}_T^2$ and total noise $\bar{e}_{ni}^2$ are known. The difficulty here is that in MOS or junction FETs, the R_G must be very large to detect the anticipated small value of $\bar{i}_n$. However, when R_G is very large, $\bar{e}_T^2$ is much greater than $\bar{i}_n^2 \cdot R_G^2$. For example, over a 1-Hz bandwidth at 25°C, if R_G is equal to 100 MΩ, then

$$\bar{e}_T^2 = 4kTR_G$$
$$= 4 \times 1.38 \times 10^{-23} \times 2.95 \times 10^2 \times 10^8$$
$$= 1.63 \times 10^{-12}\ V/\sqrt{Hz}. \qquad (22)$$

Anticipated $\bar{i}_n$ is

$$\bar{i}_n \approx 10^{-15}\ \text{Amperes}/\sqrt{Hz} \qquad (23)$$

and

$$\bar{i}_n^2 = 10^{-30}\ \text{Amperes}/\sqrt{Hz}. \qquad (24)$$

Thus

$$\bar{i}_n^2 \cdot R_G^2 = 10^{-30} \cdot 10^{16} = 10^{-14}\ V/\sqrt{Hz}. \qquad (25)$$

Therefore, $\bar{i}_n^2 \cdot R_G^2$ is much less than $\bar{e}_T^2$, which renders this method of finding $\bar{i}_n$ impractical for most common MOSFETs or junction FETs.

An improved method of measuring $\bar{i}_n^2$ is to substitute a low-loss mica capacitor for resistor R_G. The mica capacitor by definition does not have equivalent thermal noise voltage and, thus, Equation (21) becomes

$$\bar{e}_{ni}^2 = \bar{e}_n^2 + \bar{i}_n^2 \cdot X_C^2 \qquad (26)$$

(where X_C = capacitive reactance)

or

$$\bar{i}_n = \frac{(\bar{e}_{ni}^2 - \bar{e}_n^2)^{1/2}}{X_C} \qquad (27)$$

When a 10-pF mica capacitor was used in the evaluation circuit (up to a frequency of 100 Hz), a correlation of from 80 to 90% was obtained when compared to $\bar{i}_n^2$ computed from measured gate current readings. At frequencies above 100 Hz, direct computation of $\bar{i}_n$ via the capacitor method becomes unwieldy because of the rapid decrease in capacitor reactance at these frequencies.

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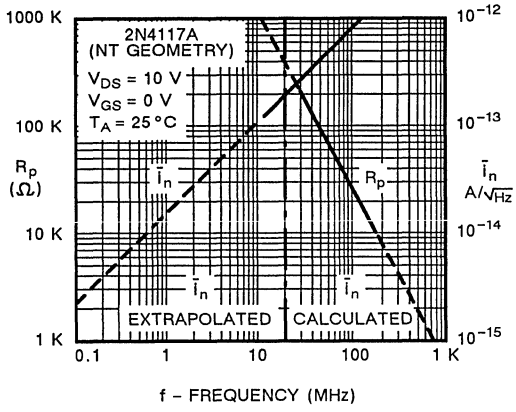


Figure 12. Low-Frequency Limit for Calculated $\bar{i}_n$

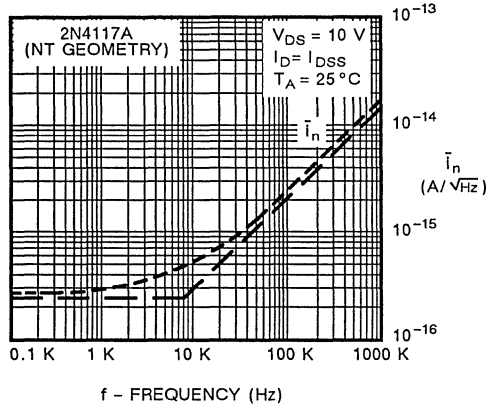


Figure 13. Extrapolated $\bar{i}_n$ vs. Frequency

In calculating $\bar{i}_n$ at higher frequencies, an alternate method is to measure (R_p) the real part of the gate-source impedance of the FET. When R_p is measured at various frequencies, the equivalent short-circuit input noise current ($\bar{i}_n$) can be computed as a function of frequency (see Equation (17). A convenient instrument to measure R_p is the Hewlett-Packard Type 250A Rx meter or equivalent. The 250A Rx meter can measure R_p accurately up to 200 kΩ. As is shown in Figure 12, this establishes the low-frequency limit of 20 MHz for $\bar{i}_n$ computed via direct measurement of R_p for the Siliconix FETs 2N4117A. For frequencies between 100 Hz and 20 MHz, $\bar{i}_n$ must be extrapolated, as shown in Figure 12 and 13. For FET types with lower R_p (such as the Siliconix 2N4393) $\bar{i}_n$ can be computed down to 2 MHz, and, hence, extrapolating $\bar{i}_n$ between 100 Hz and 100 kHz is more accurate.

The curves shown in Figure 14 are representative $\bar{e}_n$, $\bar{i}_n$ curves for Siliconix JFET products. Of particular importance is the geometry which by its design governs the basic noise characteristics of product types derived from it.

CONCLUSION

Contemporary junction FETs have noise voltages ($\bar{e}_n$) equal to those found in low-noise bipolar transistors. Each type of device has a different operating mechanism: the FET is voltage-actuated, while the bipolar transistor is current-actuated. Hence, FETs have an inherently lower noise current ($\bar{i}_n$) and are preferred over bipolar devices in most audio-frequency applications where low-noise performance is a design requirement.

When bias points are properly selected, as described in this application note, the excellent low-noise characteristics of high g_{fs} junction FETS can be realized.

The process geometry of the basic FET design of the FET governs the noise characteristics of product types derived from it. Readers are invited to refer to the Siliconix FET catalog for full geometry performance data and for specific part numbers stemming from the generic process geometries.

The measurement section of this application note showed that direct $\bar{e}_n$ measurements can readily be made. $\bar{i}_n$ can be guaranteed at frequencies below 100 Hz by measuring the dc operating gate current (I_G). When I_G is known, $\bar{i}_n$ can be extrapolated from frequencies below 100 Hz to predict noise performance at frequencies to 100 kHz.

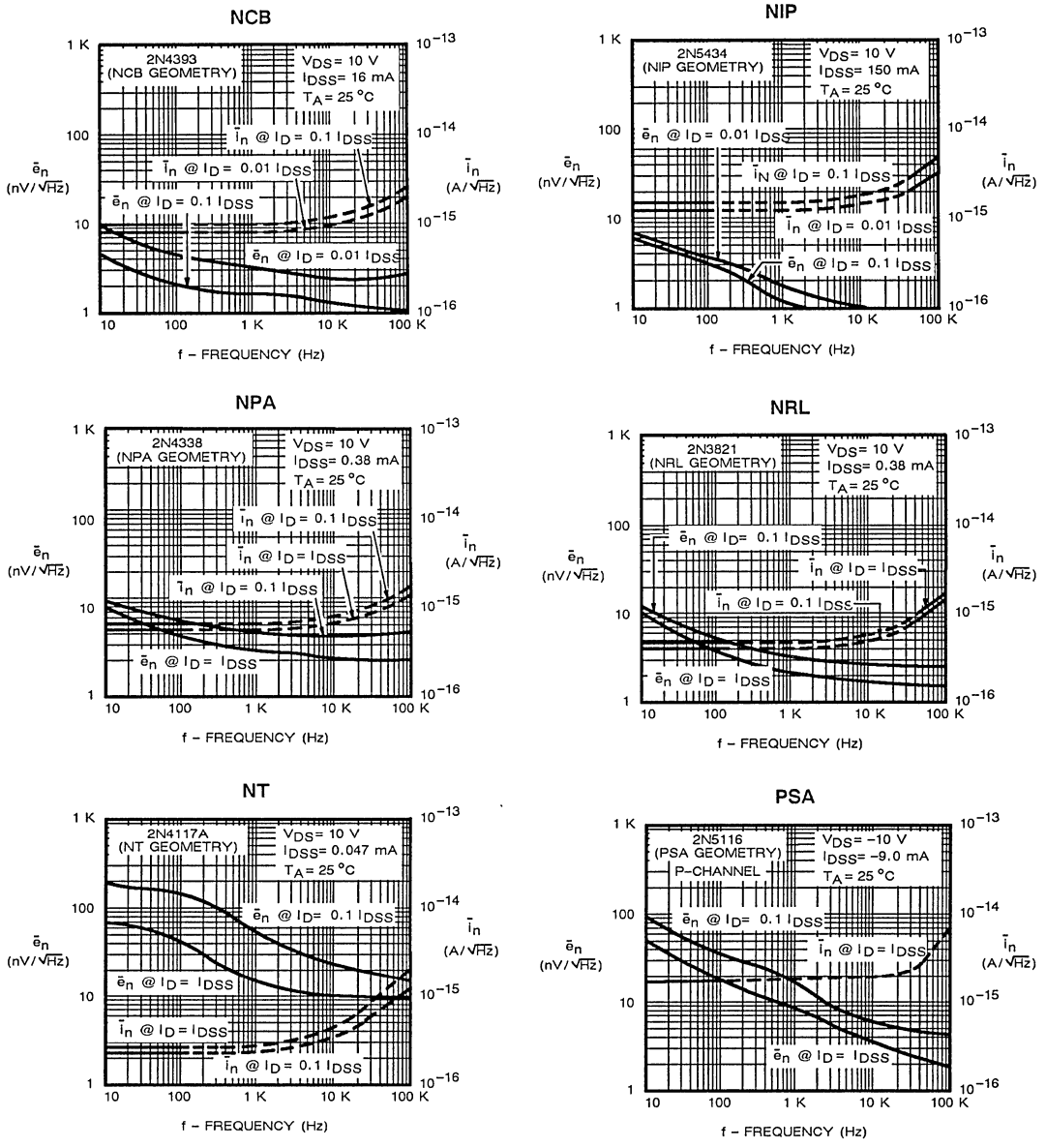


Figure 14. Noise Characteristics by Geometry

9

JFETS FOR VIDEO AMPLIFIERS

INTRODUCTION

The field-effect transistor lends itself well to video amplifier applications. Gain bandwidth products in excess of 250 MHz may be easily achieved using simple one- or two-transistor circuits. DC input resistances in the tens of MΩ range may also be easily achieved while input capacitances may be significantly reduced to less than 1 pF by well-known circuit techniques. Video amplifiers have applications in communications and pulse amplifying circuits and normally operate up to 100 MHz.

Behavior of JFET Input Resistance

A prime JFET parameter, input impedance, has a large effect in determining the frequency response of a JFET video amplifier. It is not a simple RC network, but one in which the real and imaginary parts are a function of frequency.

The voltage generator source resistance R_G and the JFET input impedance Z_{IN} form a frequency sensitive attenuation network. The larger the R_G, the worse will be the frequency response and vice versa. Examining this in greater detail, consider the input equivalent circuit of a JFET connected in the common source configuration,

where

R_{gs} and R_{gd} = bulk series gate resistance
C_{gs} and C_{gd} = bulk series gate capacitance
g_{oss} = output conductance

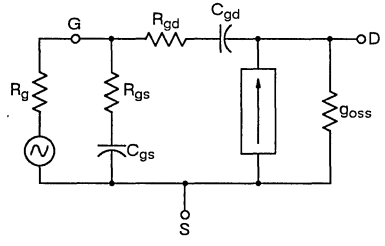


Figure 1.

For this analysis the gate source leakage resistance has been ignored due to its high value. Redrawing the input equivalent circuit as a simple parallel resistance-capacitance combination results in

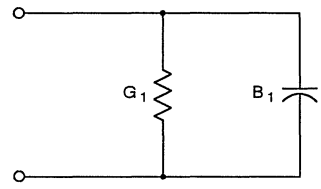


Figure 2.

where

$$G_1 = \mathrm{Re}\,|Y_{in}|$$

$$= \frac{\omega^2 [T_1C_1(1+\omega^2 T_2^2) + T_2C_2(1+\omega^2 T_1^2)]}{1-(\omega^2 T_1T_2)^2 + \omega^2(T_1^2+T_2^2)} \quad (1)$$

and

$$B_1 = I_m\,|Y_{in}|$$

$$= \frac{\omega [C_1(1+\omega^2 T_2^2) + C_2(1+\omega^2 T_1^2)]}{1-(\omega^2 T_1T_2)^2 + \omega^2(T_1^2+T_2^2)} \quad (2)$$

where

$$T_1 = C_{gd}R_{gd}$$
$$T_1 = C_{gs}R_{gs} \quad (3)$$

The input resistance varies inversely with the square of the frequency (see Figures 3 and 4), while the input reactance is inversely proportional to the frequency (see Figure 3).

In common-source circuits, $1/G_1$ will typical fall to $< 2\ k\Omega$ at 100 MHz while C_1 remains substantially constant at least up to 1000 MHz. Figures 3 and 4 exhibit these relationships.

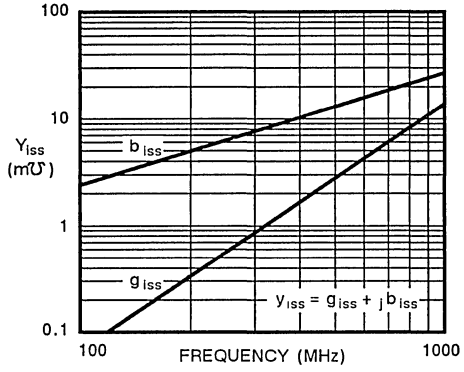
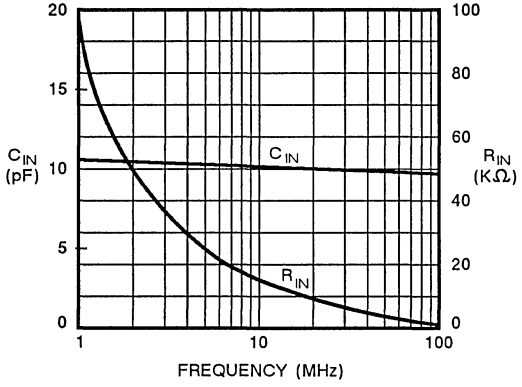
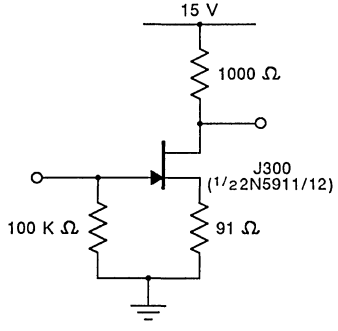


Figure 3



a.



b.

Figure 4

To maintain low input capacitance and, thus, a high input impedance over a wide frequency range, feedback may be applied to most circuits. Such techniques are explored in "JFET and Bipolar Cascade" section of this application note. The effect of R_G on the frequency response is shown in Figures 6, 9, 11, and 13 where various amplifier configurations are investigated.

Circuits to Consider

The following five video amplifier circuits are considered.

1. Common-Source Configuration
2 Shunt-Peaked Common-Source Configuration
3. Source Follower
4 Cascode Amplifier
5. JFET and Bipolar Cascade

Common-Source Circuit

The circuit shown in Figure 5 features high input impedance and high voltage gain. The drain resistor is set at 560 Ω to maintain good bandwidth which, with 50-Ω generator impedance, is determined primarily by the drain load components. These are:

$$R_D = 560\,\Omega \tag{4}$$

$$C_T = C_{gd} + C_D + C_S \tag{5}$$

C_{gd} = 2.0 pF, C_D the VTVM probe, 2.0 pF, and C_S is circuit stray capacitance of 3 pF.

$$C_T = 2 + 2 + 3 = 7\ \text{pF} \tag{6}$$

The 3-dB frequency ω_3 is given by

$$\omega_3 = \frac{1}{C_T R_D} \tag{7}$$

$$= \frac{1}{7 \times 10^{-12} \times 560} \tag{8}$$

$$\omega_3 = 255 \times 10^6 \tag{9}$$

$$f_3 = 39\ \text{MHz} \tag{10}$$

9

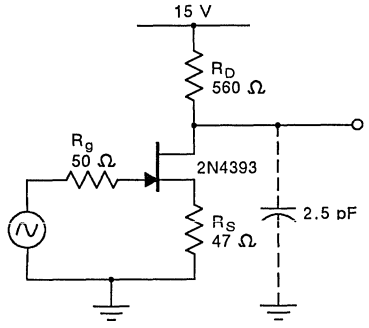


Figure 5

The low frequency voltage gain for this configuration is given by:

$$A_V = \frac{g_{fs}R_D}{1 + g_{fs}R_S} \quad (11)$$

$$A_V = 4.9 \quad (12)$$

where

g_{fs} = 15 m℧ when

I_D = 12 mA, the quiescent current

$$R_D = 560\,\Omega \quad (13)$$

$$R_D = 47\,\Omega \quad (14)$$

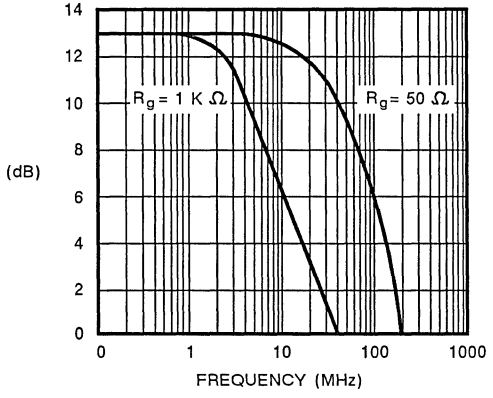


Figure 6

Measured Performance

Figure 6 shows the frequency response of the circuit. The low-frequency gain was measured at 4.5 and the 3-dB bandwidth at 44 MHz giving a gain bandwidth product of 197 MHz. This compares with a calculated gain bandwidth of 191 MHz.

Effect of Increasing Generator Impedance

If the generator resistance R_G is increased to 1 k Ω, the input time constant of the JFET is increased. The bandwidth of the amplifier is now determined primarily by the input time constant which consists of generator impedance (R_G = 1 k Ω) shunted by C_{in} (see Figure 7).

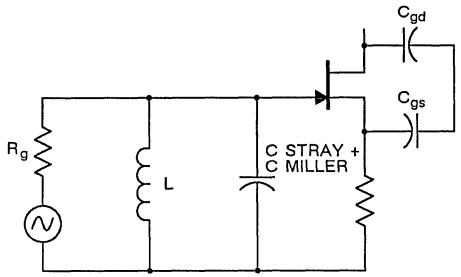


Figure 7

where

$$C_{in} = (1 + \frac{g_{fs}R_D}{1 + g_{fs}R_S})C_{gd} + (1 - \frac{g_{fs}R_S}{1 + g_{fs}R_S})C_{gs} + \text{Strays}$$

$$= (5.9 \times 3.5) + (0.6 \times 10) + 3. \quad (15)$$

$$C_{in} = 30 \text{ pF} \quad (16)$$

where

$$C_{gd} = 3.5 \text{ pF} \quad (17)$$

$$C_{gs} = 10 \text{ pF} \quad (18)$$

The corresponding 3-dB frequency is given by:

$$\omega_3 = \frac{1}{C_{in}R_G} \quad (19)$$

$$= \frac{1}{30 \times 10_{-12} \times 10^3} = \frac{10^9}{30} \quad (20)$$

$$f_3 = 5.3 \text{ MHz} \quad (21)$$

which agrees closely with the measured bandwidth shown in Figure 6.

Shunt-Peaked Common-Source Circuit

The frequency response of the resistance-loaded common-source circuit may be significantly extended by shunt peaking at the gate and/or drain. First, consider the gate circuit. Here an inductor may be connected in shunt with the gate and set to such a value that it forms a tuned circuit with the JFET input capacitance. The frequency of resonance is determined by

$$f_o = \frac{1}{2\pi\sqrt{LC_{in}}} \quad (22)$$

where

$$C_{in} = C_{iss} + C_{Stray} + C_{Miller} \quad (23)$$

The response of an input signal of frequency f_o will then be boosted to an extent depending on the loaded Q of the tuned circuit; the loaded Q, in turn is dependent on the unloaded Q of inductor L, R_G, and the JFET input resistance.

Next, consider shunt peaking in the drain circuit. In Figure 8 the inductor L is set to such a value that a low Q tuned circuit is formed; the resonating capacitance C is the parallel combination of C_{gd} plus stray and load capacitances. For a flat response, the LC circuit is tuned to the 3-dB frequency of the resistance loaded circuit of Figure 5. (See Appendix.)

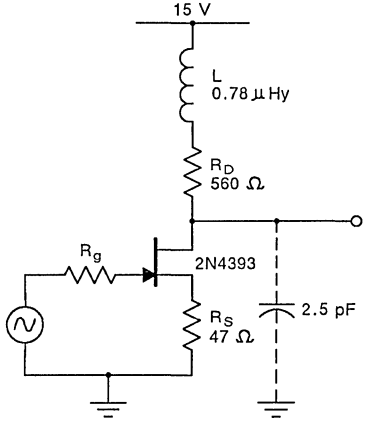


Figure 8

The required value of L is

$$L = \frac{R_D^2\, C}{2}, \text{ and for the cicuit in Figure 8.} \quad (24)$$

$$= 0.78\ \mu H \quad (25)$$

where

$$R_D = 560\ \Omega \quad (26)$$

$$C = C_{gd} + C_{Stray} + C_{VTVM\ PROBE} \quad (27)$$

$$C = 1.2 + 1.3 + 2.5 = 5\ PF \quad (28)$$

Due to the low circuit Q (about 5), the value of L is not critical.

The 3-dB bandwidth shown in Figure 9 now extends to 67 MHz, giving a gain bandwidth product of

$$67 \times 4.2 = 281\ MHz \quad (29)$$

When R_S is bypassed by a 0.1 µF capacitor, the low-frequency voltage gain is given simply by

$$A_V = g_{fs}R_D \quad (30)$$

$$= 15 \times 10^{-3} \times 560 \quad (31)$$

$$= 8.4\ (18.5\ dB) \quad (32)$$

The gain bandwidth product tends to remain constant whether R_S is bypassed or not, and this effect is shown in Figure 9.

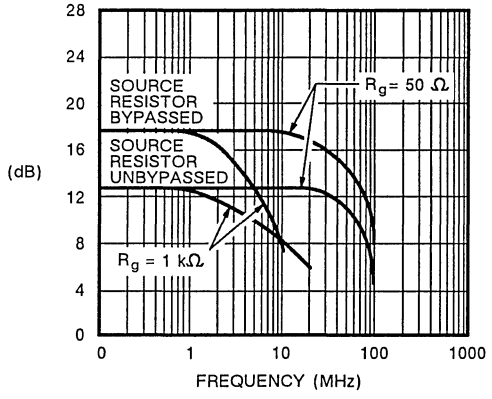


Figure 9

Source-Follower Circuit

A J300 is used in the JFET source-follower circuit Figure 10, because of its low input capacitance and high g_{fs}, which remains high at the frequency range of interest. A source follower exhibits a high input impedance and low output impedance. The real part of the output impedance is the reciprocal of g_{fs} which is independent of frequency up to about 600 MHz. The input capacitance is $C_{gd} + C_{gs}$ (1 - A_V) which, in this case, is approximately 1.5 pF maximum. The input capacitance is also independent of frequency and independent of load when the load is larger than the output resistance R_O.

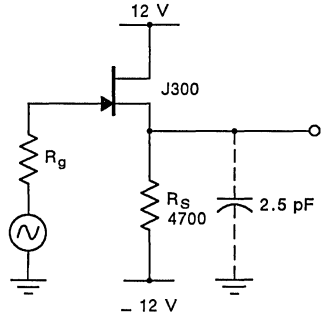


Figure 10

The frequency response is dependent mainly on the generator internal impedance. For example, when R_g is increased to 1kΩ the bandwidth falls to 80 MHz. In this particular circuit, the low-frequency voltage gain is 0.94.

The input resistance is proportional to $1/f^2$ (as explained in the section, "Behavior of JFET Input Resistance) and at some high frequency will go negative, particularly if the source resistor is large. For example, with the circuit shown in Figure 10, the input resistance is high at 10 MHz but in the negative resistance region at 100 MHz. However, when R_S is 1000 Ω, the input resistance is real at this frequency.

The voltage gain of a source follower is given by

$$A_V = \frac{g_{fs}R_S}{1 + g_{fs}R_S} \qquad (33)$$

Thus, A_V is almost independent of R_S when R_S is large. Using typical values for the J300 (or 1/2 2N5912) in Figure 10, the drain current is 3 mA, g_{fs} is 5 mS and R_S is 4700 Ω.

$A_V = 0.96$

which is near the measured value of 0.94. Measured performance is shown in Figure 11. The output resistance of this source follower is given by

$$R_o = \frac{1}{g_{fs}} = \frac{1}{5 \times 10^{-3}} = 200\ \Omega \qquad (34)$$

and in this circuit, R_o was measured at 165 Ω. The source follower is a useful versatile circuit which may be used as an impedance converter, level shifter, buffer stage, or as an input circuit to an op amp or feedback amplifier.

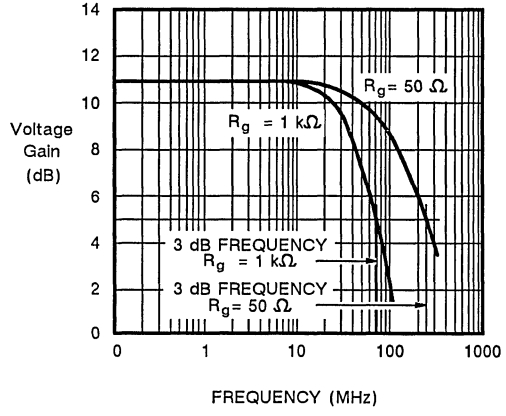


Figure 11

Cascode Circuit

The cascode circuit has applications as a buffer amplifier for use with high-stability oscillators or in low-level power amplifiers[2] mainly due to its low reverse transfer characteristics. The advantages and considerations of this configuration (Figure 12) are similar to those listed for the common-source circuit. An extra advantage exists in the cascode circuit, namely the low input capacitance:

$$C_{in} = C_{gs} + (1 - A_V)\,C_{dg} \qquad (35)$$

$$C_{in} = C_{iss} + C_{gd} \qquad (36)$$

where A_V is the voltage gain from Q_1 gate to Q_1 drain,which is essentially unity. C_{lss} for the 2N5912 dual JFET is 5 pF, and C_{gd} is 1 pF; therefore,

$$C_{in} = 5 + 1 = 6 \text{ pF, excluding strays of 4 pF}$$

Thus, Miller effect is minimized, and a good gain bandwidth product is achieved.

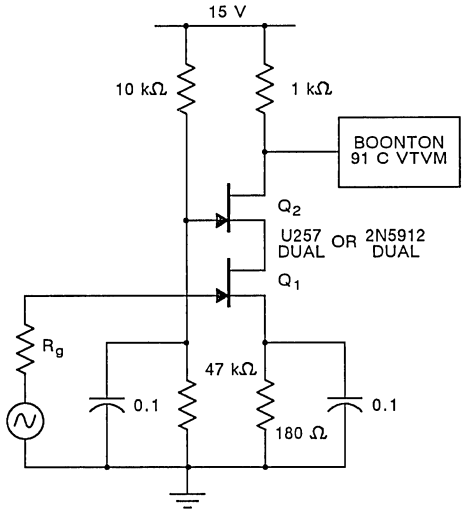


Figure 12

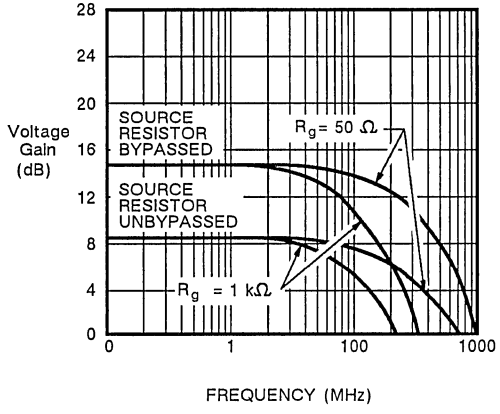


Figure 13

Figure 13 shows cascode frequency response. The voltage gain at low frequency is 15 dB (x 5.6), and the bandwidth is 24.5 MHz with a generator impedance of 50 Ω. The gain bandwidth product is 137 MHz.

JFET and Bipolar Cascade

The JFET and bipolar transistor combination shown in Figure 14 makes a good video amplifier because the JFET input provides the voltage gain, thus obtaining a superior gain bandwidth product. The feedback capacitor ac couples the emitter to the drain. The acvoltage at the gate is nearly equal to that at the source. This source voltage is dc coupled to the base. This produces an A/C voltage at the emitter, whose amplitude is almost equal to that at the base. Thus, at the JFET, $V_g \sim V_s \sim V_d$, and all three signals are in phase. In this way, Miller effect capacitance is largely eliminated.

The frequency response of this circuit is controlled by the output time constant if f_t of the transistor is much greater than the amplifier bandwidth. In the circuit shown the A/C load is 2.5 pF.

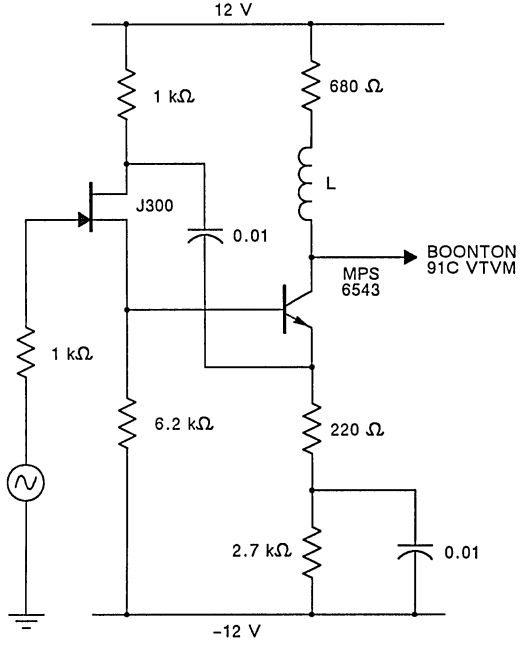


Figure 14

CONCLUSION

The input resistance of a JFET is inversely proportional to the frequency squared, while the input capacitance remains constant to at least 1000 MHz.

Several video amplifier configurations are considered. The common-source circuit is considered first. In the example, the low frequency gain is 4.5 and the 30-dB bandwidth is 44 MHz (gain bandwidth = 197 MHz). By shunt peaking in the drain circuit, gain bandwidth is increased to 260 MHz. The simple source-follower circuit gives a gain near unity with gain bandwidth almost 300 MHz and an output resistance of $1/g_{fs}$. The cascode circuit features a low input capacitance and gain bandwidth of 137 MHz. The circuit featuring the best gain bandwidth is the JFET and bipolar combination, where gain of 11 dB and bandwidth of 90 MHz is achieved.

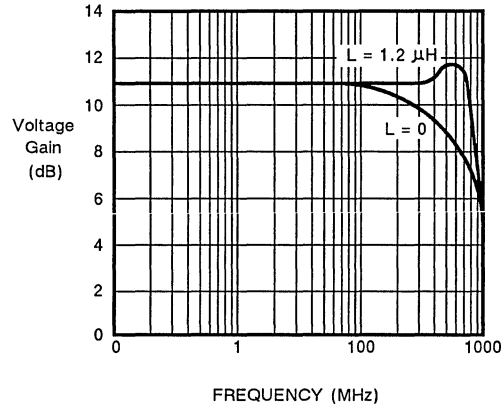


Figure 15

APPENDIX

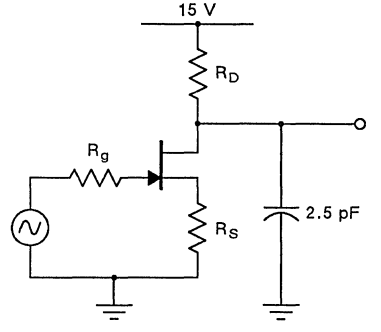
Selection of Video Amplifier Designs with Performance Summary

Note: All output voltages measured with Boonton 91C VTVM.

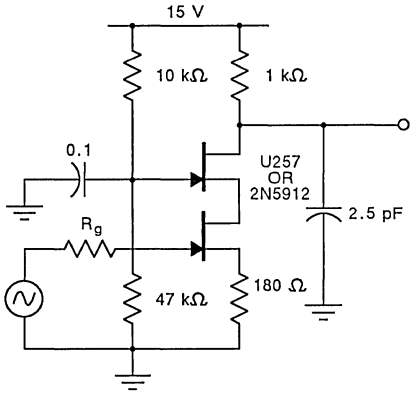
Table 1

DEVICE	R_g (Ω)	R_S Bypassed	R_S (Ω)	R_D (Ω)	GAIN	dB	C_{in} (pF)	BW (MHz)	GBW (MHz)
2N4393	50		47	560	4.5	13.0		44	197
	50	X	47	560	7.5	17.5		40	300
	1 k		47	560	4.5	13.0		5.0	22
	1 k	X	47	560	7.5	17.5		3.5	26
J300	50		91	1 K	3.8	11.6	11.0	27.5	103
1/2	50	X	91	1 K	6.3	16.0	14.5	30.0	189
2N5912	1 k		91	1 K	3.8	11.6	11.0	9.5	36
	1 k	X	91	1 K	6.3	16.0	14.5	6.5	41
2N4416	50		120	1.5 K	3.9	11.8	11.5	25	98
	50	X	120	1.5 K	6.2	15.8	13	19	118
	1 k		120	1.5 K	3.9	11.8	11.5	8	31
	1 k	X	120	1.5 K	6.2	15.8	13	7	44

COMMON SOURCE STAGE

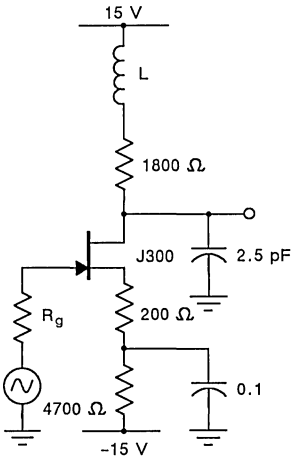


CASCODE



R_g (Ω)	R_S Bypassed	Gain	dB	C_{in} (pF)	BW (MHz)	GBW (MHz)
50		2.7	8.5	9	27	73
50	X	5.6	15	11.5	27	151
1 k		2.7	8.5	9	9.5	73
1 k	X	5.6	15	11.5	9.0	51

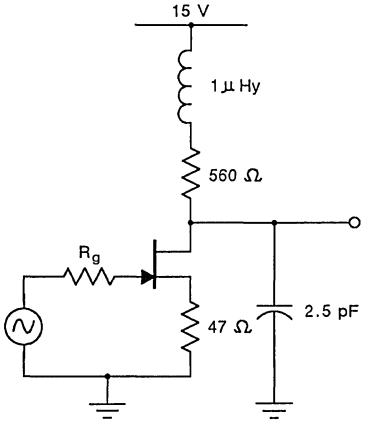
COMMON-SOURCE CIRCUIT



R_g (Ω)	L (μH)	Gain	dB	C_{in} (pF)	BW (MHz)	GBW (MHz)
50	0	3.5	11	2	20	70
1 k	0	3.5	11	2	11	38.5
50	8	3.5	11	2	37	130
1 k	15	3.5	11	2	17	60

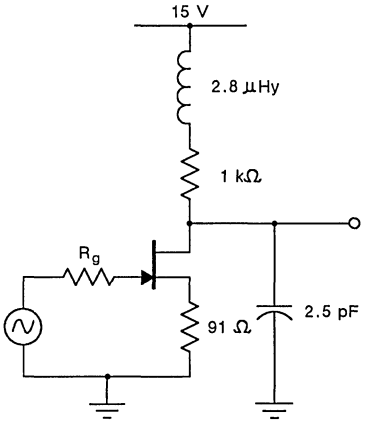
SHUNT-PEAKED COMMON-SOURCE STAGE

2N4393



R_g (Ω)	R_S Bypassed	Gain	dB	BW (MHz)	GBW (MHz)
50		4.2	12.5	66	277
50	X	7.5	17.5	54	405
1 k		4.2	12.5	6.0	25
1 k	X	7.5	17.5	3.5	26

J300
($^1/_2$2N5911/12)

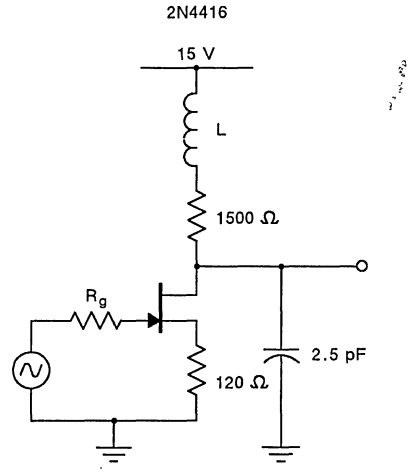


R_g (Ω)	R_S Bypassed	Gain	dB	BW (MHz)	GBW (MHz)
50		3.9	11.8	67	262
50	X	6.3	16.0	67	421

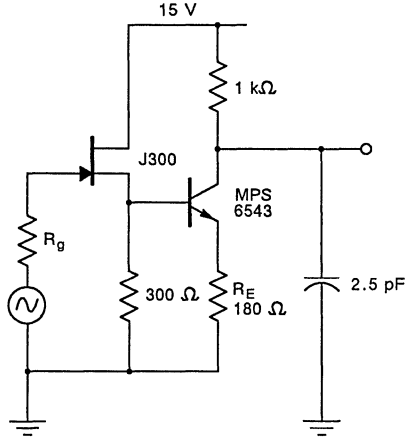
9

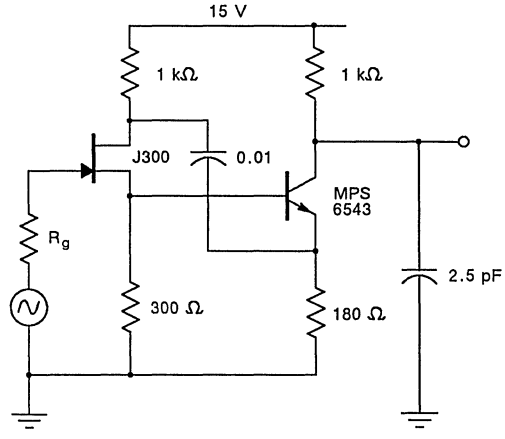
SHUNT-PEAKED COMMON-SOURCES STAGE (Cont'd.)

R_g (Ω)	L (µH)	R_S Bypassed	Gain	dB	BW (MHz)	GBW (MHz)
50	4		3.9	11.8	45	175
50	4	X	6.2	15.8	40	248
50	5	X	6.2	15.8	45	279



COMMON-DRAIN COMMON-EMITTER STAGE

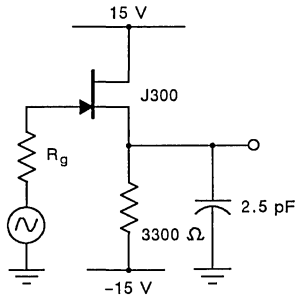


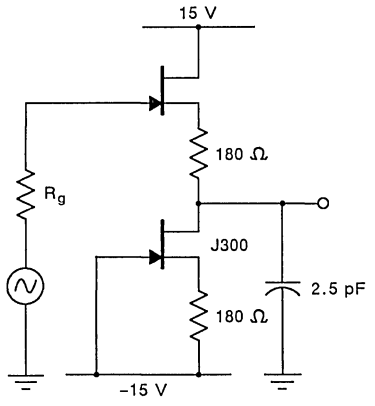


R_g (Ω)	R_S Bypassed (0.1 µF)	Gain	dB	C_{in} (pF)	BW (MHz)	GBW (MHz)
50		3	9.5	2.0	39	117
50	X	25	28	2.0	21	525
1 k		3	9.5	2.0	13	39
1 k	X	25	28	2.0	11	275

R_g (Ω)	Gain	dB	C_{in} (pF)	BW (MHz)	GBW (MHz)
50	5.6	15	1.0	32	179
1 k	5.6	15	1.0	15	84

SOURCE-FOLLOWER CIRCUIT





Rg (Ω)	Gain	Cin (Stray pF)	Total (pF)	Ro (Ω)	BW (MHz)	GBW (MHz)
50	0.92	2.2	2.7	165	350	326
1 k	0.92	2.2	2.7	165	55	50

Dual FET	Rg (Ω)	Offset (Max) (Input to Output) (mV)	Gain	BW (MHz)	GBW (MHz)
U257	50	100	0.98	70	69
2N5912	1 k	100	0.98	15	14.7
U232	50	10	0.98	85	8.3
	1 k	10	0.98	13	12.7

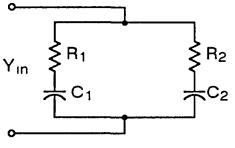
Derivation of Input Admittance Terms

where

$R_1 = R_{gs}$ $C_1 = C_{gs}$ (1)

$R_2 = R_{gd}$ $C_2 = C_{gd}$ (2)

$s = j\omega$



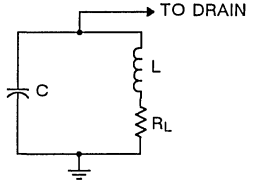
$$Y_{in} = \frac{sC_1}{R_1C_1\,s + 1} + \frac{sC_2}{R_2C_2\,s + 1} \qquad (3)$$

$$= \frac{-\omega^2 C_1C_2(R_1+R_2) + s(C_1+C_2)}{(1-\omega^2R_1R_2C_1C_2) + s(C_1R_1+C_2R_2)} \qquad (4)$$

Derivation of Shunt Peaking Formula

The equivalent circuit of the drain load is shown in the Figure below. The total impedance seen by the drain is given by:

$$Z = \left[\frac{R_L^2 + \omega^2 L^2}{(1 - \omega^2 LC)^2 + \omega^2 C^2 R_L^2}\right]^{1/2} \qquad (5)$$



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The response below shows the "normal" 3-dB frequency without peaking -f_1. It is now required to raise the response at f_1 by 3-dB to achieve a maximally flat response. Therefore, under these conditions the total impedance seen by the drain at f_1 must equal the impedance seen by the drain at f_o. Also, at f_1, $X_C = R_L$. Substituting for X_C in Equation 5:

$$R_L^2 = \frac{R_L^2 + \omega^2 L^2}{(1 - \frac{\omega L^2}{R_L} + 1)} \quad (6)$$

$$R_L^2 - 2\omega L R_L + \omega^2 L^2 + R_L^2 = R_L^2 + \omega^2 L^2 \quad (7)$$

$$R_L^2 = 2\omega L R_L \quad (8)$$

$$R_L = 2\omega L \quad (9)$$

$$L = \frac{R_L}{4\pi f_1} \quad (10)$$

and

$$f_1 = \frac{1}{2\pi R_L C}, \text{ therefore, } L = \frac{R_L^2 C}{2} \quad (11)$$

DESIGNING JUNCTION FET INPUT OP AMPS

INTRODUCTION

Junction FET input operational amplifiers generally consist of a discrete FET differential preamplifier followed by a monolithic bipolar operational amplifier. FET input op amps have a number of advantages over op amps with bipolar transistor input stages. Most of these advantages are attributable to the low input and offset current characteristics of JFET pairs, which are typically three to five orders of magnitude lower than those of bipolar op amps. This is presented graphically in Figure 1.

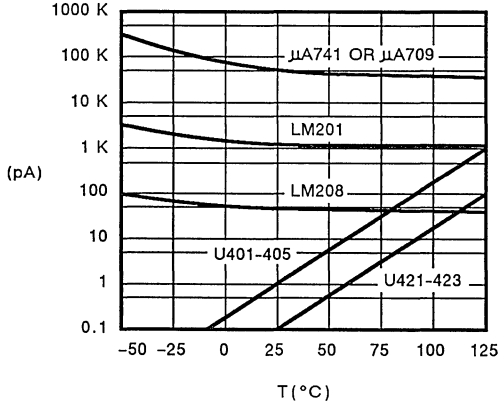

Figure 1. Comparison of Input Bias Currents In Dual FET and Bipolar Op Amps

In integrator circuits, the low offset current of junction FET input op amps permit the integrator charge to be held more than 1000 times longer at 25°C than is possible with a typical bipolar input op amp. FET input op amps also pay off in high impedance amplifier circuits where their low offset current results in low (I_{offset}) x ($R_{generator}$) error voltage.

Behavior of JFET Preamplifiers

FET input op amps usually include a preamplifier constructed of a matched FET pair and a monolithic bipolar op amp. Two configurations of the preamplifier circuit are shown in Figures 2 and 3. These circuits are a common-drain or differential source follower (Figure 2) and a common-source or long tailed pair differential amplifier (Figure 3).

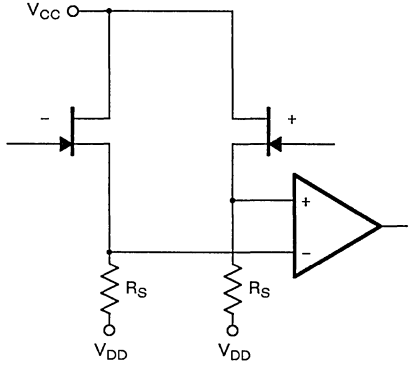

Figure 2. Common-Drain or Differential Source Follower

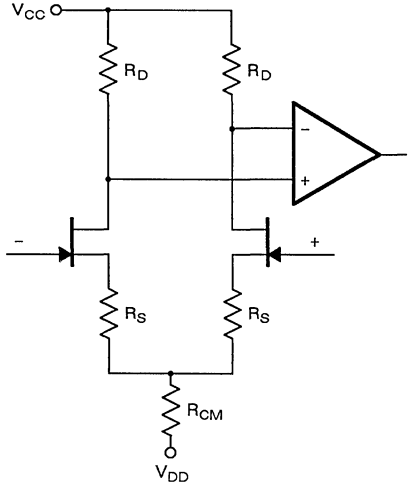

Figure 3. Common-Source Differential Amplifier

The differential common drain (or "source follower") circuit has a differential voltage gain

$$A_{diff} = \frac{R_S}{1 + R_S (g_{fs} + g_{os})} \quad (1)$$

A_{diff} never exceeds unity for the common drain circuit, and only approaches unity for high values of R_S and light loading.

The differential output impedance is twice that of the single-ended output impedance, or

$$Z_{out(diff)} = 2 \left[\frac{R_S + g_{os} R_S^2}{1 + R_S (g_{fs} + g_{os})} \right] \quad (2)$$

Neglecting the output conductance, g_{os}, and assuming R_S is very large, one can arrive at the useful approximation that

$$Z_{out(diff)} \approx \frac{2}{g_{fs}} \quad (3)$$

The common-source (or "long-tailed pair") differential amplifier has a differential voltage gain of,

$$A_{diff} = \frac{-g_{fs} R_D}{1 + g_{os} (R_D + R_S) + g_{fs} R_S} \quad (4)$$

A useful approximation for the case where $R_S = 0$ can be arrived at if, again, g_{os} is neglected. In that instance,

$$A_{diff} \approx -g_{fs} R_D \quad (5)$$

Note that there is a phase inversion between the gate and the drain, and that the value of the common-mode resistor, R_{CM}, does not affect the gain.

The differential output impedance is

$$Z_{out(diff)} = \frac{2 R_D}{\frac{g_{os} (R_D + R_S)}{1 + g_{fs} R_S} + 1} \quad (6)$$

If $R_D << \frac{1}{g_{os}}$ and if $R_S = 0$, then

$$Z_{out(diff)} \approx 2 R_D \quad (7)$$

In the common-source differential amplifier, the addition of R_S lowers the gain and raises the output impedance. Lower gain and higher output impedance will tend to degrade the offset, drift and noise of the FET input amplifier. For this reason it not generally advisable to use source resistors in common-source FET preamplifiers. The use of a source resistor does tend to stabilize the gain of a FET pre-amplifier over the temperature range of the device, but stable open loop gain is not generally of great importance in an op amp.

At low frequencies, input impedance is not a very useful concept for a FET amplifier. It is far more realistic to consider that there is a very small current source, typically ranging from 0.01 to 1000 pA in the gate lead. The value of this current source is dependent on a number of factors. This aspect of op amp applications will be covered in a subsequent section of this Application Note. In general neither the common-drain circuit or the common-source circuit enjoys any particular advantage over the other in terms of input current.

As general rule, a common-source FET preamplifier will produce better results in a FET input op amp than will a common-drain preamplifier. There are three reasons for this superior performance. A common source preamplifier tends to mask the drift and offset of the second stage because of its voltage gain. By the same mechanism, the noise of the second stage is diminished. The third advantage of the common-source preamplifier is that is removes common-mode variations from the input of the second stage. These points will all be considered in more detail in later sections of this Application Note.

Offset and Drift

The offset of a FET pair is the difference in gate-to-source voltage between the two devices when measured at the operating current. Drift is the change of offset with temperature. As is the case with any dc amplifier, the offset and drift of the input devices are indistinguishable from the input signal. Thus offset and drift are erroneous signals, and must be minimized until their magnitude is small in comparison to the input signal.

In a FET input op amp the input FET pair and the second stage both contribute to offset and drift. Figure 4 shows an equivalent circuit for a common-drain FET input op amp, including the sources of offset.

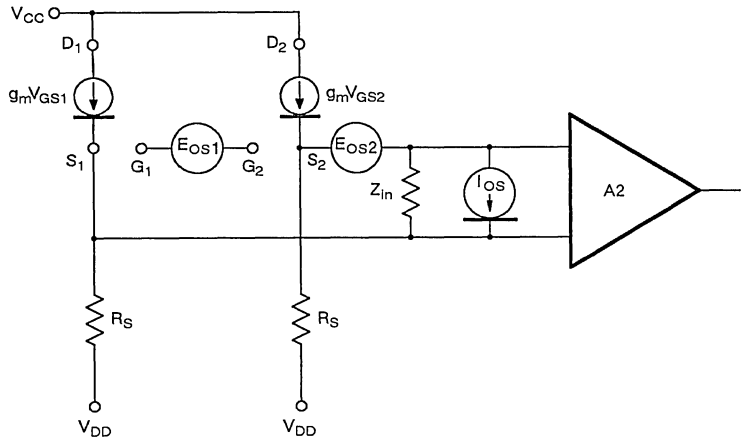

Figure 4. Offset Equivalent Circuit for FET Input Op Amp with Common-Drain Preamplifier

If

R_T = Z_{OUT} of the FET preamp in parallel with Z_{IN} of the second stage,

E_{os1} = Voltage offset of the FET pair,

E_{os2} = Voltage offset of the second stage,

I_{OS} = Current offset of the second stage.

A_1 = Voltage gain of the FET preamplfier,

A_2 = Open-loop voltage gain of the second stage,

E_{Tout} = Total offset error at output of second stage,

E_{TIn} = Total offset from all sources referred to the input, and

g_{fs} = Forward transconductance of the FET at the operating current,

then

$$E_{Tout} = E_{os1} A_1 A_2 + I_{os} R_T A_2 + E_{os2} A_2 \quad (8)$$

and

$$E_{TIn} = \frac{E_{os1} A_1 A_2 + I_{os} R_T A_2 + E_{os2} A_2}{A_1 A_2} \quad (9)$$

or

$$E_{TIn} = E_{os1} + \frac{I_{os} R_T}{A_1} + \frac{E_{os2}}{A_1} \quad (10)$$

Allowing the simplifications $Z_{IN} >> Z_{OUT}$, $g_{os} = 0$, A_1, = 1, and $Z_{OUT} = 2/g_{fs}$, one can obtain an equation for the total offset referred to the input of a FET op amp, using a common-drain preamplifier:

$$E_{TIn} \approx E_{os1} + \frac{2\, I_{os}}{g_{fs}} + E_{os2} \quad (11)$$

If both sides of Equation (11) are divided by ΔT, and equation is derived for total drift referred to the input:

$$\frac{E_{TIn}}{\Delta T} \approx \left(\frac{E_{os1}}{\Delta T}\right) + \frac{2}{g_{fs}} \left(\frac{I_{os}}{\Delta T}\right) + \left(\frac{E_{os2}}{\Delta T}\right) \quad (12)$$

Thus the total drift referred to the input of a FET input op amp with a common drain preamp is approximately the sum of the voltage drift of the FET pair plus the voltage drift of the second stage.

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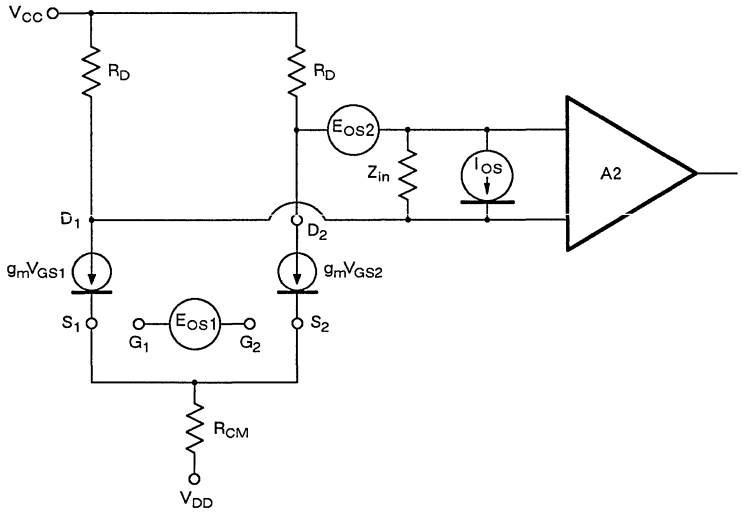

Figure 5. Offset Equivalent Circuit for FET Input Op Amp with Common-Source Preamplifier

Figure 5 shows the offset equivalent circuit for a FET input op amp with a common-source FET preamplfier.

As is the case of the common-drain preamplifier, Equation (10) applies. If it is assumed that $Z_{IN} >> Z_{OUT}$, $Z_{OUT} = 2R_D$, $g_{os} = 0$, and $A_1 = g_{fs}R_D$, where R_D is the drain resistance and R_S is the source resistance, then one can derive an equation for the total offset referred to the input for an op amp with a common source FET preamp.

$$E_{TIn} \approx E_{os1} + \frac{2\, I_{os}}{g_{fs}} + \frac{E_{os2}}{g_{fs}R_D} \qquad (13)$$

If both sides of equation (13) are divided by ΔT, then

$$\frac{E_{TIn}}{\Delta T} \approx \left(\frac{E_{os1}}{\Delta T}\right) + \frac{2}{g_{fs}}\left(\frac{I_{os}}{\Delta T}\right) + \frac{1}{g_{fs}R_D}\left(\frac{E_{os2}}{\Delta T}\right) \qquad (14)$$

Thus a FET input op amp with a common-source preamplifier has a total drift referred to the input of the drift of the FET pair, plus the current-related voltage drift and the voltage drift of the second stage divided by the gain of the preamplifier. Note that for lowest offset and drift, the gain of the preamplifier should be as large as possible. For high gain, the drain resistors should be as large as possible, consistent with other design criteria (See FET biasing, a later section of this Application Note). When equations (12)-(14) and (11)-(13) are compared, it is apparent that the common-source FET preamplifier always will produce lower overall offset and drift.

Offset Nulling

Methods of nulling offset in the FET input op amp will depend on the configuration of the FET preamplifier in the circuit. Two common methods of nulling offset in common-drain FET preamplifiers are shown in Figure 6A and 6B.

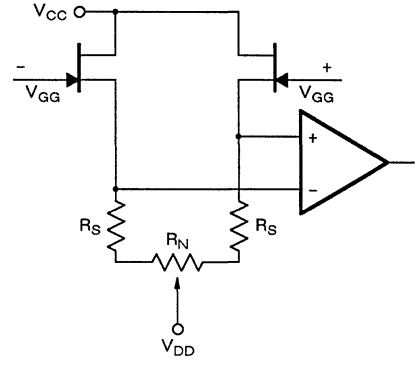

Figure 6A. Nulling a Common-Drain Preamp with Source Resistor Biasing

By changing the drain current in the FET, one can change the gate-to-source voltage and thus change the offset. In a junction FET

$$V_{GS} = V_{GS(off)}\left[1 - \left(\frac{I_D}{I_{DSS}}\right)\right]^{1/2} \quad (15)$$

In a source-follower configuration where $V_{GG} - V_{DD} >> V_{GS(off)}$,

$$I_D \approx \frac{V_{GG} - V_{DD}}{R_S} \quad (16)$$

If Equation (16) is substituted into Equation (15):

$$V_{GS} \approx V_{GS(off)} - \left[\frac{V_{GS(off)}^2 (V_{GG} - V_{DD}) R_S^{-1}}{I_{DSS}}\right]^{1/2} \quad (17)$$

If V_{GS} is differentiated with respect to R_S, one can derive a value of $\Delta V_{GS}/\Delta R_S$ for small changes in R_S:

$$\frac{dV_{GS}}{dR_S} \approx \frac{\Delta V_{GS}}{\Delta R_S} \approx \left[\frac{V_{GS(off)}^2 (V_{GG} - V_{DD})}{4 I_{DSS} R_S^3}\right]^{1/2} \quad (18)$$

Thus in a single-source follower, to correct for an offset E_{Tin}, the value of ΔR_S should be

$$\Delta R \approx \frac{E_{Tin}}{\frac{\Delta V_{GS}}{\Delta R_S}} \quad (19)$$

In the circuit in Figure 6A, where the resistor is a potentiometer in both legs of the differential source follower, the effect of any resistance change is double that of Equation (19). Hence the value of the null potentiometer R_N to correct for an expected maximum offset of E_{Tin} is

$$R_N \approx \frac{E_{Tin}}{\frac{\Delta V_{GS}}{\Delta R_S}} \approx \frac{E_{Tin}}{\left[\frac{V_{GS(off)}^2 (V_{GG} - V_{DD})}{I_{DSS} R_S^3}\right]^{1/2}} \quad (20)$$

For any type of junction FET, there will be a range of $V_{GS(off)}$ and I_{DSS} values. For a conservative value of R_N, minimum values of $V_{GS(off)}$ and I_{DSS} should be used in Equation (20). Also, there will inevitably be small differences in the values of the the two source resistors due to their tolerance; the value of R_N must be increased to correct for these differences.

In the circuit in Figure 6B, the offset is nulled by varying the difference between e_1 and e_2. The value of the fixed resistor, R, is

$$R = \frac{E_{Tin}}{I_{BIAS}} \quad (21)$$

The value of the potentiometer then is 2R. The value of E_{Tin} in Equation (21) is the value found in Equation (11),

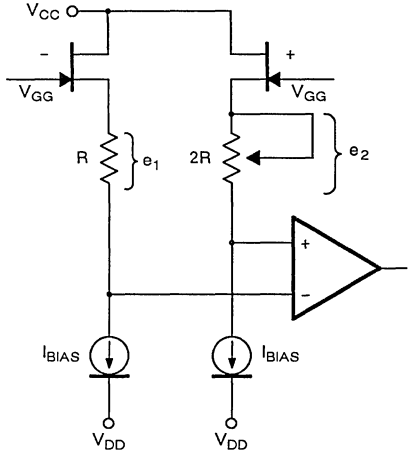

Figure 6B. Nulling a Common-Drain Preamp with Constant Current Biasing

plus any offset caused by unbalance in the current sources. The voltage offset caused by current unbalance in the current sources can be calculated from Equation (15).

In a common-source FET preamplifier, offset can be nulled by either of two techniques. One method is to insert a potentiometer in the source circuit, as is shown in Figure 7A.

In the circuit in Figure 7A, the offset is nulled by the difference in $I_{CM} R_1/2 - I_{CM} R_2/2$. The value of the potentiometer should be

$$R_N \approx \frac{2 E_{Tin}}{I_{cm}} \quad (22)$$

where E_{Tln} is the worst-case value calculated in Equation (13). Before the source nulling method is used, the value of R_N calculated in Equation (22) should be checked against Equations (4) and (6) to confirm that it has no significant effect on gain and output impedance.

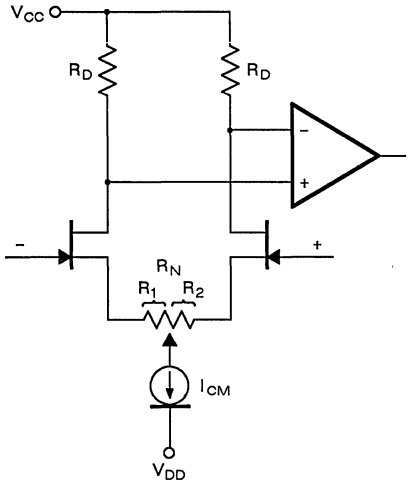

Figure 7A. Source Nulling in Common-Source FET Differential Amplifier

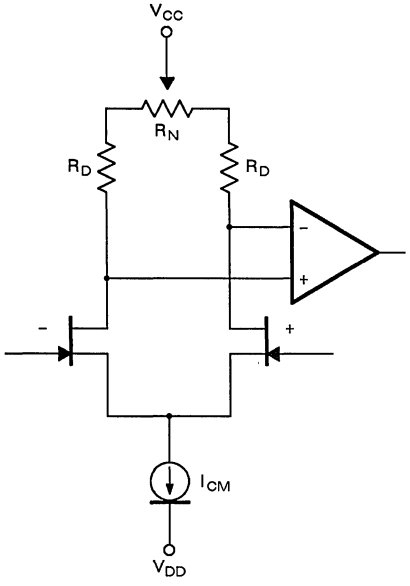

Figure 7B. Drain Nulling in Common-Source FET Differential Amplifier

The second method of accomplishing offset null is a common-source FET differential amplifier is know as drain nulling, and an equivalent circuit is shown in Figure 7B. The basic principle of drain nulling is the same as that employed in source nulling except that the offset which is to be nulled is multiplied by the gain of the stage. Hence, for drain nulling:

$$R_N \approx \frac{2\,E_{Tln}\,\bar{g}_{fs}R_D}{I_{CM}} \qquad (23)$$

Offset nulling is a relatively simple technique which consists of adjusting an offset potentiometer for zero output with zero input. The technique to compensate for drift, however, is more complex and time consuming. The method is based upon the fact that the temperature coefficient of V_{GS} is dependent on drain current. Thus by varying the ratio of the drain current in the two FETs, the drift can be compensated. The technique is of limited practical value, however, because of the lengthy oven testing required. For this reason, drift compensation will not be discussed in depth in this Application Note.

Noise

During design of a FET input operational amplifier, it is useful to be able to predict the total noise of the amplifier referred to the input. The total noise output is then equal to the total noise referred to the input, multiplied by the voltage gain of the amplifier. In a FET amplifier, the total noise can be broken down to three specific sources, for ease of mathematical analysis.

The first noise source is the thermal noise of the generator, which is caused by random electron movement in the generator resistance. Thermal noise is often referred to as "white" noise, since its spectral density is constant for all frequencies. The power spectral density of thermal noise is

$$\bar{S}_t = 4kTR_G \qquad (24)$$

where $\bar{S}_t$ is the power spectral density of the thermal noise in the generator resistance in V^2/Hz, T is the temperature in degrees Kelvin, R_G is the generator resistance, in ohms, and k is Boltzmann's constant to 1.38×10^{-23} Joules/°Kelvin.

The total noise over a bandwidth $f_b - f_a$ is

$$|\bar{e}_t| = \sqrt{|\bar{S}_t|(f_b - f_a)} \qquad (25)$$

where $|\bar{e}_t|$ is the magnitude of the thermal noise stemming from the generator resistance is rms volts, and $f_b - f_a$ is the bandwidth in Hz.

The second significant source of noise is the equivalent short circuit input noise voltage of the FET. This noise voltage, referred to as $\bar{e}_n$, is caused by a number of phenomena within the channel of the FET, and is not constant with frequency; it is made up of two noise components. One of these is white noise, with a spectral density that is constant with frequency. The second is "1 over f" noise, so termed because its power spectral density varies inversely with frequency. 1/f noise usually becomes dominant below a frequency between 100 and 1000 Hz. The power spectral density of $\bar{e}_n$ is the sum of the power spectral densities of the white noise and the 1/f noise components, thus

$$\bar{S}_e = \bar{S}_W + \bar{S}_f \qquad (26)$$

where $\bar{S}_e$ is the total power spectral density of $\bar{e}_n$ in V^2/Hz, $\bar{S}_W$ is the power spectral density of the white noise generated in the FET channel in V^2/Hz, and $\bar{S}_f$ is the power spectral density of the 1/f noise in the FET channel in V^2/Hz.

To find the total rms noise voltage over a given bandwidth, $\bar{S}_e(f)$ must be integrated over the frequency range of interest, and its square root obtained. To accomplish this, it is necessary to define an analytical expression for $\bar{S}_e(f)$. This can be done if two values of $\bar{S}_e(f)$ are known. Usually $\bar{S}_e(f)$ is not given on FET data sheets, however $\bar{e}_n$ is usually given and $\bar{e}_n$ is the square root of $\bar{S}_e(f)$. One value of $\bar{S}_e(f)$ must lie in the 1/f region, and is referred to as $|\bar{S}_{e1}|$ at f_1, and the other (which must lie out of the 1/f region), and is referred to as $|\bar{S}_{e2}|$. A typical graph carrying these values is shown in Figure 8. Note that Figure 8 is a graph of power spectral density, not $\bar{e}_n$.

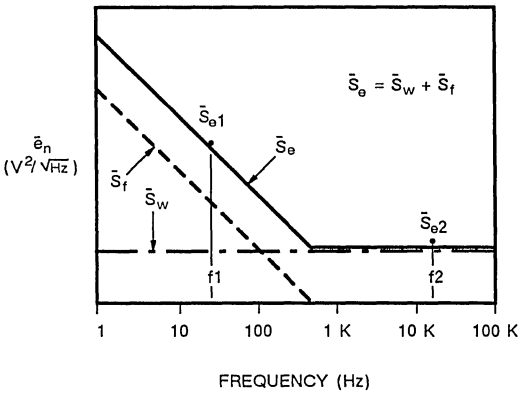

Figure 8. Equivalent Short Circuit Input Noise Power Spectral Density vs. Frequency

Then

$$\bar{S}_e(f) \approx \frac{(|\bar{S}_{e1}| - |\bar{S}_{e2}|)f_1}{f} + |\bar{S}_{e2}| \qquad (27)$$

and

$$|\bar{e}_{nT}| \approx \sqrt{\int_{f_b}^{f_a} \left[\frac{(|\bar{S}_{e1}| - |\bar{S}_{e2}|)f_1}{f} + |\bar{S}_{e2}|\right] df} \qquad (28)$$

where $|e_{nT}|$ is the total rms noise voltage attributable to the short circuit input noise of the FET.

Then,

$$|\bar{e}_{nT}| \approx \sqrt{(|\bar{S}_{e1}| - |\bar{S}_{e2}|)f_1 \ln\left(\frac{f_a}{f_b}\right) + |\bar{S}_{e2}|(f_b - f_a)} \qquad (29)$$

It should be noted that if fa is chosen to be zero Hz in Equation (29), the total noise, $|\bar{e}_{nT}|$, will be infinite. In reality, as the period of the noise becomes greater than several seconds, it begins to resemble drift rather than noise. With this rationale in mind, it is wise to choose a non-zero frequency for f_a, such as 0.1 Hz. Such a frequency selection will provide reasonably accurate data, and will allow comparison between various device types and amplifier circuits.

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The third source of noise is current noise, usually referred to as $\bar{i}_n$. Noise current has a flat spectral density up to the region of 10 to 100 kHz. Beyond this point, the spectral density increases because of noise which feeds through the drain-gate capacitance to the gate. Feed through noise above 100 kHz is known as "shot noise", and will not be dealt with in this Application Note.

The power spectral density of noise current is expressed in the white noise region as

$$|\bar{S}_I| = 2q|I_G| \tag{30}$$

where $|\bar{S}_I|$ is the power spectral density of the current noise in A^2/Hz, q is the charge of an electron, 1.6×10^{-19} coulombs, and I_G is the gate current in amperes. Thus the total input current-caused noise referred to the input of the amplifier is

$$|\bar{e}_{IT}| = R_G\sqrt{|\bar{S}_i|\,(f_b - f_a)} \tag{31}$$

When using Equation (30) it is important to choose a value for I_G which corresponds to the actual operating conditions of the FET. I_G will vary over several decades, depending on temperature, V_{DG} and I_D.

The total input FET noise of a single-ended amplifier is the vector sum of the three components

$$|\bar{e}_T| = \sqrt{\bar{e}_t^2 + \bar{e}_{nT}^2 + \bar{e}_{IT}^2} \tag{32}$$

Since the differential amplifier contains two devices, the noise from both FETs must be accounted for:

$$|\bar{e}_{Tdiff}| = \sqrt{2}\,|\bar{e}_T| \tag{33}$$

The foregoing analysis covers only the noise in the FET pre-amplifier. It does not include the noise contribution of the second stage. As in the case of offset and drift, the noise contribution of the second stage can be referred back to the input of the op amp. For a common-drain preamplifier, the total noise referred to the input of the op amp is

$$|\bar{e}_{Tt}| \approx \sqrt{|\bar{e}_{Tdiff}|^2 + \left(\frac{2|\bar{i}_n|}{g_{fs}}\right)^2 + |\bar{e}_{n2}|^2} \tag{34}$$

where $|\bar{e}_{Tt}|$ is the magnitude of the total op amp noise from all sources referred to the input in rms volts, $|\bar{i}_{n2}|$ is the magnitude of the input noise current of the second stage in rms amperes, and $|\bar{e}_{n2}|$ is the magnitude of the input voltage noise of the second stage in rms volts.

Since the spectral densities of $\bar{i}_{n2}$ and $\bar{e}_{n2}$ are functions of frequency, the $|\bar{I}_{n2}|$ and $|\bar{e}_{n2}|$ must be determined in a manner similar to that of Equation (29). That is

$$|\bar{e}_{n2}| \approx \sqrt{(|\bar{S}_{e1}| - |\bar{S}_{e2}|)f_1 \ln\left(\frac{f_a}{f_b}\right) + |\bar{S}_{e2}|\,(f_b - f_a)} \tag{35}$$

where $|\bar{S}_{e1}|$, $|\bar{S}_{e2}|$, f_1, f_a and f_b are as previously defined, except that they now refer to the noise voltage of the second stage. Also,

$$|\bar{i}_{n2}| \approx \sqrt{(|\bar{S}_{i1}| - |\bar{S}_{i2}|)f_1 \ln\left(\frac{f_a}{f_b}\right) + |\bar{S}_{e2}|\,(f_b - f_a)} \tag{36}$$

where $|\bar{S}_{i1}|$ is a point on the curve of input current power spectral density vs frequency in the 1/f region, and $|\bar{S}_{i2}|$ is a point totally out of the 1/f region.

In the case of a FET input op amp with a common-source FET preamplifier, the total op amp noise referred to the input is

$$|\bar{e}_{Tt}| \approx \sqrt{|\bar{e}_{Tdiff}|^2 + \left(\frac{2|\bar{i}_{n2}|}{g_{fs}}\right)^2 + \left(\frac{2|\bar{e}_{n2}|}{g_{fs}R_D}\right)^2} \tag{37}$$

As was the case for offset and drift, the common source FET preamplifier will always product lower equivalent input noise for the total op amp than will the FET common-drain preamplifier.

In any discussion of noise the term "noise figure" is bound to arise. Noise figure is the ratio of added noise power to the thermal noise power of the generator resistance. In a FET preamplifier

$$NF = 10\log_{10}\left[1 + \frac{\bar{e}_n^2 + \bar{i}_n^2 R_G^2}{(f_a - f_b)\,4kTR_G}\right] \tag{38}$$

For any device there is one value of generator impedance for which the noise figure is optimum

$$R_{opt} = \frac{|\bar{e}_n|}{|\bar{i}_n|} \qquad (39)$$

Noise figure is a useful concept in RF circuits where, by various matching techniques, the generator resistance can be adjusted for R_{opt} so that the required noise figure is achieved. Most FET input op amps, however, are used in dc-coupled applications, and there is seldom any choice for the designer concerning generator resistance. For this reason, noise figure is not a very useful concept in FET input op amps. A much more useful figure of merit is simply $\sqrt{|\bar{e}_n^2| + |\bar{i}_n^2| R_G^2}$, which is added noise voltage referred to the input of the device.

Input and Offset Current

The gate of a JFET forms a reverse-biased junction with the channel. For this reason, the input current of a junction FET is the leakage current through the reverse-biased gate-to-source and gate to drain junctions. In normal operation the drain-to-gate voltage is much higher than the source-to-gate voltage; thus it is the drain-to-gate junction which is responsible for most of the leakage current.

N-Channel junction FETs experience an I_G "breakpoint" where the gate current rises rapidly with increasing drain-to-gate voltage. This is shown in the plot of gate current vs drain-to-gate voltage in Figure (9).

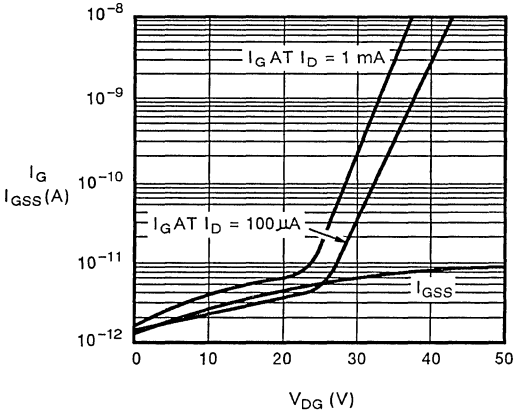

Figure 9. Gate Current vs. Drain-to-Gate Voltage

The I_G breakpoint results from carriers in the channel being accelerated by the applied field to such a degree that they are capable of generating hole-electron pairs upon collision with a silicon atom. This phenomenon is similar to normal junction breakdown, but occurs at a lower voltage than BV_{GSS}. This is because, under operating conditions, there are more carriers available in the channel for collisions. Operation at higher drain current will result in lower I_G breakpoints for the same reasons.

At low drain-to-gate voltages the leakage current doubles for approximately every 10°C increase in temperature. However, I_G breakpoints occur at a higher voltage for increasing temperature. This is consistent with normal breakdown voltage behavior for diodes above 6 V, where the avalanche effect dominates.

Figure 10 shows that for some voltages, I_G at 125°C is actually lower than I_G at room temperature!

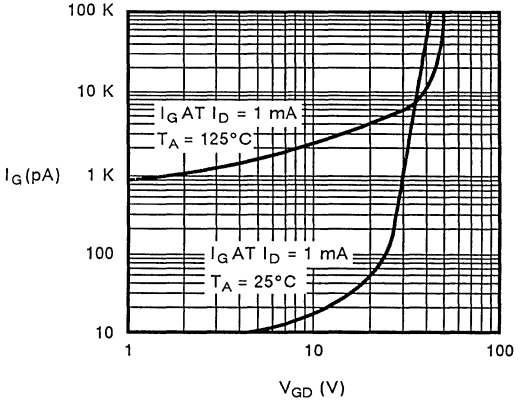

Figure 10. Gate Current vs Drain-to-Gate Voltage at 25°C and 125°C.

In a dual FET, the difference between the I_G of each device is known as I_G offset. A good rule of thumb for design analysis is

$$I_G \text{ offset} \approx 0.1\, I_G \qquad (40)$$

Common Mode Errors

Common mode errors are output errors caused by common-mode input signals. A common-mode input signal is any signal which equally affect both sides of a differential amplifier. Common-mode inputs often take the form of either 60 Hz signal pickup or dc bias signals. It is interesting to note that ambient temperature is also a common-mode signal since it affects both devices equally.

Common-mode input signals cause two types of output errors in differential amplifiers. One type of error is a differential output signal caused by the common-mode input; the other is a common-mode output signal where both outputs change equally and in the same direction. Since the op amp which follows the FET input stage will typically amplify the differential mode error 80 dB more than the common-mode error(assuming its CMRR is 80 dB), the differential mode error is by far the more important of the two.

Differential mode error is the result of unequal gain between the two sides of the differential amplifier. This can be caused by imprecise transconductance matching of the dual FETs, unbalanced drain resistances, unbalanced source resistances, imprecise output conductance matching of the FETs, or any combination of these factors. Thus, if the drain or source resistances are adjusted for drift or offset nulling, the differential output error will be increased and CMRR degraded.

Consider the case where the differential amplifier has slightly unbalanced gain. An equivalent circuit is shown in Figure 11.

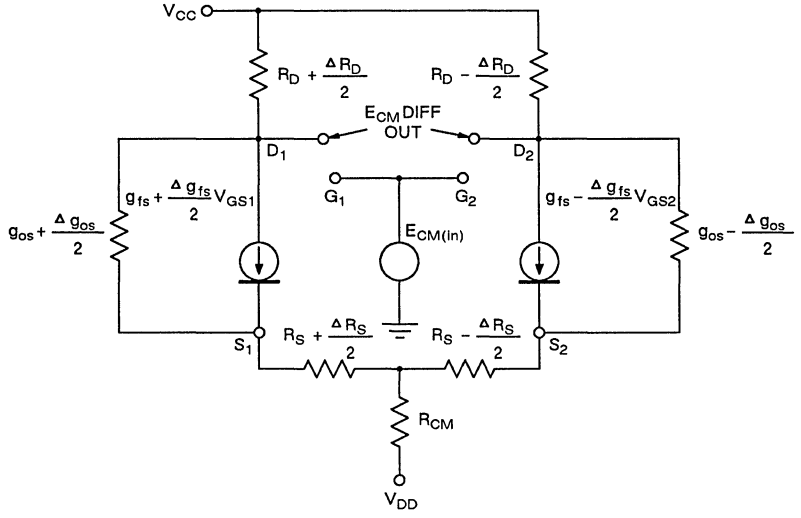

Figure 11. Differential Output Equivalent Circuit

A Figure of Merit CMRR can be derived for differential out errors:

$$CMRR_{(diff)} = \frac{A_{diff}}{A_{CM(diff)}} \quad (41)$$

The differential mode gain, assuming both halves of the differential amplifier are nearly equal, can be approximated as:

$$A_{diff} \approx \frac{g_{fs}R_D}{1 + g_{fs}R_S}\left(\frac{1}{1 + g_{os}R_D}\right) \quad (42)$$

$$\text{for } \frac{1}{g_{os}} >> R_S$$

For $R_S >> 1/g_{fs}$ and $R_D << 1/g_{os}$, this simplifies to the familiar expression:

$$A_{diff} \approx g_{fs}R_D \quad (43)$$

If the circuit is balanced except for the drain resistors, the differential mode error resulting from a common-mode input signal becomes:

$$A_{CM(diff)} \approx \frac{R_D}{2R_{CM}} \quad (44)$$

so

$$CMRR_{(db)} = 20 \log\left[\frac{2R_{CM}}{R_D} g_{fs}R_D\right] \quad (45)$$

Similarly, the error introduced by unbalanced transconductance is taken into account:

$$CMRR_{(db)} = 20 \log 2\Delta g_{fs} R_{CM} \quad (46)$$

When unequal output conductances are taken into account:

$$CMRR_{(db)} = 20 \log \frac{2g_{fs} R_{CM} R_o}{\Delta R_o} \quad (47)$$

and with unbalanced source resistors,

$$CMRR_{(db)} = 20 \log \frac{2R_{CM}}{\Delta R_S} \quad (48)$$

assuming $1/g_{fs} >> R_S$.

A more general equation, resulting from the combination of all the above factors, is:

$$CMRR_{(db)} = 20 \log\left[\frac{2g_{fs} R_{CM}}{\frac{\Delta R_S + 1/\Delta g_{fs}}{R_S + 1/g_{fs}} \pm \frac{\Delta R_D}{R_D} \pm \frac{\Delta R_o}{R_o}}\right] \quad (49)$$

The other type of error, common-mode output voltage, is important when only one of the outputs of the differential stage is used, or when the following stage has a poor CMRR. Figure 12 shows how common-mode output error can be measured. If common-mode gain for common-mode output errors is defined as

$$A_{CM(cm)} = \frac{V_{D1}}{V_{G1}} = \frac{V_{D2}}{V_{G2}} \quad (50)$$

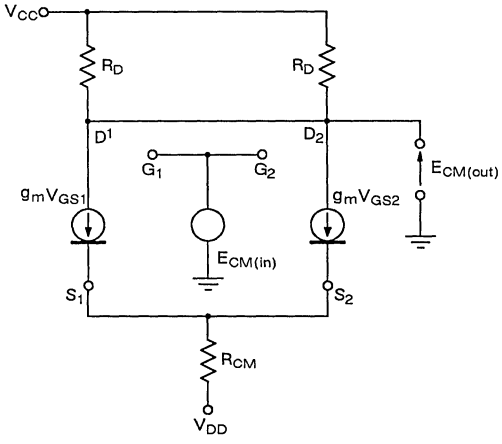

Figure 12. Common-Mode Output Equivalent Circuit

then an expression may be found by noting that

$$V_D = -g_{fs}V_{GS}R_D \quad (51)$$

However,

$$V_{GS} = V_G - V_S \quad (52)$$

and

$$V_S = \frac{-2\ V_D R_{CM}}{R_D} \quad (53)$$

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Thus,

$$V_D = -g_{fs} V_G R_D - g_{fs} 2 R_{CM} V_D \quad (54)$$

and

$$A_{CM(cm)} = \frac{V_D}{V_G} = \frac{-g_{fs} R_D}{1 + 2 g_{fs} R_{CM}} \quad (55)$$

It is common practice to assign a Figure of Merit to a differential amplifier. This Figure of Merit is "common mode rejection ratio," usually abbreviated as CMRR. CMRR is defined as

$$CMRR = \frac{A_{diff}}{A_{CM}} \quad (56)$$

When equations (5) and (55) are substituted into equation (56), it is apparent that the common-mode rejection ratio for common-mode output errors is

$$CMRR_{(cm)} \approx \frac{-g_{fs} R_D}{\frac{-g_{fs} R_D}{1 + 2 g_{fs} R_{CM}}} = 1 + 2 g_{fs} R_{CM} \quad (57)$$

Most op amps have single-ended outputs. In such cases, there can be only one result of a common-mode input signal; and error in the output. In a FET input op amp the total CMRR will be a function of the common-mode and differential output errors of the preamplifier as well as the CMRR of the second stage. To calculate the combined CMRR of both stages of the FET input op amp, refer to Equation (56), which is the definition of CMRR.

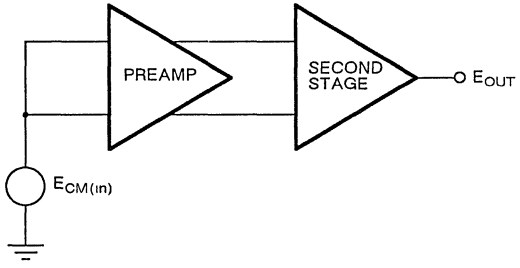


Figure 13. Two-Stage Op Amp CMRR Model

A two-stage amplifier is shown in Figure 13. Calculations of CMRR in this circuit is made as follows:

$$CMRR = \frac{A_{diff}}{A_{CM}} = \frac{[A_{diff1}][A_{diff2}]}{[A_{CM(cm)1}][A_{CM2}] + [A_{CM(diff)1}][A_{diff2}]} \quad (58)$$

Substituting Equation (56) into Equation (58) we have,

$$CMRR_{total} = \frac{1}{\frac{1}{[CMRR_{(cm)1}][CMRR_2]} + \frac{1}{[CMRR_{(diff)1}]}} \quad (59)$$

where $CMRR_{(cm)1}$ is the CMRR referred to in Equation (57) for the FET preamplifier, $CMRR_2$ is the CMRR specification of the second stage, and $CMRR_{(diff)1}$ is the CMRR referred to in Equation (49) for the FET preamplifier.

In a common drain stage, the common-mode gain with respect to common-mode output error $[A_{CM(cm)}]$ is unity (when $A_{diff} = 1$). Hence, the entire output common-mode signal is passed along to the second stage. All of the equations in this section, except for (50)-(55) and (57) apply equally to common drain preamplifiers.

Frequency Response

The frequency response of a FET differential amplifier is determined by two time constants, one for the input and one for the output.

The input time constant is formed by the generator impedance and the effective input capacitance, C_{in}, where

$$C_{in} = \left(\frac{g_{fs} R_D}{1 + g_{fs} R_S}\right) C_{DG} + \left(1 - \frac{g_{fs} R_S}{1 + g_{fs} R_S}\right) C_{GS} + C_{stray} \quad (60)$$

and

$$f_{in} = \frac{1}{2\pi C_{in} R_G} \quad (61)$$

The output time constant is formed by the drain resistance and the output capacitance, C_{out}, where

$$f_{out} = \frac{1}{2\pi C_{out} R_D} \quad (62)$$

and

$$C_{out} = C_{gd} + C_{load} + C_{stray} \quad (63)$$

Equations (60) and (61) apply to common drain preamplifiers as well as to common source preamplifiers, if $R_D = 0$.

For the case of the output time constant for the common drain preamplifier.

$$f_{out} = \frac{g_{fs}}{2\pi C_{out}} \quad (64)$$

$$C_{out} = C_{gs} + C_{sd} + C_{load} + C_{stray} \quad (65)$$

Typically, the Bode plot of a FET preamplifier will resemble that shown in figure 14.

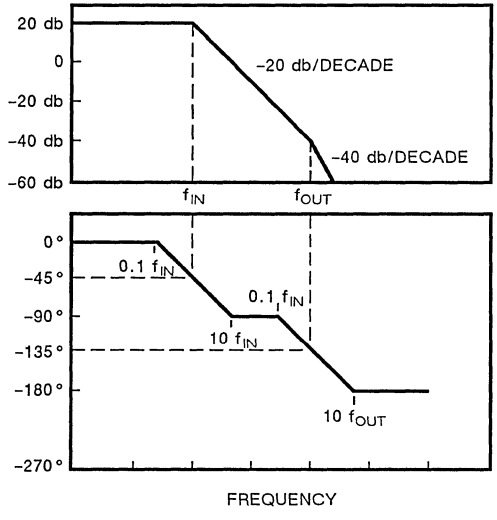


Figure 14. Phase and Gain Bode Plots for Typical FET Preamplifier

Stability and Phase Compensation

The stability criterion for any closed loop system, including an operation amplifier, is that the phase shift around the loop must never reach 360° for any frequency at which the gain is unity or greater. Since the feedback around an op amp is in the inverting input there is an intrinsic 180° phase shift. This dictates that the additional phase shift in the amplifier plus the phase shifty of the feedback network must be less than 180° for all frequencies where gain is unity or greater.

Most commercially-available operational amplifiers are compensated so that they have only 90° of phase shift where gain is unity or greater. This is demonstrated in Figure 15. When a FET preamplifier is added ahead of an op amp, the total gain and phase response will be the sum of the response of the preamplifier and the second stage. Often, this results in a phase shift of 180° or greater over much of the frequency range. An intolerable situation is thus created in that the total FET input op amp will oscillate if the gain is set to a value where the phase shift is greater than 180° .

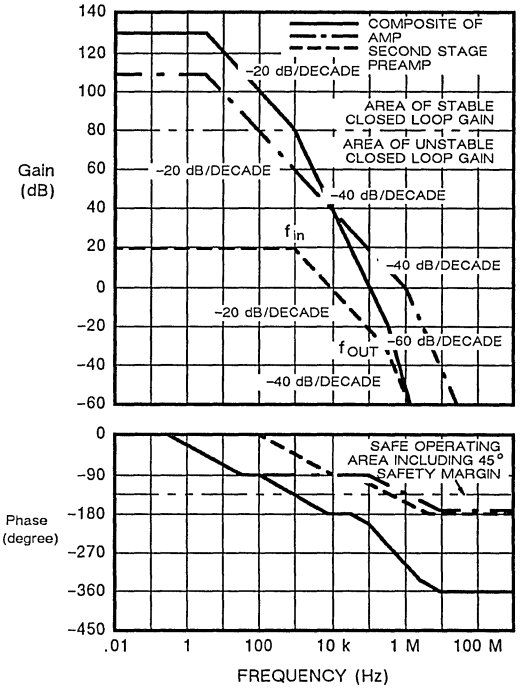


Figure 15. Compensated Phase Shift in Op Amps

As a rule of thumb, an op amp will not oscillate if the closed loop gain is such that the slope of the roll-off is no greater than 20 dB/decade. This point corresponds to a worst-case phase shift of 135° .

There are a number of techniques for stabilizing the amplifier; this Application Note will not attempt to treat them.

Selecting the Proper FET Pair

FeT differential pairs can be broken down into four general types, according to their intended application. These types include low leakage, low noise, high frequency and general purpose FET duals.

Low-leakage FETs generally have leakage currents in the range of 0.1 to 1.0 pA at 25°C. To achieve this low leakage, the active area of the device is made as small as possible. This small active area produces low g_{fs} and low capacitance. Although low leakage FETs are preferred whenever low circuit leakage is is the primary design criterion, the designer should consider using a general-purpose FET if slightly higher leakage can be tolerated. General purpose devices offer better g_{fs}, offset, drift and $\bar{e}_n$ than do low-leakage devices. One feature of the low-leakage FET which is not often specified in data sheets, but which is important to actual circuit performance, is the I_G breakpoint; that is, the drain-to-gate voltage at which the gate current rises rapidly. In practical circuits, the drain-to-gate voltage can reach 15 or 20 volts causing excessive leakage for FETs with low I_G breakpoints.

Low-noise FETs are designed primarily for low $\bar{e}_n$. They also have moderate g_{fs}, low g_{os}, and moderate leakage and breakdown voltage. Low-noise devices tend to have better drift and CMRR characteristics than do other types of dual FETs. A low-noise FET can product the lowest noise operation of any FET when the generator impedance is below 1 to 10 MΩ. For higher generator impedances, low-leakage FETs may well provide lower overall noise performance because of their lower noise current.

High frequency dual FETs have very high g_{fs} and low capacitance. To achieve these characteristic leakage currents, breakdown voltage and the I_G breakpoint must be sacrificed. Because of these performance tradeoffs, high-frequency FETs should be used only when their high-gain bandwidth is a design requirement. High-frequency FETs are usually of hybrid (two chip) construction rather than of a monolithic design, because of the significantly lower capacitances between the two chips.

General-purpose dual devices are often the best choice for FET input op amp applications, exhibiting good g_{fs} and breakdown voltage and moderately low g_{os}, leakage current, and capacitance. General-purpose dual FETs also tend to have low $\bar{e}_n$ and good CMRR and drift characteristics.

Representative geometries of the four types of FETs described preceding are shown in Figure 16, and provide a good insight into the relationship of device active area and performance characteristics.

When selecting any dual FET, two factors which affect the overall performance of the devices should be considered. One is the maximum value of $V_{GS(off)}$; a low maximum value of $V_{GS(off)}$ simplifies bias design and improves common-mode range, CMRR, offset and drift. The other factor is the offset of the device. Although any value of offset can be nulled out of a circuit, the nulling process itself degrades CMRR and the drift performance of the circuit.

Selecting the Op Amp Integrated Circuit

The monolithic IC op amp portion of a FET input op amp circuit either contributes to or solely determines five parameters of the complete circuit. For three of the parameters – offset, drift and noise – the contributions are diminished in the complete op amp circuit by the gain of the FET differential amplifier. In many circuits, however, these parameters are still significant and should not be ignored. Whenever possible, an IC op amp device should be chosen which specifies maximum values for V_{OS}, I_{OS}, V_{drift}, e_n and i_n. Many IC op amp data sheets will provide only typical values for these parameters. Typical values can be in error by an order of magnitude, and almost inevitably vary from lot to lot.

One parameter which is usually ignored on IC op amp data sheets is so-called "popcorn noise". Even though this parameter is missing from the data sheet it is usually present in the op amp IC and can be quite troublesome in low noise designs. If low noise is a prime design criterion an op amp specified for low "popcorn noise" should be selected.

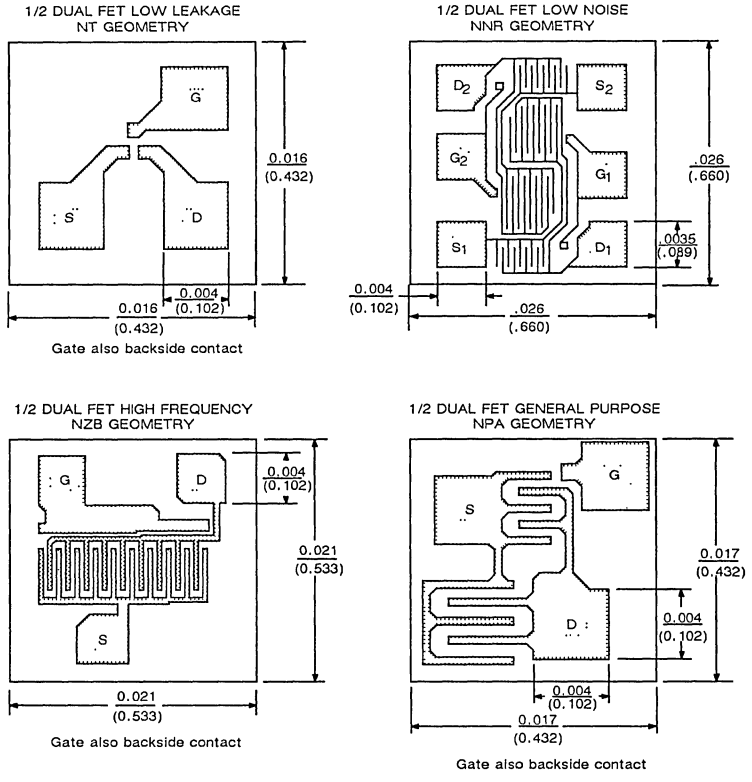


Figure 16. Four FET Geometries

All dimensions in inches
(All dimensions in millimeters)

Two other circuit parameters, output impedance and slew rate, are determined entirely by the IC op amp portion of the circuit.

Biasing the FET preamplifier

After the proper FET has been selected and the op amp IC chosen for the second stage, the next consideration is the bias design of the FET preamplifier. The first objective in biasing a FET preamplifier is the determination of the correct FET operating current. Usually, this will be the manufacturer-recommended operating current of the FET, which can range from 30 μA for the low-leakage devices to 200 μA for general purpose or low-noise devices. If some other value of operating current is desired, two limiting factors exist and should be kept in mind.

The upper limit is the minimum value of I_{DSS} for the type of FET selected, that is

$$I_D \text{ operating} \leq I_{DSS(min)} \quad (66)$$

If a value of operating current greater than minimum I_{DSS} is selected, the FETs will operate with forward-biased gate-source junctions, and thus negate the low I_G characteristics of the circuit.

The lower limit for I_D is determined by the fact that g_{fs} is related to I_D through the following equation

$$g_{fs} \approx g_{fso}\sqrt{\frac{I_D}{I_{DSS}}} \quad (67)$$

where g_{fs} is the forward transconductance at V_{GS} = 0 and I_{DSS}, I_D is the operating current, I_D is the operating current, and I_{DSS} is the drain current with V_{GS} = 0.

For very small values of drain current, the transconductance and thus the gain become very small.

The next step in bias design is selection of the current source. The simplest means of establishing a current source is via a resistor. This method, however, has an inherent drawback in that the current will change as the common-mode voltage changes on the gates; offset, drift and CMRR are unfavorably affected.

A better approach to selection of a current source is to use an active device, such as a juction FET current limiter diode. These devices have very low g_{os} and temperature coefficient; recommended types are the CR100 series of diodes.

In the case of the common-drain preamplifier, selection the the current sources completes the bias design. For the common-source preamplifier, however, the value of the drain resistor remains to be established. The value of these resistors affects offset, drift, noise, open-loop gain, current leakage, common-mode range, and bandwidth in the circuit. With the exception of the last two, these parameters will be improved if the resistors are as large as possible; the factor which ultimately limits resistor size is the voltage drop across them. Figure (17) shows a typical circuit employing this form of biasing.

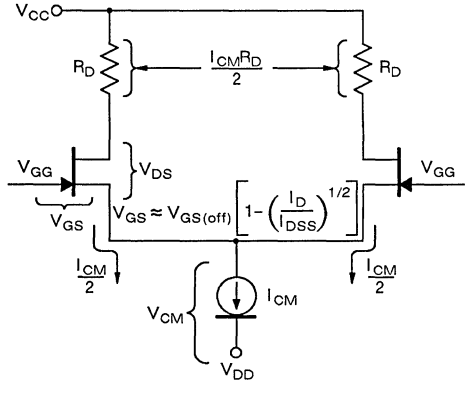


Figure 17. Op Amp Circuit Biasing

Since the voltage drop across the drain resistors is I_{CM} $R_D/2$, the voltage on the drains of the FETs is V_{DQ} where

$$V_{DQ} = V_{CC} - \frac{I_{CM}R_D}{2} \quad (68)$$

It is important to insure that the voltage drop across the FET drain to the FET source is always greater than $V_{GS(off)}$. This is necessary for the FET to operate in the "pentode" or saturation region, where the drain current is relatively independent of the drain-to-source voltage. In this condition, the device g_{os} will be low, and in turn will assure good offset and CMRR.

The maximum common mode bias voltage which can be applied to the gates without operating the FETs in the triode region is

$$V_{GG(max)} = V_{CC} - \frac{I_{CM}R_D}{2} + V_{GS(off)max} + V_{GS(on)max} \quad (69)$$

Where $V_{GS(off)}$ and $V_{GS(on)}$ are negative voltages

and

$$V_{GS(on)max} \approx V_{GS(off)max}\left[1 - \left(\frac{I_D}{I_{DSS(max)}}\right)^{1/2}\right] \quad (70)$$

However in most cases $V_{GS(on)max}$ is approximately $V_{GS(off)max}$ so

$$V_{GG(max)} \approx V_{CC} - \frac{I_{CM}R_D}{2} + V_{GS(off)max} \quad (71)$$

The minimum common mode voltage which can be applied to the gate is

$$V_{GG(min)} = V_{DD} + V_{CM(max)} + V_{GS(min)} \quad (72)$$

when V_{DD} and $V_{GS(min)}$ are negatives voltages and

$$V_{GS(min)} = V_{GS(off)min}\left[1 - \left(\frac{I_D}{I_{DSS(max)}}\right)^{1/2}\right] \quad (73)$$

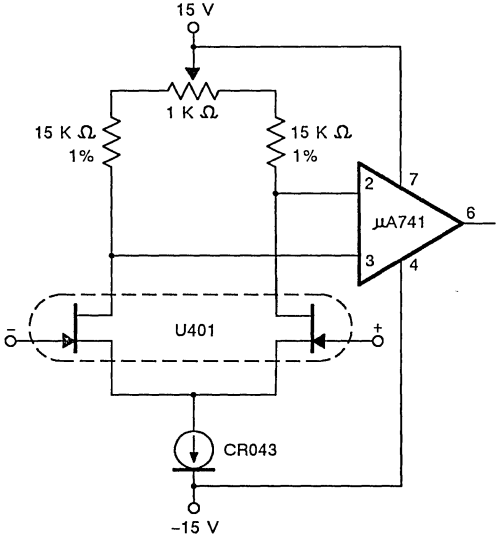
But in most cases $V_{GS(min)} \approx 0$ so

$$V_{GG(min)} \approx V_{DD} + V_{CM(max)} \quad (74)$$

Drain resistors should be of good quality, such as metal film, and should be mounted in close physical proximity to minimize temperature differentials. Temperature-induced resistance differentials of only hundredths of a percent can cause offsets of many millivolts.

APPENDIX A – DESIGN EXAMPLE

This Appendix deals with a typical FET input op amp design example, using a Slliconix U401 N-Channel junction FET. The U401 is designed to be operated with an I_D of 200 μA per device, or with an I_{CM} of 400 μA. A general-purpose operational amplifier should have a large common-mode range and good CMRR. These two requirements dictate that an active current source be used, such as the Siliconix CR043 current regulator diode. The CR043 is ideal for this purpose, with a nominal current value of 430 μA ±10% and a low temperature coefficient of less than 0.05%/°C typically, or 0.2 μA/°C.



General Purpose Design Example Circuit

Selection of drain resistor value involves a trade-off between preamplifier gain and common-mode range. Common-mode range decreases and gain increases proportionally to increased value of the drain resistor. If a voltage drop of 3 V across the drain resistors is permissible, then the value of the drain resistors can be found by applying Ohm's Law, as in

$$R_D = \frac{3\ V}{200\ \mu A} = 15\ k\Omega \qquad (1)$$

Gain of the preamplifier will be as established in

$$A_{diff} \approx - g_{fs} R_D \qquad (2)$$

From the U401 data sheet, g_{fs} at 200 μA operating current varies from a minimum of 1000 μ℧ to a maximum of 1600 μ℧. For a worst-case design, the minimum value should be used:

$$A_{diff(min)} \approx (1 \times 10^{-3}) \bullet (1.5 \times 10^{4}) = 15.0 \qquad (3)$$

The maximum positive common-mode excursion can be calculated if the voltage drop across the drain resistors is subtracted and the device $V_{GS(off)}$ and the device $V_{GS(on)}$ are added to the positive power supply voltage

$$V_{GG(max)} = V_{CC} - \frac{I_{CM} R_D}{2} + V_{GS(off)max} + V_{GS(on)max} \qquad (4)$$

I_{CM} can be up to 430 μA + 10% = 473 μA. $V_{GS(off)}$ max from the data sheet is given as 2.5V, and $V_{GS(on)}$ may be obtained from Equation (64), preceding

$$V_{GS(on)max} \approx V_{GS(off)max} \left[1 - \left(\frac{I_D}{I_{DSS(max)}} \right)^{1/2} \right] \qquad (5)$$

Maximum values of $V_{GS(off)}$ and I_{DSS} will provide the maximum value of $V_{GS(on)}$

$$V_{GS(on)max} \approx -2.5 \left[1 - \left(\frac{0.2}{10.0} \right)^{1/2} \right] \approx -2.2\ V \qquad (6)$$

if ±15 V supplied are used.

$$V_{GG(max)} = 15 - 3.6 - 2.5 - 2.2 = +6.7\ V \qquad (7)$$

9

and

$$V_{GG(min)} = V_{DD} + V_{CM(max)} + V_{GS(min)} \quad (8)$$

where V_{DD} and V_{GS} are negative numbers.

The CR043 data sheet indicates that a minimum knee impedance of 0.75 mΩ occurs at V_{CM} = 6V. Thus

$$V_{GG(min)} = -15 + 6 + V_{GS(min)} \quad (9)$$

but

$$V_{GS(min)} \approx V_{GS(off)min}\left[1 - \left(\frac{I_D}{I_{DSS(min)}}\right)^{1/2}\right] \quad (10)$$

or

$$V_{GS(min)} \approx -(0.5)\left[1 - (0.4)^{1/2}\right]$$

$$= -(0.5) \bullet (1 - 0.6)$$

$$= -(0.5) \bullet (0.4) = -0.20 \quad (11)$$

then

$$V_{GG(min)} = -15 + 6.0 - 0.2 = -8.8\ V \quad (12)$$

If the U401 FET is used a μA741 bipolar op amp, the offset will be as established in Equation (13), preceding:

$$E_{TIn} \approx E_{os1} + \frac{2\,I_{os}}{g_{fs}} + \frac{E_{os2}}{g_{fs}R_D} \quad (13)$$

From the U401 data sheet, E_{os1} = 5 mV, and $g_{fs(min)}$ at I_D = 200 μA is 1000 μ℧. From the op amp data sheet, $I_{SO(max)}$ is given as 200 nA. Therefore

$$E_{TIn(max)} = 5 \times 10^{-3} + \frac{2\,(2 \times 10^{-7})}{1 \times 10^{-3}} + \frac{5 \times 10^{-3}}{15.0} \approx 5.73\ mV \quad (14)$$

In Equation (14) preceding, drift was established as

$$\frac{E_{TIn}}{\Delta T} \approx \frac{E_{os1}}{\Delta T} + \frac{2}{g_{fs}}\left(\frac{I_{os}}{\Delta T}\right) + \frac{1}{g_{fs}R_D}\left(\frac{E_{os2}}{\Delta T}\right) \quad (15)$$

$$\frac{E_{TIn}}{\Delta T} \approx 10 \times 10^{-6} + \frac{2(6 \times 10^{-10})}{9 \times 10^{-4}} + \frac{1 \times 10^{-5}}{15.0} \quad (16)$$

or

$$\frac{E_{TIn}}{\Delta T} \approx 12\ \mu V/°C \text{ worst case} \quad (17)$$

Equation (17) assumes that the drain resistors are perfectly balanced.

For drain nulling, the value of the null potentiometer should be

$$R_N = \frac{2\,E_{TIn(max)}\,g_{fs(max)}R_D}{I_{CM(min)}} \quad (18)$$

or

$$R_N = \frac{2(5.8 \times 10^{-3})(1.6 \times 10^{-3})(1.5 \times 10^{4})}{3.87 \times 10^{-4}} \quad (19)$$

or

$$R_N = 720\ \Omega$$

However, to this approximation for R_N must be added the maximum drain resistor unbalance, which is 2% R_D for 1% tolerance resistors or 300 Ω. Thus $R_N \approx 1\ k\Omega$.

Equation (29) established total rms noise voltage attributable to the short circuit input noise voltage of the FET as

$$|\bar{e}_{nT}| \approx \sqrt{(|\bar{S}_{e1}| - |\bar{S}_{e2}|) f_1 \ln\left(\frac{f_a}{f_b}\right) + |\bar{S}_{e2}| (f_b - f_a)} \quad (20)$$

From typical values given in the U401 data sheet, $\bar{S}_{e1} = 36 \times 10^{-18}$ V^2/Hz; $\bar{S}_{e2} = 6.25 \times 10^{-18}$; $f_1 = 10$ Hz; $f_2 = 10$ kHz; and if $f_a = 1$ Hz and $f_b = 1$ kHz, then,

$$|\bar{e}_{nT}| \approx \sqrt{(3 \times 10^{-17}) 10 (6.9) + (6.25 \times 10^{-18}) (1 \times 10^3)} \quad (21)$$

or

$$|\bar{e}_{nT}| \approx \sqrt{2.07 \times 10^{-15} + 6.25 \times 10^{-15}} \quad (22)$$

and

$$|\bar{e}_{nT}| \approx \sqrt{83.2 \times 10^{-16}} = 9.1 \times 10^{-8} = 91 \text{ nV rms.} \quad (23)$$

In Equation (36), $\bar{i}_n$ was established as

$$|\bar{i}_n| \approx \sqrt{(|\bar{S}_{I1}| - |\bar{S}_{I2}|) f_1 \ln\left(\frac{f_b}{f_a}\right) + |\bar{S}_{I2}| (f_b - f_a)}; \quad (24)$$

and from the op amp data sheet, values are given so that $\bar{S}_{I1} = 5 \times 10^{-23}$, $\bar{S}_{I2} = 3 \times 10^{-25}$, $f_1 = 10$ Hz and $f_2 = 10$ kHz. Therefore,

$$|\bar{i}_n| \approx \sqrt{5 \times 10^{-23} (10) (6.9) + (3 \times 10^{-25}) (1 \times 10^3)} \quad (25)$$

or

$$|\bar{i}_n| = 6.2 \times 10^{-11} \text{ amps rms} = 62 \text{ femtoamps rms.} \quad (26)$$

Equation (35) preceding established that

$$|\bar{e}_{n2}| \approx \sqrt{(|\bar{S}_{e1}| - |\bar{S}_{e2}|) f_1 \ln\left(\frac{f_b}{f_a}\right) + |\bar{S}_{e2}| (f_b - f_a)}; \quad (27)$$

from the data sheet, $\bar{S}_{e1} = 5 \times 10^{-15}$ V^2/Hz, $\bar{S}_{e2} = 4 \times 10^{-16}$ V^2/Hz, $f_1 = 10$ Hz and $f_2 = 10$ kHz. Therefore,

$$|\bar{e}_{n2}| \approx \sqrt{(4.6 \times 10^{-15}) 10 \ln(1000) + 4 \times 10^{-16} (1 \times 10^3)} \quad (28)$$

or

$$|\bar{e}_{n2}| \approx 8.47 \times 10^{-7} \text{ V rms} = 847 \text{ nV rms.} \quad (29)$$

In Equation (33) preceding it was established that

$$|\bar{e}_{Tdiff}| = \sqrt{2}\, |\bar{e}_T| = 1.4 \text{ (91 nV)} = 129 \text{ nV} \quad (30)$$

and from Equation (37) preceding, $\bar{e}_{Tt}$ was defined as

$$|\bar{e}_{Tt}| \approx \sqrt{|\bar{e}_{Tdiff}|^2 + \left(\frac{2|\bar{i}_n|}{g_{fs}}\right)^2 + \left(\frac{|\bar{e}_{n2}|}{g_{fs} R_D}\right)^2} \quad (31)$$

or

$$|\bar{e}_{Tt}| \approx \left\{(1.29 \times 10^{-7})^2 + \left[\frac{2 (6.2 \times 10^{-11})}{(1 \times 10^{-3})}\right]^2 + \left(\frac{8.47 \times 10^{-7}}{1.5 \times 10^{1}}\right)^2\right\}^{1/2} \quad (32)$$

or

$$|\bar{e}_{Tt}| \approx \left[(1.66 \times 10^{-14}) + (1.5 \times 10^{-14}) + .32 \times 10^{-14})\right]$$

$$\approx 1.88 \times 10^{-7} \approx 188 \text{ nV rms} \quad (33)$$

9

Frequency Response

As defined in Equation (57) preceding, the output frequency of the preamplifier will be

$$f_{out} = \frac{1}{2\pi C_{out} R_D} \quad (34)$$

where

$$C_{out} = C_{gd} + C_{load} + C_{stray} \quad (35)$$

or

$$C_{out} \approx 5\ pF + 2\ pF + 5\ pF \approx 12\ pF \quad (36)$$

and thus

$$f_{out} = \frac{1}{(6.28)\ (1.5 \times 10^{4})\ (1.2 \times 10^{-11})} = 880\ kHz \quad (37)$$

The combined Bode plot of the preamplifier and the second stage is shown in Figure 18.

The Bode plot indicates that the op amp will be stable for any closed-loop gain of greater than 35 dB. For closed-loop gains of less than this value, one of the numerous forms of op amp compensation must be used.

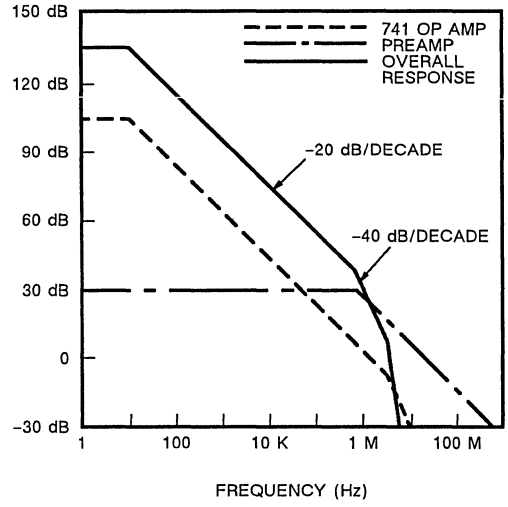


Figure 18. Bode Plot of Preamplifier and Second Stage

PREVENTING LATCH-UP IN MONOLITHIC DUAL JFETS

Ed Oxner
Central Applications

Monolithic JFETs offer the designer unmatched performance for a wide range of applications. While their monolithic structure offers tight matching and good drift characteristics it can also lead to a regenerative current flow known as latch-up. Fortunately, it is completely preventable, but only with some understanding of the mechanism by which it occurs.

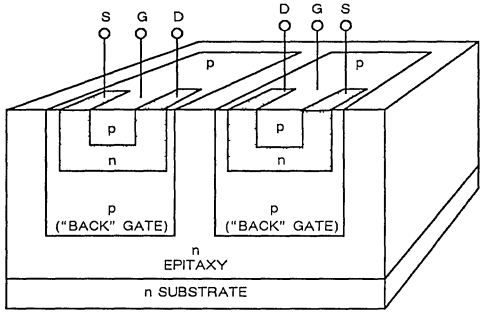


Figure 1. Cross-Sectional View of a Junction-Isolated Monolithic Dual JFET

Like CMOS, a monolithic JFET consists of multiple layers of both p- and n-doped silicon. Figure 1 offers a greatly simplified view. This construction technique is commonly called "junction isolation," so named for the fact that each junction in the monolithic structure is reverse biased. Ideally, junction isolation means a p-n junction will not conduct when a positive potential is applied to the n-doped region and a negative voltage is applied to the p-doped region. In practice, of course, there will be leakage currents.

Latch-up results when, as an unexpected result of normal functioning, conduction current flows that cannot be halted. This flow will stop only when the device burns out or power to the device is physically interrupted.

The potential for latch-up exists when a combination of p-n junctions forms an SCR – a silicon-controlled rectifier. An SCR consists of a pnp transistor and an npn transistor in a cascode arrangement as shown in Figure 2. SCR action occurs when the product of the individual current gains (Beta) of the npn and pnp exceed unity. If the base of the npn is more positive than its emitter, the npn turns on. Likewise, if the base of the pnp is more negative than its emitter, it turns on. Consequently, a positive potential applied to the npn's base will turn it on. Conduction through the npn pulls the pnp's base below its emitter potential (base-negative with respect to the emitter) and the pnp turns on, while conduction through the pnp pulls the npn base high (positive), resulting in the regenerative latch-up effect. Physically interrupting conduction is the only way to stop this effect.

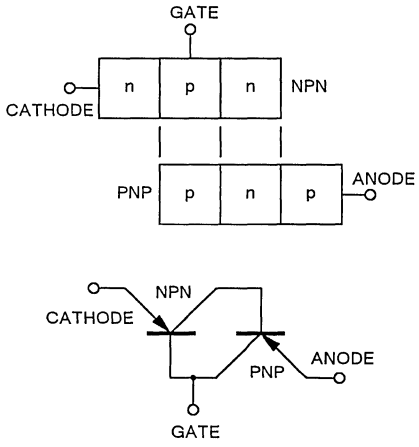


Figure 2. The Silicon-Controlled Rectifier, represented Symbolically and Electrically

In Figure 1's simplified cross-sectional view, both JFETs are junction-isolated from each other. The Figure shows a pair of n-channel JFETs with a p-doped region – representing the "back" gate – surrounded by an n-doped epi that forms an effective junction-isolated buffer between each JFET. This combination of p-n junctions, however, forms a potential SCR. This is more clearly shown in Figure 3.

The path in Figure 3 shows that SCR action will occur if either "back" gate is biased more positively than the opposing source (n-doped region) when the substrate is left floating.

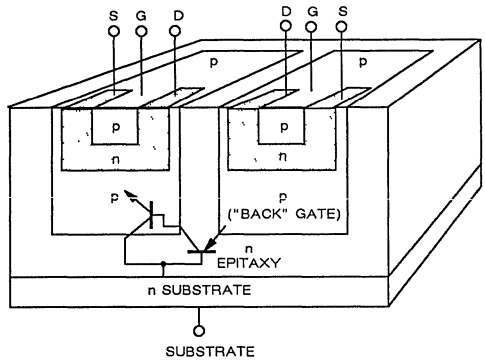


Figure 3. Cross-Sectional View of a Junction-Isolated Monolithic Dual JFET Showing SCR Effect

In some cases, such a combination of biases does not exist and latch-up will not be a worry. However, in many popular JFET applications, SCR action is entirely possible. Typical applications are shown in Figure 4.

As Figure 5 shows, preventing latch-up is simple. Bias the substrate at a positive potential equal to or greater than the positive potential of the uppermost gate. This prevents the parasitic pnp from conducting, and in turn halts any SCR action.

In the special case of a differential amplifier, substitute a current regulator for the source resistor. This not only ensures against latch-up but also improves the amplifier's common-mode rejection performance.

For monolithic dual JFETs available in the TO-78 case, pin 4 is the substrate. For the TO-71, the substrate is the can, and there is no pin connection. In this case, a bond to the can may be improvised with a spring clip; this is generally preferred to soldering a lead to the can.

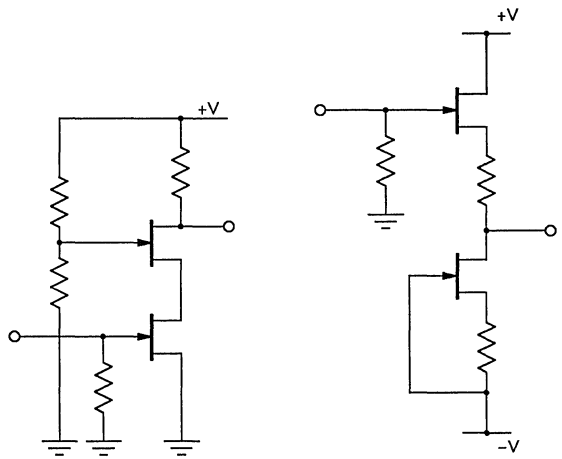
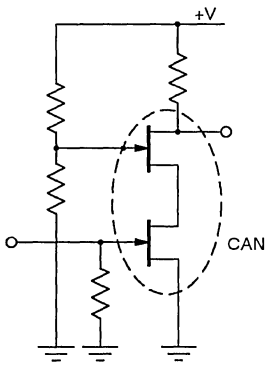
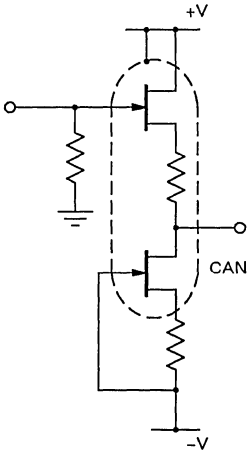


Figure 4. Typical Circuits Where Latch-Up is Possible

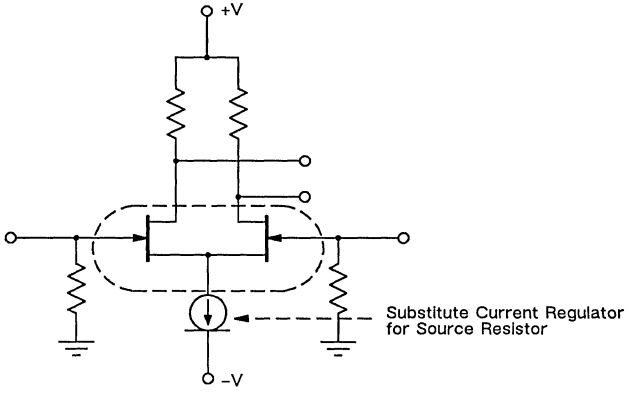


CASCODE AMPLIFIER

SUBSTRATE CONNECTION
TO-78 Pin 4
TO-71 Can



CASCODE CONSTANT-CURRENT
SOURCE FOLLOWER



DIFFERENTIAL AMPLIFIER

Figure 5. Procedures to Prevent SCR Latch-Up

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Siliconix incorporated

APPLICATIONS FOR THE 2N6908 SERIES JFET AMPLIFIER

Doyle Slack

INTRODUCTION

The Siliconix 2N6908 series is much more than a JFET; it is a complete monolithic amplifier circuit featuring a low-noise, low-leakage JFET and two parallel diodes from the gate of the device to the substrate. This application note will discuss the operation of the 2N6908 series and its uses and advantages. Also, several example circuits are included to show the 2N6908 series' versatility as an impedance matching circuit and/or small-signal amplifier.

DEVICE OPERATION AND SPECIFICATIONS

The 2N6908 series (2N6908, 2N6909, 2N6910) incorporates the features of two of our more popular JFET products, producing a unique combination of low noise and low leakage. Two parallel diodes are connected between the JFET gate and the substrate (which is tied to the fourth lead of the package). These diodes clip transient spikes and overvoltages, protecting the output of the circuit from sudden voltage fluctuations.

Figure 1 shows the two circuits and their connections to the leads of a TO-72 can. It also shows the pad layout and dimensions of the 2N6908 die for use in hybrid circuit applications. Added flexibillity can be achieved with the 2N6908 series when they are used as source-follower amplifiers. By varying the source resistor, a wide range of amplifiers can be designed – all featuring input protection. Table 1 shows some of the more important typical values for the 2N6908 series. A transfer characteristic graph is included in Figure 2 to give an idea of the operating range of the 2N6908 series.

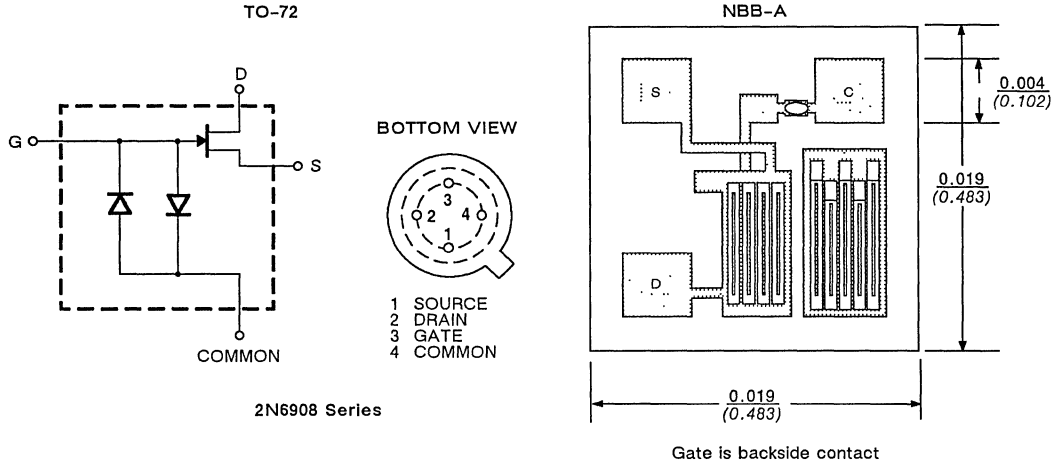

Figure 1. Schematic Diagrams, Lead Connections, and Die Layout for the 2N6908 Series.

Table 1. Typical Values for discussed parameters of the 2N6908 series

Parameter	2N6908 Family	Test Conditions
Diode Leakage	< 2 pA	V_{G4} = ±100 mV
JFET Leakage	< 1 pA	V_{GS} = 0 V, V_{DS} = 10 V
		V_{G4} = 0 V
Noise	10 nV/√Hz	V_{DS} = 10 V, V_{GS} = 0 V
		f = 10 Hz

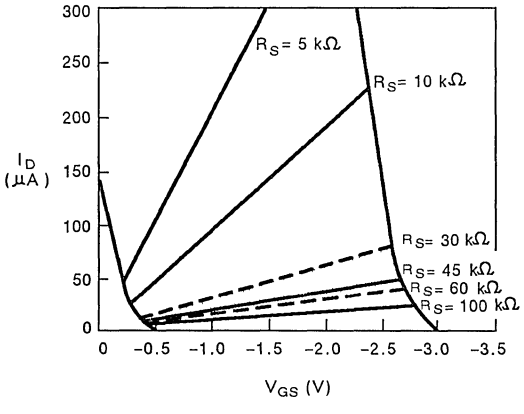

Figure 1. Graph of the Transfer Characteristics of the 2N6908 series

ADVANTAGES AND APPLICATIONS

Several advantages of the 2N6908 series – such as low noise, low leakage, and small size – have already been mentioned. These and other advantages over discrete amplifiers, including improvements in both circuit operation and ease of implementation, make this series very attractive:

1. A low-noise and low-leakage combination is effective in providing an extremely high input impedance and low loading. These characteristics allow connection to the outputs of high-impedance transducers with minimal signal loss and signal noise injection.
2. The diodes provide overvoltage protection for later stages. If voltage sensitive circuits follow the 2N6908 series part, the maximum output swing of the 2N6908 source follower amplifier will be less than a diode forward voltage drop above or below ground potential if the fourth lead of the device is grounded.
3. Monolithic design reduces space requirements to a minimum, allowing circuit placement in locations that are often impossible for discrete amplifiers. It also reduces the possibility of noise insertion from nearby sources because the case of the part is normally grounded to provide an effective RF shield. Also, the 2N6908 series' small die size makes it very attractive for use in hybrid circuits, such as those designed for hearing aids where minimizing space is an essential design factor.
4. Low-current/low-voltage capability makes the 2N6908 series amplifier ideal for battery operation. This is important for low-cost field operation and for portable equipment.

The most universal application of the 2N6908 series is in impedance matching for high-impedance sources (such as transducers) to low-impedance loads (such as transmission lines). Figure 3 demonstrates how simply the 2N6908 can solve the impedance problem. The input impedance of JFETs is typically in the range of 1000 G Ω (10^{12}) while the output impedance of the amplifier is set by the source resistor. In Figure 4, the 2N6908 is shown in a more specific application – as a preamplifier for an electret microphone.

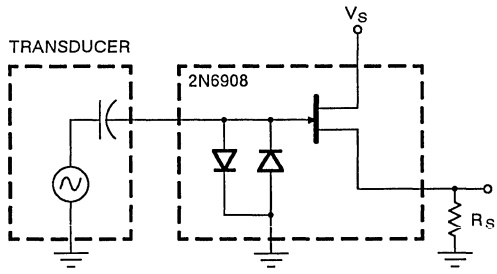

Figure 3. 2N6908 Devices Connected As Impedance Transformers

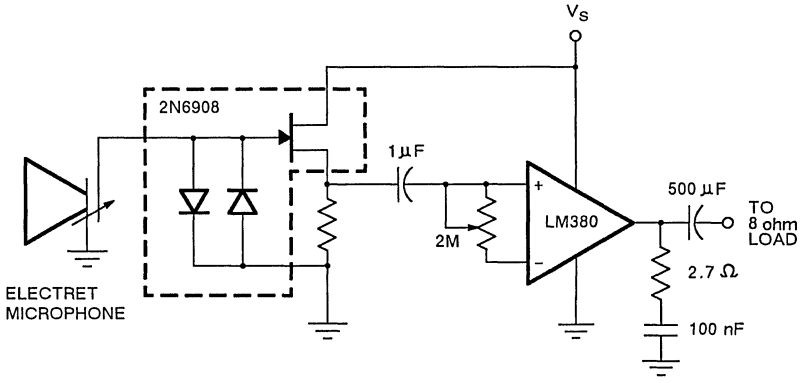

Figure 4. Schematic Diagram of An Audio Amplifier Using the 2N6908 As A Microphone Preamplifier

But what if an even lower load impedance, such as 50 Ω, from a transmission line is to be used? Figure 5 shows how the output impedance of the source follower circuit can be lowered even more with the help of a bipolar transistor. The reflected resistance through the base of the bipolar is paralleled with the effective output resistance of the 2N6908 circuit to produce an output resistance of less than 60 Ω and a voltage gain of better than 0.95 V/V. This allows both the source and load to be optimally matched with virtually no signal loss.

The bipolar-assisted source follower gives great flexibility by allowing interface between any ultra high-impedance source and a 50 Ω load with virtually no signal loss or noise insertion. Some examples of ultra high-impedance transducers are electret microphones, input preamplifiers for hearing aids, accelerometers for military and industrial sensing, infrared sensors, and ion chambers such as those used for industrial radiation exposure monitors.

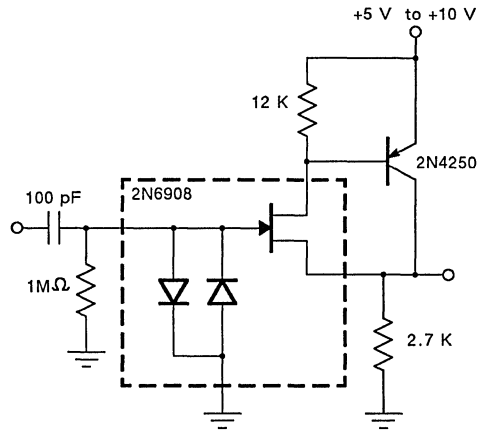

Figure 5. Schematic Diagram of the Bipolar Assisted Low Output Impedance Source-Follower Amplifier

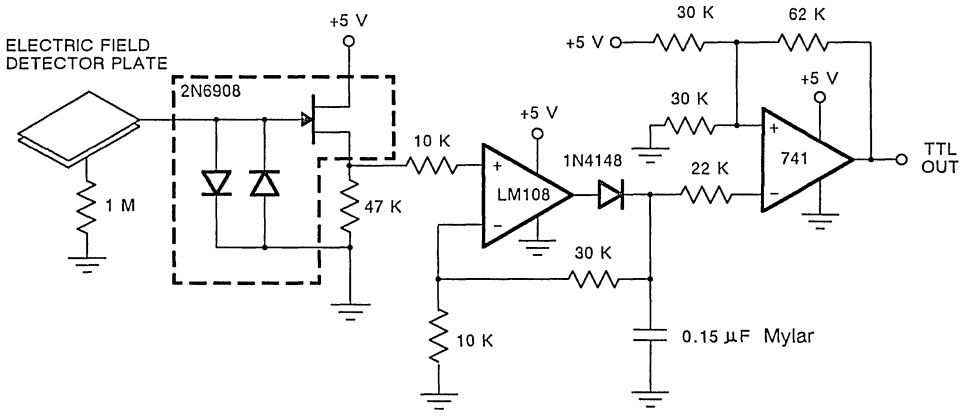

Figure 6. Schematic Diagram of the 2N6908 Series Proximity Sensor

Another example of how the 2N6908 family could be used is given in Figure 6. Here, the 2N6908 series circuit input is connected to a capacitive field sensor (as simple as a piece of double sided circuit board). Any induced voltage change on the plates is fed to the input of the peak detector section of the op-amp circuit. The Schmitt trigger monitors the voltage across the capacitor and changes its output state when the capacitor voltage crossed the 2.5 V trigger point. The output from the Schmitt trigger switches between 0 and 5 V and is microprocessor-compatible for sensor applications, such as computer-controlled intruder alarms.

Another transducer interface problem occurs when high impedance measurement networks are connected to operational amplifiers for differential measurement. This can be solved by the circuit shown in Figure 7. Here a pair of 2N6908 series parts has been used to monitor a high-impedance bridge for an instrumentation amplifier. This circuit allows precision measurement at low input signal levels and easy zeroing of the amplifier output.

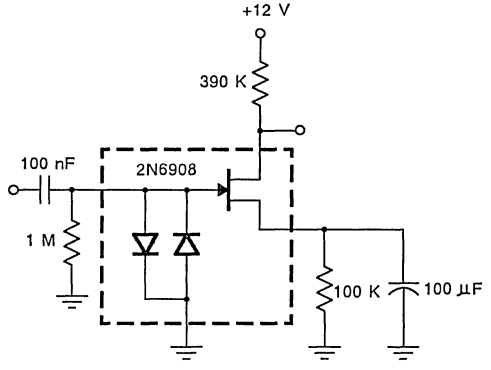

Figure 7. Schematic Diagram of the Low Signal 2N6908 High Impedance Instrumentation Amplifier

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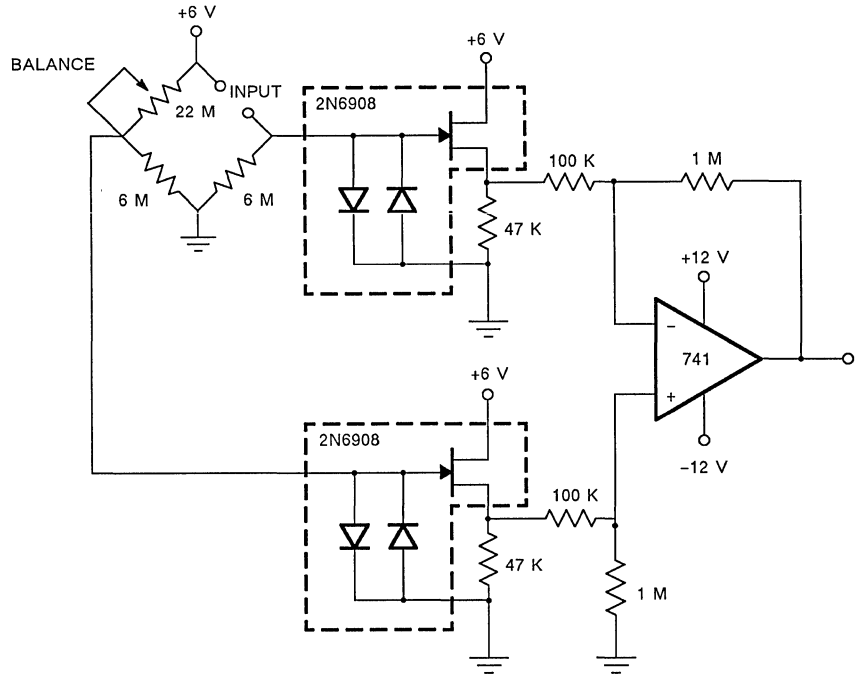

Figure 8. Schematic Diagram of the 2N6908 Series Low Power Common Source Amplifier

Another use for the 2N6908 is in the common-source amplifier mode where low power or battery operation is important. Figure 8 shows a circuit that will operate in the 10- to 20- μA range at a 12 V supply. voltage. The diode protection is still available in this configuration, but the circuit voltage gain will be between 10 and 20 V, with extremely low power consumption (approximately 250 μW). This is very desirable for remote or battery operation where minimum maintenance is important.

CONCLUSION

With its low noise and low leakage combination, the 2N6908 series amplifier is an ideal circuit for impedance matching. Although this series has been designed for source follower applications, it is flexible enough to be converted to any suitable amplifier design and still provide diode protection. There are many good reasons to include these devices in your designs, such as small size, outstanding performance, and reasonable cost, lower parts count, and higher reliability. These advantages make the 2N6908 series preferable for numerous small signal applications.

ANALOG SWITCHING USING FETS

SECTION 1: FETS AS ANALOG SWITCHES

INTRODUCTION

The past few years have seen a pronounced growth of analog/digital systems which employ integrated circuits. One of the interface elements in such a system is the digitally-controlled analog switch. As more and more applications arise for the analog switch, especially in the areas of industrial processing and control, the question is often asked: "Which is the best switch for my application?"

The sheer variety of applications precludes any pat answer to this question; however, the user of analog switches can gain valuable insight on the subject through an understanding of the nature of solid-state switches. Areas which require exploration include:

1. Base factors affecting switch performance.
2. Details of switch-driver circuit design.
3. Total switching characteristics of driver circuits and switches.
4. Characterization of the analog switch at high frequencies.

The intent of this section is to consider (1) above, in detail, with minor attention to the other areas.

Field-Effect Transistor Operation

The field-effect transistor (FET) is in effect a conductor whose cross-sectional area may be varied by the application of appropriate voltages. When the conducting area (the channel) is maximum, conductance is also maximum (minimum resistance). When the conducting area is minimum, conductance is minimum (maximum resistance). This phenomenon makes possible the use of FETs as analog switches. When conductance is maximum, the switch is in the ON state; when conductance is minimum, the switch is in the OFF state. In the ON state, an n-type channel contains n-type carriers; similarly, p-channel FETs contain p-type carriers. Cross-sections for three types of n-channel FETs are shown in Figure 1.

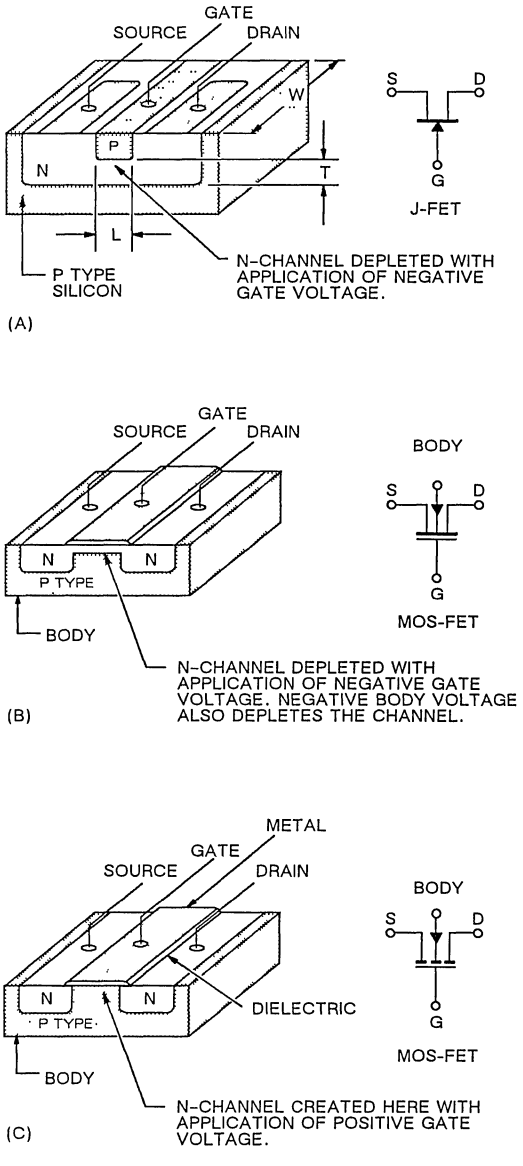

Figure 1. N-Channel FET Cross-Sections

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P-channel FET cross-sections are quite similar, except that the channel contains p-type carriers and the voltage polarities are reversed. Depletion-mode devices are shown in Figures 1A and 1B; these FET types have high channel conductance (are ON) with zero gate-channel voltage, and are characterized as "normally-ON" switches. An enhancement-mode FET is shown in Figure 1C. This device requires that voltage be applied to the control gate to create a conducting channel - the ON state. Enhancement-mode FETs are said to be normally-OFF.

For enhancement-mode devices, channel conductance (g_{DS}) is a function of length (L), width (W), thickness (T), carrier mobility (μ), and mobile carrier concentration (Nc):

$$g_{DS} = K_1 \frac{WT}{L} \mu Nc$$

Effective channel thickness and carrier concentration are functions of the electric field in the channel. Voltage on the control gate changes the field, and hence the channel conductance, g_{DS}.

The gate voltage is applied with respect to the channel (source or drain). In most devices, the function of the source and drain can be interchanged, because of symmetrical FET geometry. By convention, however, voltage is specified between gate and source, V_{GS}. Figure 2 shows the variation of g_{DS} with V_{GS} for both n- and p-channel devices. In all cases, $g_{DS} = 1/r_{DS}$.

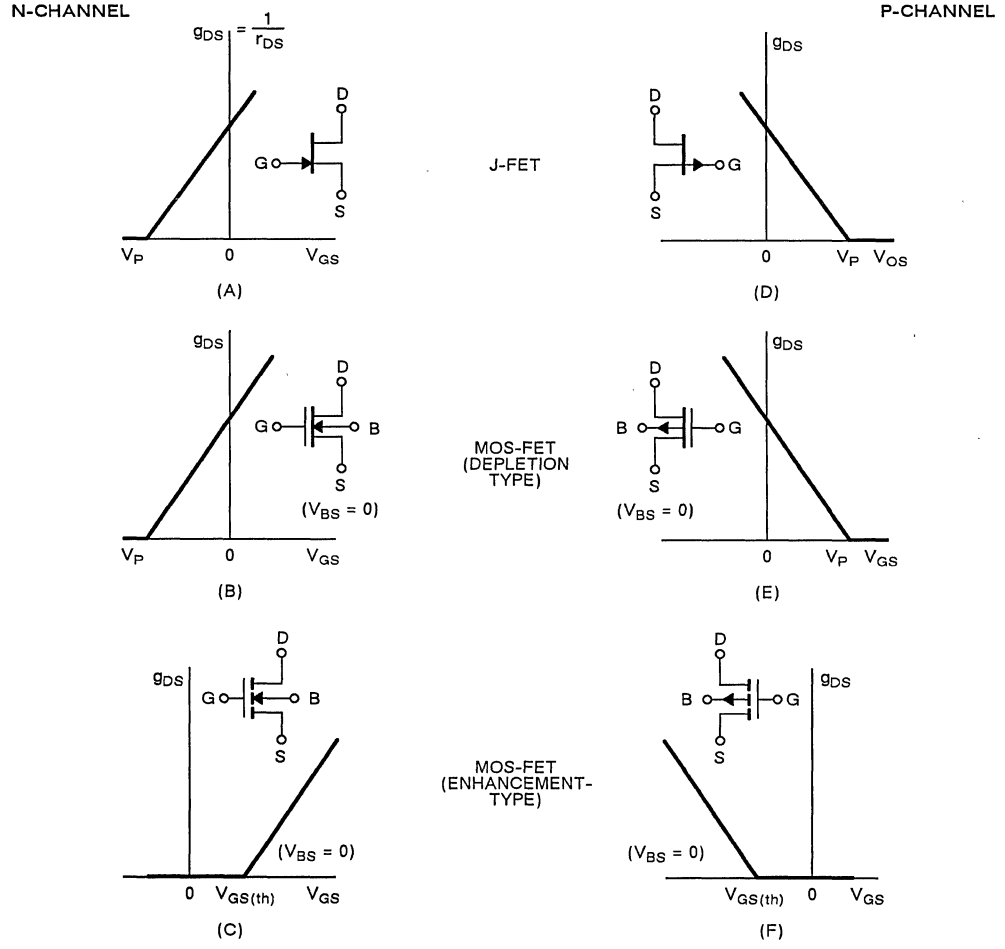


Figure 2. Channel Conductance vs Gate-Source Volatage

Note that the slopes ($\Delta g_{DS}/\Delta V_{GS}$) for all three types of n-channel FETs are constant and positive, while the slopes for the p-channel devices are constant and negative. n- and p-channel depletion-mode FETs are ON when $V_{GS} = 0$, while enhancement-mode devices of both types are OFF when $V_{GS} = 0$. Typically, the cut-off voltage, $V_{GS(off)}$, is designed to fall in the 1-to-10 volt range, while the gate-to-source threshold voltage, $V_{GS(th)}$ - that amount of voltage applied to the point where the device begins to conduct - falls in the 1-to-5 volt range. Figure 2 also demonstrates that g_{DS} is approximately a linear function of V_{GS}, with zero g_{DS} occurring at $V_{GS(off)}$ or $V_{GS(th)}$, as follows:

$$g_{DS} = K_2 |V_{GS} - V_{GS(off)}| \quad \text{(depletion)}$$

$$g_{DS} = K_2 |V_{GS} - V_{GS(th)}| \quad \text{(enhancement)}$$

For a given active area, a junction FET (JFET) will have a higher conductance slope than a MOS FET. Additionally, n-channel carriers have higher mobility than p-type carriers. Thus, all things being equal, n-type FETs have higher g_{DS} ($=1/r_{DS}$) than p-type devices. If the active area of the device is increased to raise the g_{DS} level, three other FET parameters will also be increased: leakage, capacitance, and cost. The design tradeoffs of these latter parameters are discussed in this Application Note.

When a FET is used as an analog switch, the drain-to-source voltage, V_{DS}, may be either positive or negative. In the OFF state, a typical switch may have $V_{DS} = \pm 20V$. In the ON state, current flows equally well from drain to source or from source to drain (the channel is resistor). For most applications, the voltage across the switch will be small.

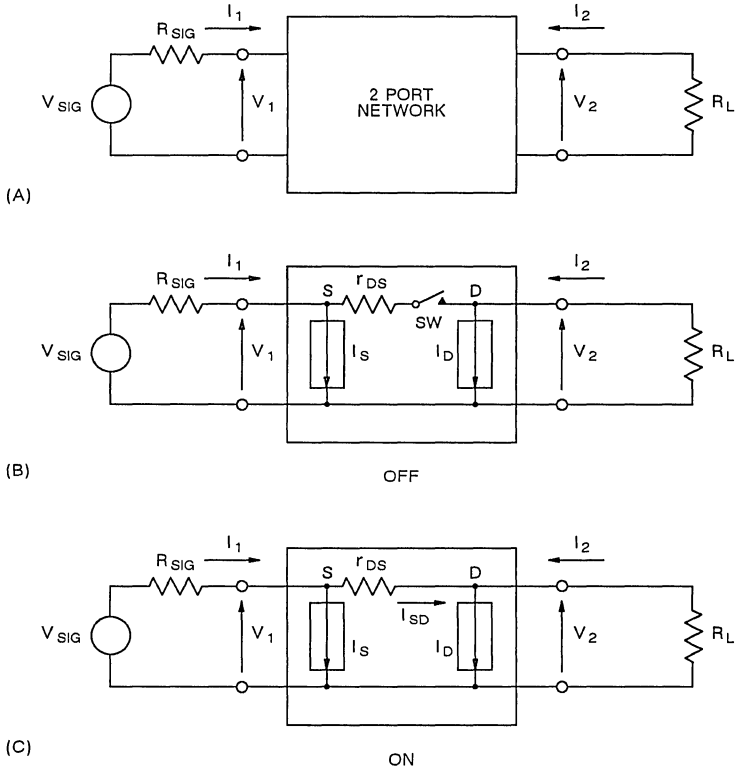


Figure 3. DC Equivalent Circuits

DC Equivalent Circuits

The perfect switch would have infinite resistance (zero conductance) when open and zero resistance (infinite conductance) when closed. While the FET is not a perfect switch, there are many applications where this deviation from perfection is unimportant. This statement can be justified by an analysis of the implications of the circuits shown in Figure 3.

The general two-port network in Figure 3A couples the signal source, V_{SIG}, to a resistive load, R_L. The network can be characterized by its terminal voltage and currents. V_1, V_2, I_1, and I_2. Figure 3B shows the equivalent circuit of a FET switch in the OFF state. In this condition, the "source" and "drain" are not connected to one another; however, two leakage current sources, I_S and I_D, are present. The same device is shown in the ON state in Figure 3C. The following typical values are assumed for the circuit:

V_{SIG} = 10 V (full scale)
$I_S = I_D$ = 1 nA
r_{DS} = 100 Ω
R_L = 200 kΩ
R_{SIG} = 10 Ω

In the following calculations, leakage current (deviation from the state of a perfect switch) is expressed in terms of error percentage.

OFF Condition Calculation

(1) $I_1 = I_S$ = 1 nA

$V_{SIG} - V_1 = I_1 \cdot R_{SIG}$ = (1 nA) (10 Ω) = 10 nV

$$\% \text{ Error in } V_1 = \frac{(10^{-8}\text{ V})\ (10^2)}{10\text{ V}} = 1 \times 10^{-7}\%$$

(2) $I_2 = I_D$ = 1 nA

$V_{2(off)} = I_2 R_L$ = (1 nA) (200 kΩ) = −200 μV

$$\% \text{ Error in } V_{2(off)}^{*} = \frac{(2 \times 10^{-4})\ (10^2)}{10} = 0.002\%$$

ON Condition Calculation

$I_1 = I_S + I_D - I_2$

$$I_2 = \frac{V_2}{R_L} \simeq \frac{V_{SIG}}{R_L + R_{SIG} + r_{DS}}$$

$V_{SIG} - V_2 \simeq$ = (50 μA) (110 Ω) = 5.5 mV

$$\% \text{ Error in } V_2^{*} = \frac{(5.5 \times 10^{-3})\ (10^2)}{10} = 5.5 \times 10^{2} = 0.005\ \%$$

* Referred to V_{SIG} (full scale)

The foregoing calculations indicate that for all but the most critical applications the performance of the FET equivalent circuits in Figure 3 is a good approximation of the perfect switch. In particular, the OFF condition leakage currents contribute only a negligible portion of total error.

The actual error currents of three different types of FET switches are shown in Figure 4. The measured error is much lower than the 1 nA (1000 pA) obtained from the sample calculations. These data are taken from a MOS FET, an n-channel JFET, and a complementary MOS (CMOS) combination including a p-channel device and an n-channel device diffused onto the same substrate. The behavior of these FETs as elements of analog switching integrated circuits will be dealt with in detail elsewhere in this Application Note.

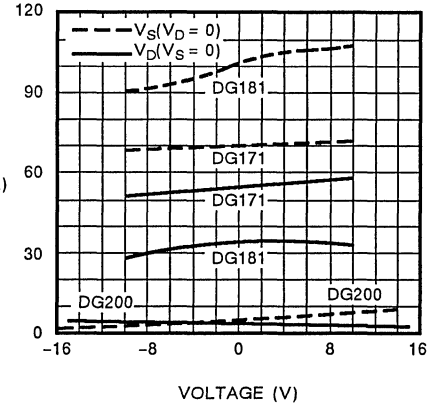


Figure 4. FET Switch Error Currents

The JFET as a Switch

A suitable driving circuit must be considered when assessing the performance of the JFET as a switch. Such a circuit is shown in Figure 5.

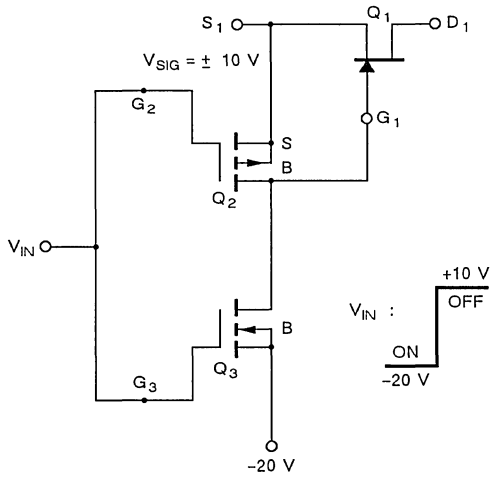
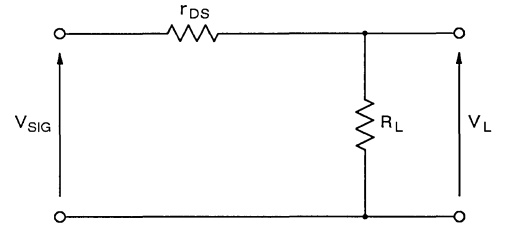


Figure 5. JFET Switch Control Circuit

Note that Q_1 is an n-channel JFET, Q_2 is an enhancement-mode p-channel MOS FET, and Q_3 is an enhancement-mode n-channel MOS FET. From Figure 2, V_{IN} of −20 V will turn Q_2 ON and Q_3 OFF, so that S_1 and G_1 are connected (V_{GS} = 0 V) and Q_1 is ON. If V_{GS} is allowed to vary, g_{DS} (=1/r_{DS}) will also vary. This variation in resistance appears as a source of error when the switch is ON, and the error is defined as resistance modulation. In Figure 6, the error percentage in the case of resistance modulation is greater than that which occurs when Δr_{DS} = 0.

The suggested driving circuit of Figure 5 eliminates Δr_{DS} at low frequencies. The typical positive supply voltage is +10 V and the typical negative supply voltage is −20 V. In order for V_{GS} to change, current must flow through Q_2, which is ON. There are only two possible current paths through Q_2; (1), through Q_3, which is OFF and subject only to variations in leakage current, or (2), into the gate of Q_1, which is also subject to leakage current. Since both paths through Q_2 provide only negligible changes in V_{GS}, their effect in the circuit may be ignored. As the switching frequency is increased, capacitive reactance will provide lower impedance paths, so that some degree of Δr_{DS} is possible. Thus two conditions contribute to Δr_{DS} = 0 in the circuit. First, $V_{SIG} \simeq V_{G1}$, due to the low impedance between these points. Second, the output impedance of Q_3 (driver output) is very large when compared to the R_{ON} of Q_2.



NO RESISTANCE MODULATION:

$$\% \text{ ERROR} = \frac{-100}{1+\frac{R_L}{r_{DS}}}$$

WITH RESISTANCE MODULATION:

$$\% \text{ ERROR} = \frac{-100}{1+\frac{R_L}{r_{DS}+\Delta r_{DS}}}$$

Figure 6. Error Due to Switch ON-Resistance (r_{DS})

When V_{IN} is +10 V, Q_2 is OFF and Q_3 is ON; G_1 is at −20 V and Q_1 is OFF. In Figure 7, note that Q_1 will remain OFF only so long as $V_{SIG} > (V_{G1} - V_{GS(off)})$. $V_{GS(off)}$ is a negative voltage for an n-channel FET; thus the negative analog signal is limited by the $V_{GS(off)}$ of Q_1 and the negative supply ($V_{G1} \simeq$ −20 V).

The ON condition is also shown in Figure 7. g_{DS} is constant because with $V_{G1} = V_{SIG}$ imposed by the switch control circuit, $V_{GS} \simeq 0$.

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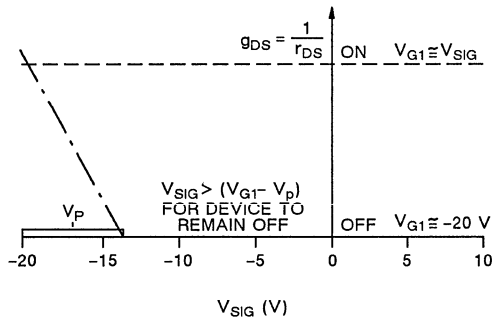


Figure 7. Switch ON Condition

The MOS FET as a Switch

The p-channel enhancement-mode MOS FET is currently used in more applications than its n-channel counterpart. The consideration of MOS FET switch performance will thus center on p-channel devices.

The ON and OFF conditions of the MOS FET are analyzed in Figure 8. When the device is in the ON stage, note that the FET begins to turn ON when V_{SIG} (V_S or V_D) becomes $V_{GS(th)}$ volts more positive than V_G (= -20 V).

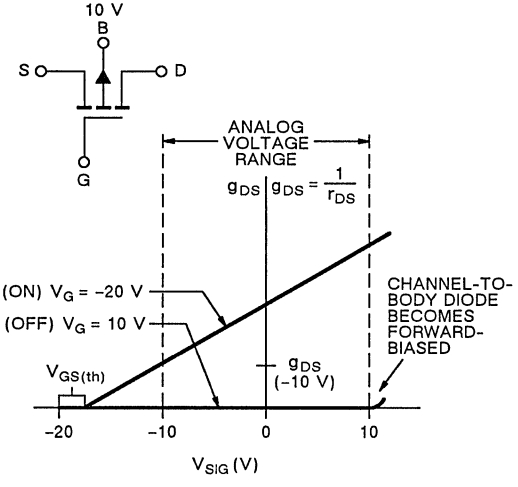


Figure 8. PMOS Channel Conductance (r_{DS}) vs Signal Voltage

Figure 8 also indicates that at any given point along the g_{DS} vs V_{SIG} curve, a unique value of g_{DS} will be obtained. Assume that a battery is inserted between the source and the gate, with the source clamped to the body as shown in Figure 9.

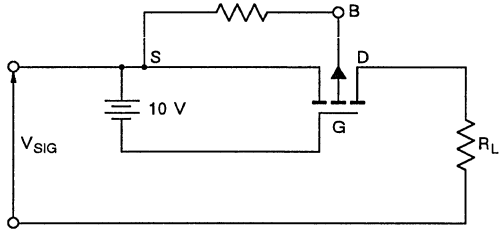


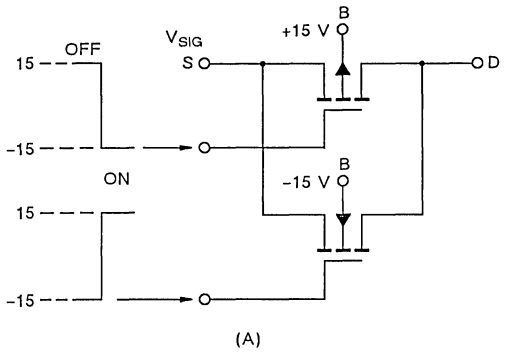
Figure 9. "Floating" Battery and Clamped Source

A constant voltage between source and gate will produce a constant value of g_{DS} vs V_{SIG}, provided that the body-to-source voltage is also constant. In a MOS FET, variation of the body-to-source voltage will also cause a modulation of g_{DS}. To further complicate the picture, several MOS FETs will have a common body when they are integrated on a single chip. Finally, the construction of a "floating battery" circuit is difficult. Thus MOS FET switch designers currently cope with the problem of Δr_{DS} by specifying r_{DS} for a given switch at several points over the entire analog voltage range.

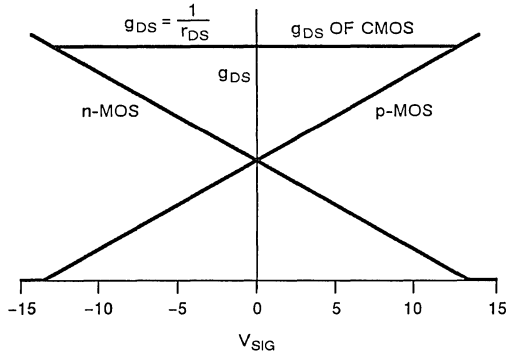
Referring to the switch in the OFF condition (V_G = +10 V), it is apparent that no problem will exist until the source-to-body or drain-body diode becomes forward-biased.

The CMOS Switch

As noted previously, the typical PMOS switch circuit will exhibit a variation in ON conductance as the analog voltage is varied. This undesirable characteristic can be overcome by paralleling p- and n-channel FETs, as shown in Figure 10A. For the ON state, the n-channel gate is forced positive and the p-channel gate is forced negative. Figure 10B shows the combined conductance of the two FET switches. The integrated combination of n-channel and p-channel devices on a common substrate is referred to as complementary MOS (CMOS).

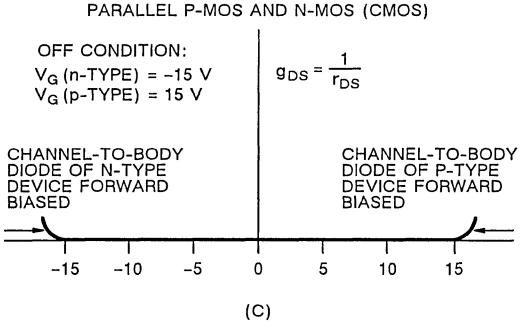


(A)



	p-MOS	n-MOS	
V_G	-15 V	+15 V	ON
V_G	+15 V	-15 V	OFF

(B)



(C)

Figure 10. Characteristics of CMOS Devices

The OFF condition for the CMOS device will be maintained so long as the channel-to-body diodes do not become forward-biased, as shown in Figure 10C.

The major advantages the CMOS construction technique makes to analog switching are:

- Lower r_{DS} variation with analog signal characteristics, similar to the performance of a junction FET.
- Analog signal range extends to + and - supply voltages. For instance, using the same ±15 V supplies typical of operational amplifiers, the signal-handling capability of the system is limited by the op amp, not by the switch.

Summary of FET Switch Performance and Tradeoffs

Figure 11 compares the performance of two switch types with respect to $r_{DS(on)}$ vs V_{SIG}.

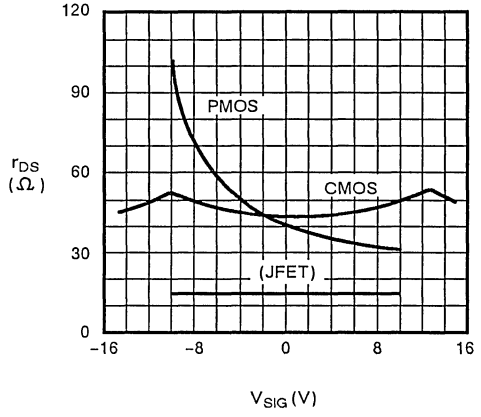


Figure 11. Performance of Three FET Switches

The curves in Figure 12 define the maximum r_{DS} (or Δr_{DS}) which can exist for a given allowable error percentage with a fixed value of R_L. Recall that in the circuit in Figure 3, a resistive load of 200 kΩ was assumed. If it is also assumed that an error level of 0.1% is tolerable, then r_{DS} = 200 Ω is the maximum allowable switch resistance. On the other hand, if settling time is not critical, then an R_L of 1 MΩ, yielding r_{DS} = 1 kΩ is permissible.

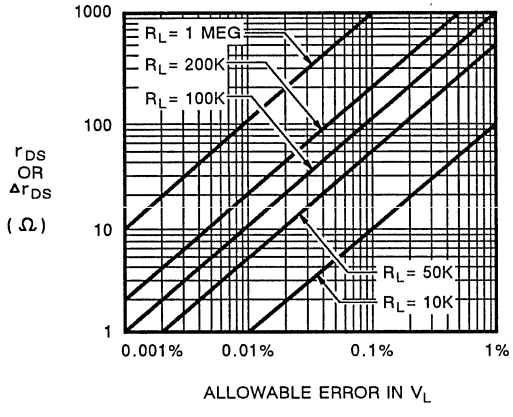
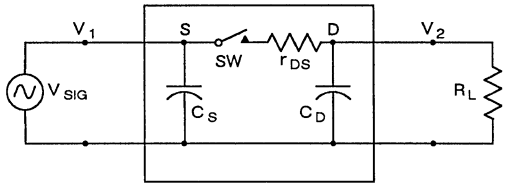
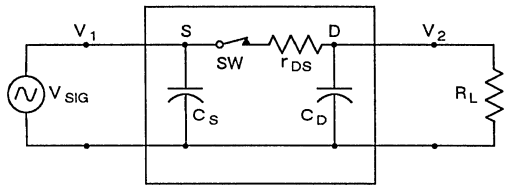


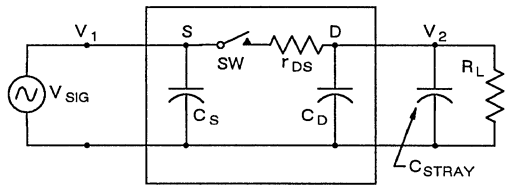
Figure 12. Tolerable Level of Δr_{DS} and r_{DS}



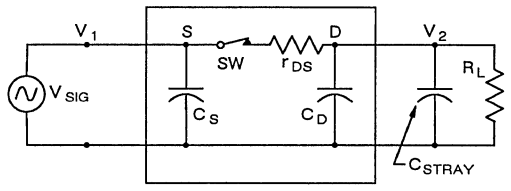
OPEN SWITCH CAPACITANCE



CLOSED SWITCH CAPACITANCE



OPEN SWITCH CONTAINING STRAY CAPACITANCE
$C_L = C_D + C_{STRAY}$



CLOSED SWITCH CONTAINING STRAY CAPACITANCE

Figure 13. Switch Settling Time Equivalent Circuits

In situations where settling time is indeed a design consideration, the circuits in Figure 13 will provide an overview of the exact nature of settling time for V_2 (= V_L) at turn-OFF and turn-ON. For a turn-ON signal, C_L charges through r_{DS}. During turn-OFF, C_L discharges through R_L. For a system error level of 0.1%, R_L = 1000 r_{DS}; therefore, the maximum settling time for V_2 occurs during turn-OFF.

Consider a switch with $C_S = C_D$ = 3 pF, for an application requiring 0.1% accuracy with 5 µs settling time. A typical stray capacitance (C_{IN} for an op amp) may be 6 to 7 pF. Therefore, C_L = 3 pF + 7 pF = 10 pF. Resistance loads, R_L, of 100 kΩ, 50 kΩ, and 25 kΩ are considered for the switch. The time required for an RC system to settle to within 0.1% of its final value is 6.9 time constants (6.9 RC). Table 1 shows the R_L and r_{DS} values necessary to satisfy a number of settling time specifications. From Table 1, it is apparent that so long as $R_L \leq 72$ kΩ, the desired settling time of 5 µs will be achieved.

Table 1

R_L (kΩ)	r_{DS} (Ω)	C_L (pF)	t_{ON} (V_2)** (0.1% settling time) (ns)	t_{OFF} (V_2)** (0.1% settling time) (μs)
25	25	10	1.72	1.72
50	50	10	3.45	3.45
* 72	72	10	5.00	5.00
100	100	10	6.90	6.90

* Maximum R_L for t_{set} = 5 μs
* Does not include delay times

If cost is a design constraint, it is wise to make a close analysis of actual system switch requirements. Too often, designers buy unnecessary performance capability. In Table 1, the switch with r_{DS} = 25 Ω costs nearly twice as much as does the switch with r_{DS} = 50 Ω, yet either switch will meet the 5 μs settling time specification.

Switch Capacitance

In general, the lower the switch capacitance the better the switching time and high-frequency isolation performance.

The simplified representation of switch capacitance shown in Figure 13 can be used to provide a very good estimate of what problems (if any) will be caused by switch capacitance in a given application.

In general, capacitance is proportional to the active area in a FET chip, prior to bonding onto a header. Additional stray capacitances are introduced when the leads are brought out through the device package. Thus, as lower r_{DS} (higher g_{DS}) is required, the active area is generally increased to obtain that parameter. The increase in area leads to an increase in capacitance.

The foregoing statements are true so long as one is dealing with a given device type. However, in transition from a JFET to a PMOS device, a significant difference will be observed in the active areas required for a given r_{DS}. Figure 14 compares the area of a JFET (from the hybrid DG181 circuit) and the monolithic PMOS circuit. Note that the r_{DS} for the JFET is approximately one-third that of the PMOS device, while the active PMOS area is almost three times greater than that of the JFET. Yet the ratio of PMOS-to-JFET capacitance is almost 2:1.

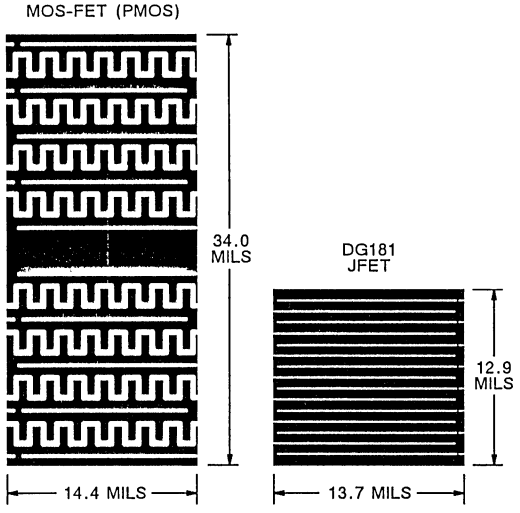


Figure 14. Active Area Comparison of PMOS and JFET Switches

Switch Comparison

A comparison between the characteristics of the three types of JFET switches is made in Table 2.

Table 2

Switch Type	Analog Signal Range	r_{DS}	Δr_{DS}	Leakage I_D or I_S
PMOS	$(V_- - V_{GS(th)}) < V_{SIG}$*	High	High	Low
JFET	$(V_- - V_{GS(off)}) < V_{SIG}$*	Low	Low	Low
CMOS	$V_- \leq V_{SIG} \leq V_+$	Med.	Med.	Low

* Both $V_{GS(th)}$ (for PMOS) and $V_{GS(off)}$ (for N-channel JFET are negative voltages
V_- is defined as positive supply voltage
V_+ is defined as negative supply voltage

This section of this Application Note has surveyed the characteristics of FET switches and their associated drivers. In considering the FET as an analog switch, discussion has largely centered on the devices themselves, including specific load problems and applicable driver circuits. Total switch performance is a function of the switch and the switch driver. Typically, high-performance switch drivers require numerous switching transistors. When discrete devices are considered, the total parts count will be high and the cost will be prohibitive. From the standpoint of cost, improved performance, and smaller size, the integrated circuit FET switch and driver is often the superior choice.

SECTION 2: DMOS FET ANALOG SWITCHES AND SWITCH ARRAYS

INTRODUCTION

This section of this Application Note describes in detail the principle of operation of the SD5000/210 series of high-speed analog switches, switch arrays, and drivers. It also contains an explanation of the most important switch characteristics. Application examples, test data, and other application hints are included.

Description

The Siliconix SD210 and SD5000 series are single and quad monolithic arrays, respectively, of single-pole single-throw analog switches. The switches are n-channel enhancement-mode silicon field-effect transistors that are built using double-diffusion silicon-gate technology.

This family of devices is designed to handle a wide variety of video, fast ATE and telecom, analog switching applications. They are capable of ultrafast switching speeds (t_r = 1 ns, t_{OFF} = 9 ns) and excellent transient response. Thanks to the reduced parasitic capacitances, DMOS can handle wideband signals with high OFF-isolation and minimum crosstalk.

The SD210 series of single-channel FETs is available non-zenered to reduce leakage and in Zener protected versions to reduce electrostatic discharge hazards. The SD5000 series is presented in 16-lead dual in-line plastic or side braze ceramic packages, as well as in 14-lead SOT plastic packages. Analog signal voltage ranges up to ±10 V and frequencies up to 1 GHz can be controlled.

Applications

Thanks to the fast switching speeds, low ON-state resistance, high channel-to-channel isolation, low capacitance, and low charge injection, these DMOS devices are especially well suited for a variety of applications such as: high-speed video/audio switching, fast analog or digital signal multiplexing, sample and hold, choppers, etc.

A few of the many possible application areas for DMOS analog switches (and their improved characteristics) are listed below:

1. Video and RF switching (high speed, high off-isolation, low cross-talk):
   - Multiple video distribution networks
   - Sampling scanners for RF systems

2. Audio routing (glitch-and noise-free)
   - High-speed switching
   - Audio switching systems using digitized remote control

3. Data acquisition (high speed, low charge injection, low leakage):
   - High-speed sample and hold
   - Audio and communication analog-to-digital converters

4. Other:
   - Digital switching
   - PCM distribution networks
   - UHF Amplifiers
   - VHF Modulators and Double-Balanced Mixers
   - High-speed inverters/drivers
   - Switched capacitor filters
   - Choppers

Principle Of Operation

The electrical symbol shown in Figure 15 provides several important bits of information: It depicts an n-channel enhancement-mode device with an insulated gate and asymmetrical structure. The gate protection Zener is shown with broken lines to indicate that, although it is present on the chip, it is not a main constituent of the fundamental switch structure.

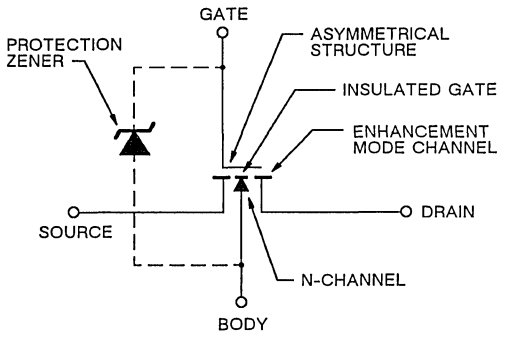


Figure 15. DMOS Electrical Symbol

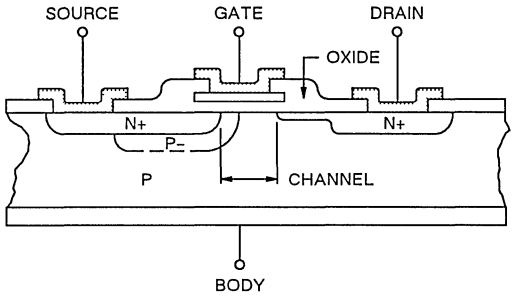


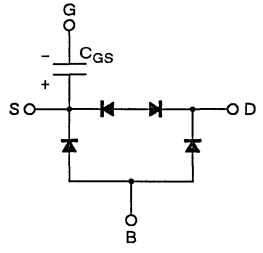
Figure 16. Cross-sectional View of the Idealized DMOS Structure

Each switch is a DMOS n-channel field-effect transistor of the enhancement-mode type: that is, the device is normally OFF when gate-to-source voltage (V_{GS}) is 0 V. The lateral double-diffused MOS (DMOS) transistor, shown in cross-section in Figure 16, has three terminals (source, gate, and drain) on the top surface and one (the body or substrate) on the bottom of the chip. A Zener diode with a breakdown voltage of approximately 40 V is added to protect the gate against overvoltage and electrostatic discharges.

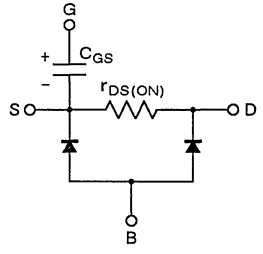
The double-diffusion process creates a thin self-aligning region of p-type material, isolating the source from the drain region. The very short channel length that results between the two junction depths permit achieving extremely low source-to-drain and gate-to-drain capacitances at the same time that provides good breakdown voltages.

The silicon-gate process allows for high manufacturing repeatability and very stable performance without the instabilities associated with the metal-gate technique.

When the gate potential is equal to or negative with respect to the source, the switch is OFF. In this state, the p-type material in the channel forms two back-to-back diodes and prevents channel conduction (Figure 17a). If a voltage is applied between the S and D regions, only a small junction leakage current will flow.



(A) EQIUIVALENT "OFF" CIRCUIT



(B) EQUIVALENT "ON" CIRCUIT

Figure 17.

The oxide insulator present between gate and source forms a small capacitor that accumulates charge. If the gate-to-source potential (V_{GS}) is made positive, the capacitive effect attracts electrons to the channel area immediately adjacent to gate oxide. As V_{GS} increases, the electron density in the channel will exceed the hole density, and the channel becomes an n-type region. As the channel conductivity is enhanced, the n-n-n structure then becomes a simple silicon resistor through which current can easily flow in either direction. Figure 18 shows the normal mode of operation of a single switch for ±10 V analog signal processing. Note that the source is recommended for the input since feedback or reverse transfer capacitance is lower when the drain is used as the output. In this case, the gate is driven by +20, −10 V for which an SD5200, SD210, or D211 could be used.

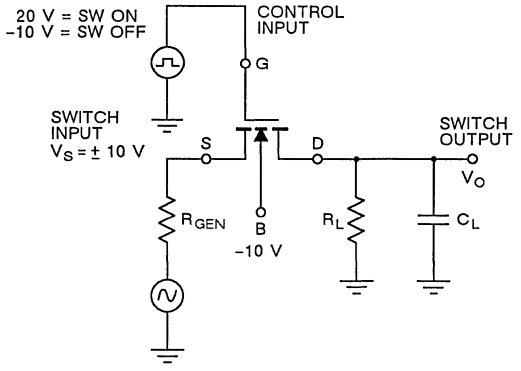


Figure 18. Normal Switch Configuration for ±10 V Analog Switch

As can be seen from Figures 17a and 17b, the body-source and body-drain pn junction should be kept reverse biased at all times: otherwise, signal clipping and even device damage may occur if unlimited currents are allowed to flow. Body biasing is conveniently set, in most cases, by connecting the substrate to V-.

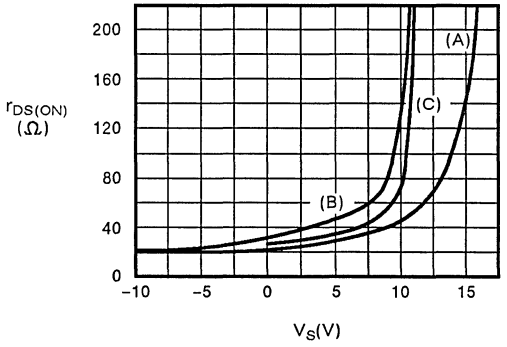
Main Switch Characteristics

$r_{DS(on)}$

ON-channel resistance is controlled by the electric field present across and along the channel. Channel resistance is mainly determined by the gate-to-source voltage difference. When V_{GS} exceeds the threshold voltage (V_T), the FET starts to turn on.

Numerous applications call for switching a point to ground. In these cases the source and substrate are connected to ground and a gate voltage of 3 to 4 V is sufficient to ensure switching action.

With a V_{GS} in excess of +5 V, a low resistance path exists between the source and the drain. The circuit shown in Figure 18 exhibits the $r_{DS(on)}$ vs. analog signal voltage relationship shown in Figure 19.



(A) V_{BODY} = 10 V: V_{GATE} = 20 V
(B) V_{BODY} = 10 V: V_{GATE} = 15 V
(C) V_{BODY} = 0 V: V_{GATE} = 20 V

Figure 19. ON-Resistance Characteristics

When the analog signal excursion is large (for example ±10 V) the ON-channel resistance changes as a function of signal level. To achieve minimum distortion, this ON-channel resistance modulation should be kept in mind, and the amount of resistance in series with the switch should be properly sized. For instance, if the switch resistance varies between 20 Ω and 30 Ω over the signal range and the switch is in series with a 200-load, the result will be a total ΔR = 4.5%. Whereas, if the load is 100 kΩ, ΔR will only be 0.01%.

Threshold Voltage

The threshold voltage (V_T) is a parameter used to describe how much voltage is needed to initiate channel conduction. Figure 20 shows the applicable test configuration. In this circuit, it is worth noting, for instance, that if the device has V_T = 0.5 V, when V+ = 0.5 V, the channel resistance will be:

$$R_{channel} = \frac{0.5\ V}{1\ \mu A} = 500\ k\Omega$$

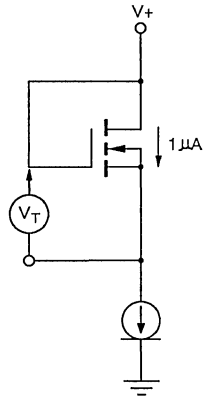


Figure 20. Threshold Voltage Test Configuration

Body Effect

For a MOSFET with a uniformly doped substrate, the threshold voltage is proportional to the square root of the applied source-to-body voltage. The SD5000 family has a non-uniform substrate, and the V_T behaves somewhat differently. Figure 21 shows the typical V_T variation as a function of the source-to-body voltage V_{SB}.

As the body voltage increases in the negative direction, the threshold goes up. In consequence, if V_{GS} is small, the ON-resistance of the channel can be very high. Figure 22 shows the effects of V_{SB} and V_{GS} on R_{ON}. Therefore, to maintain a low ON-resistance it is preferable to bias the body to a voltage close to the negative peaks of V_S and use a gate voltage as high as possible.

Charge Injection

Charge injection describes that phenomenon by which a voltage excursion of the gate produces an injection of electric charges via the gate-to-drain and the gate-to-source capacitances into the analog signal path. Another popular name for this phenomenon is "switching spikes."

Since these DMOS devices are asymmetrical[1], the charge injected into the S and D terminals are different. Typical parasitic capacitances are on the order of 0.2 pF for C_{DG} and 1.5 pF for C_{SG}.

[1]The chip geometry is such that non-identical behavior occurs when the source and drain terminals are reversed in a circuit.

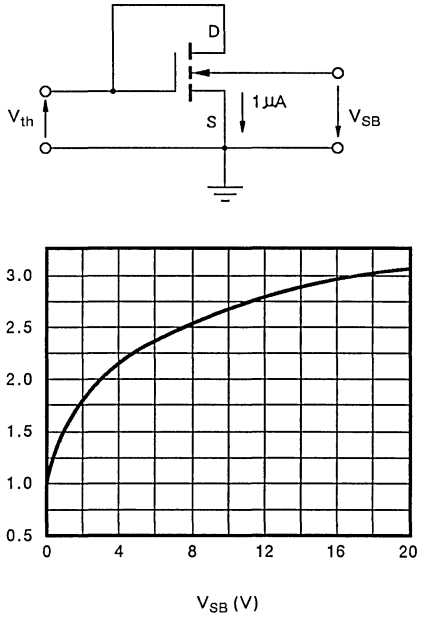


Figure 21. Threshold vs Source-to-Body Voltage

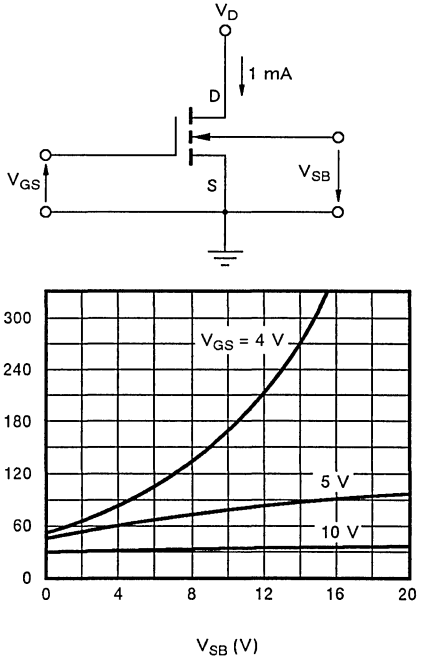


Figure 22. ON-Resistance vs Source-to-Body and Gate-to-Source Voltages

Another factor that influences the amount of charge injected is the amplitude of the gate-voltage excursion. This is a directly proportional relationship: the larger the excursion, the larger the injected charge. This can be seen by comparing curves (a) and (c) in Figure 23. One other variable to consider is the rate of gate-voltage change: Large amounts of charge are injected when faster rise and fall times are present at the gate. This is shown by curves (a) and (b) in Figure 23.

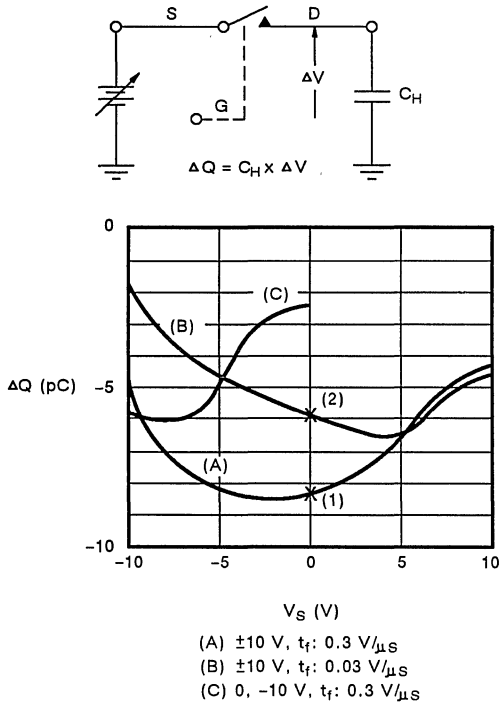
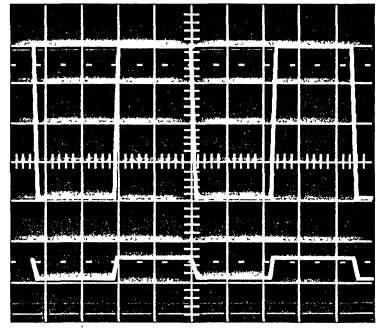


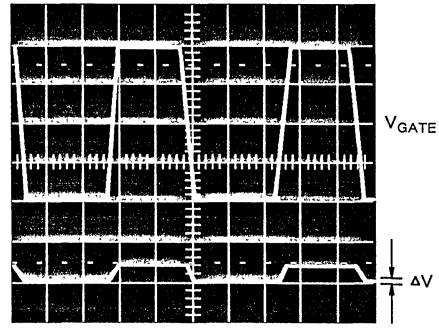
Figure 23. SD5000 Charge Injection

Switching spikes occur at switch turn-on as well as turn-off time. When the switch turns on, the charge injection effect is minimized by the usually low signal-source impedance. This low impedance tends to produce a rapid decay of the extra charge introduced in the channel. At turn-off, however, the injected charge might become stored in a sampling capacitor and create offsets and errors. These errors will have a magnitude that is inversely proportional to the magnitude of the holding capacitance.

Figure 23 illustrates several typical charge injection characteristics. Figure 24 shows some of the corresponding waveforms. The DMOS devices, thanks to their inherent low parasitic capacitances, produce very low charge injection when compared to other analog switches, either PMOS, CMOS, JFET, BIFET etc. Still, when the offsets created are unacceptable, charge injection compensation techniques exist that eliminate or minimize them. The solution basically consists of injecting another charge of equal amplitude but opposite polarity at the time when the switch turns off.



(A) TOP: 5 V/div HOR: 0.5 μs/div
BOT: 50 mV/div POINT (1)



(B) TOP: 5 V/div HOR: 2 μs/div
BOT: 50 mV/div POINT (2)

Figure 24. Waveforms for points (1) and (2) of Figure 7

Off-isolation And Crosstalk

The dc ON-state resistance is typically 30 Ω and the OFF-state resistance is typically 10^{10} Ω, which results in an OFF-state to ON-state resistance ratio in excess of 10^8. However, for video and VHF switching applications, the upper usable frequency limit is

determined by how much of the incoming signal is coupled through the parasitic capacitances and appears at the switch output when ideally no signal should appear there, in the OFF state.

Off-Isolation is defined by the formula:

$$\text{Off-Isolation (dB)} = 20 \log \frac{V_{OUT}}{V_{IN}}$$

When several analog switches are simultaneously being used to control high frequency signals, crosstalk becomes a very important characteristic. For video applications, the stray signal coupled via parasitic capacitances to the signal of an adjacent channel can form ghosts and signal interference. To help obtain high degrees of isolation, it becomes necessary to exercise careful circuit layout, reducing parasitic capacitive and inductive couplings, and to use proper shielding and bypassing techniques. Figure 25 shows the excellent off-isolation and crosstalk performance typical of this family of DMOS analog switches.

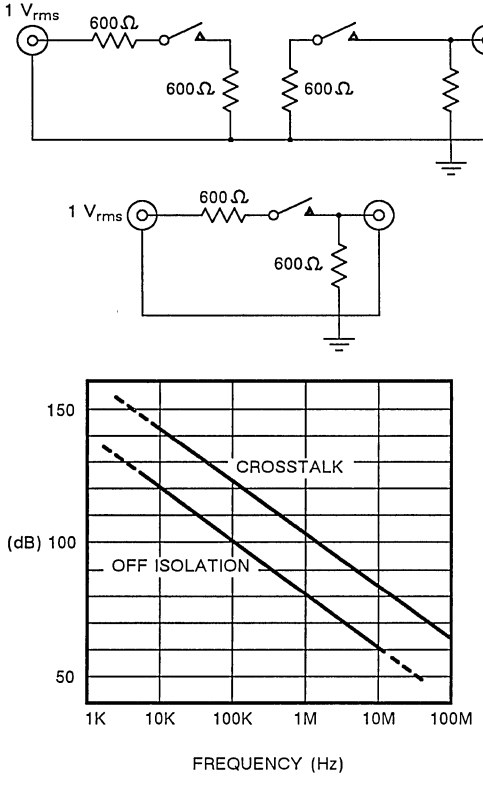


Figure 25. SD5000 Crosstalk and OFF-Isolation vs Frequency

Insertion Loss

At low frequencies, the attenuation caused by the switch is a function of its ON-state resistance and the load impedance. They form a simple series voltage divider network. As an example, for a 600 Ω load impedance the insertion loss for voice signals (1 V_{RMS} at 3 kHz) is less than 0.3 dB. Thus, the SD5000 series make good telephone crosspoint switches.

Speed

Because the ON-state resistance and input capacitance are low, the DMOS switches are capable of subnanosecond switching speeds. At these speeds the external circuit rather than the FET itself is often responsible for the rise and fall times that can be obtained. Let's consider the switching test circuit of Figure 26. At turn-on, the fall time observed at the drain is a function of R_G and of the input pulse amplitude and rise time. The sooner C_{GS} reaches V_T, the sooner turn-on will occur, and the lower the $r_{DS(on)}$ reached, the faster C_{DS} will be discharged.

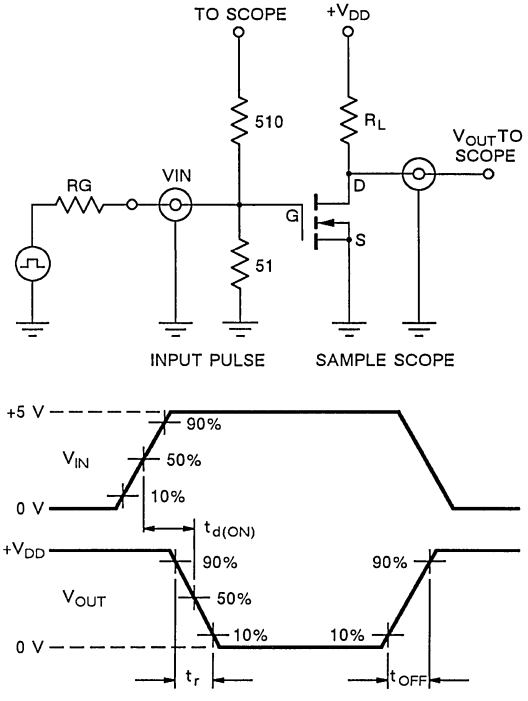


Figure 26. Switching Test Circuit

The turn-off time (or the rise time of V_D) is not as much limited by the velocity at which C_{GS} can be discharged by the gate control pulse, as it is by the time it takes to charge up C_{DS} and C_{DG} via the load resistor R_L. Table 3 shows typical performance obtained. It is important to realize that stray capacitance and parasitic inductances as well as scope probe capacitance can seriously affect the rises and fall times (switching speed).

Table 3 Typical Switching Times

V_{DD} (V)	R_L (Ω)	$t_{d(on)}$ (ns)	t_r (ns)	*t_{OFF} (ns)
5	680	0.6	0.7	9.0
10	680	0.7	0.8	9.0
15	1 K	0.9	1.0	14.0

*t_{OFF} is dependent on R_L and does not depend on the device characteristics

Drivers

The switch driver's function is to translate logic control levels, (either TTL, CMOS or ECL) into the appropriate voltages needed at the gate so that the switch can be turned ON or OFF.

The SD5200 operates as an inverter capable of driving up to 30 V. This high voltage rating, together with its high speed, make it an ideal driver for the other members of the SD5000 family. Figure 27 shows this and several other driving methods. The Siliconix D169 is a convenient TTL compatible driver.

Since switching times depend on the C_{GS} charge/discharge times, it is important to note that the driver's current source/sink capability plays a very important roll in the process.

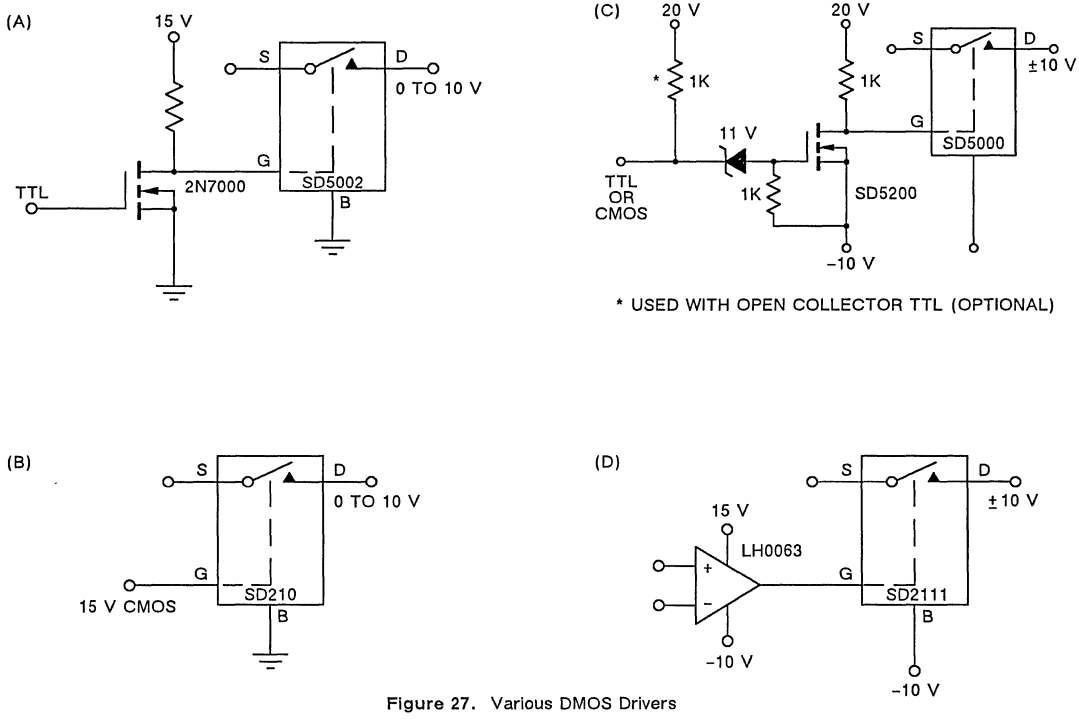


Figure 27. Various DMOS Drivers

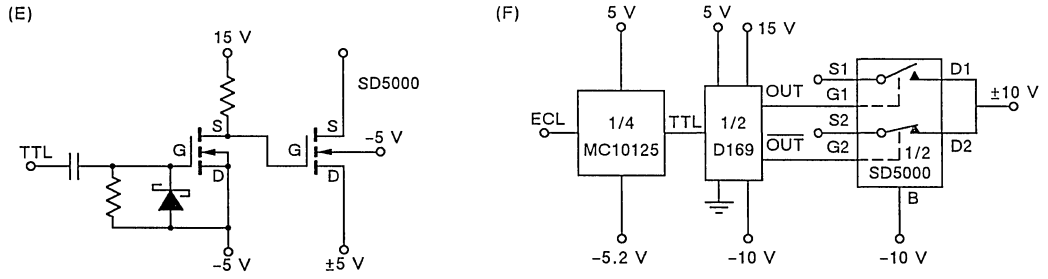


Figure 27. Various DMOS Drivers

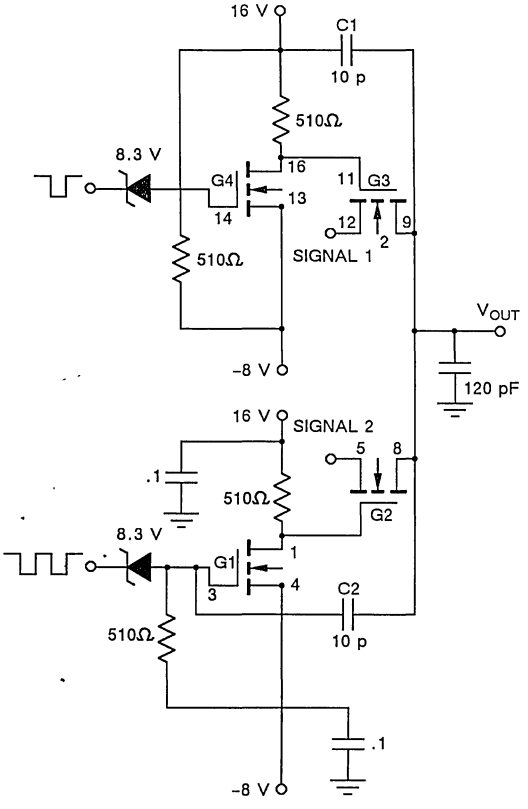


Figure 28. 5 MHz Multiplexer and Sample-and-Hold Circuit

Design Idea

In a typical application, the circuit of Figure 28 is used to multiplex, sample, and hold two analog signals at a 5-MHz rate. Two of the switches in an SD5000 are used as level shifter/drivers to provide the gate drive of the single-pole-double-throw arrangement formed by switches 3 and 4. Capacitors C1 and C2 provide charge injection compensation.

Signal 1 is a 6-V, 156 kHz square wave. Signal 2 is a 2-Vpp, 78-kHz alternating waveform with a dc offset of -3.4 V (Figure 29).

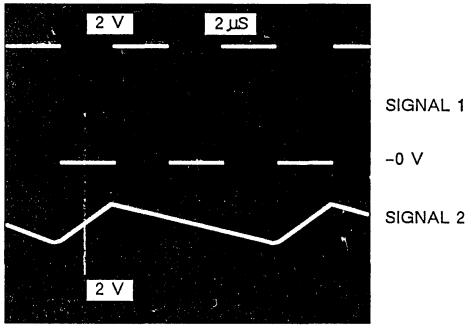


Figure 29. The Two Analog Signals to be Sampled

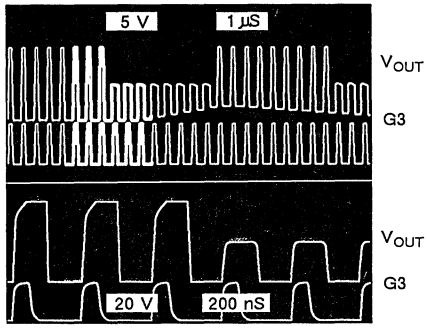


Figure 30. Composite Sample and Hold Output Along with Gate 3 Control Signal

Figure 30 illustrates the resulting composite waveform present at the holding capacitor along with the gate 3 control signal.

As can be seen, the switching times are about 15 ns, the acquisition time is 80 ns, and the holding time is about 90 ns. The total sample-and-hold cycle has taken 200 ns. Even though not maximized, this speed is faster than what any other presently available (50 ns) analog switch products can achieve.

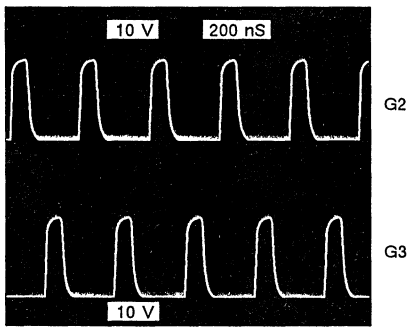


Figure 31. Gate Control Signals for the SPDT Switch Configuration

The timing and amplitude of gate 3 and gate 4 control-signals can be examined in Figure 31.

Figure 32 shows a single-pole-single-throw configuration used to select one of two AM modulated 10-MHz signals. Figure 33 illustrates the two waveforms available at the output. Table 4 contains typical values of crosstalk and off-isolation attainable with this configuration.

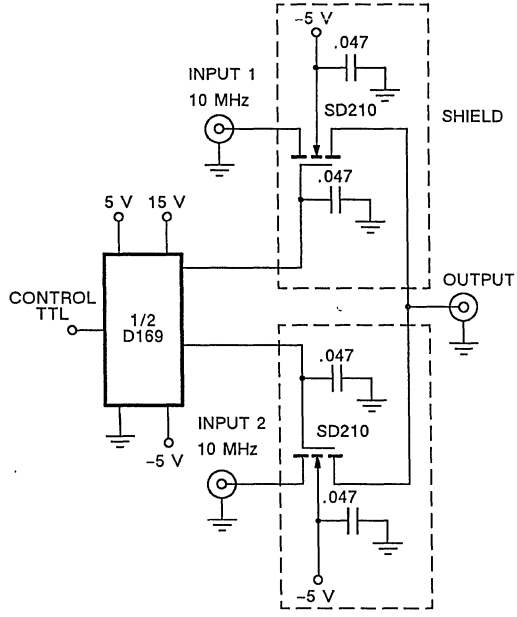
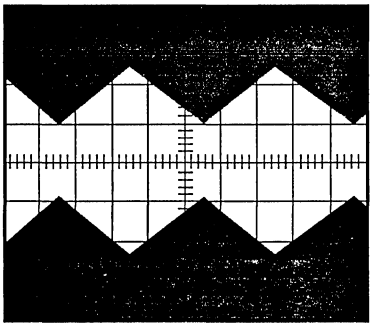


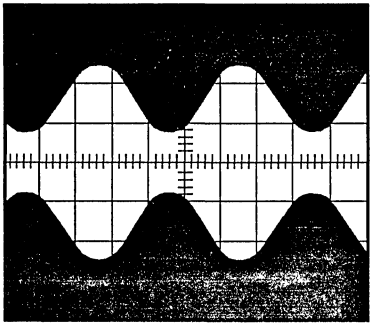
Figure 32. High Frequency SPDT Switch

Table 4 SPDT Switch Performance

FREQ (Hz)	SIG LVL (dBm)	INS LOSS (dB)	OFF ISOL (dB)	XTALK (dB)
100 k	0	1.8	80	113
1 M	0	1.8	70	92
5 M	0	1.9	69	69
10 M	0	2.0	61	65
10 M	6	2.0	61	66
10 M	12	2.0	61	66



CH1 ON



CH2 ON

SCALES– VERT: 1V/div
HOR: 20 µs/div

Figure 33. Two 10 MHz AM Modulated Outputs for the SPDT Switch of Figure 28

SUBNANOSECOND SWITCHING WITH DMOS FETS

Ed Oxner

Despite the popularity of gallium arsenide devices for high frequency applications, the silicon double-diffused MOSFET is easily capable of subnanosecond switching. This note describes limitations once attributed to high-speed DMOS switching and offers a novel driver that makes subnanosecond switching possible with Siliconix DMOS FETs.

All majority-carrier transistors have fast switching times, especially when their interelectrode (parasitic) capacitances are low. Both turn-on and turn-off times are controlled by the application or removal of gate charge. Knowing this, it seems small-signal DMOS FETs should switch off at a speed very nearly equal to turn-on. The fact is that they do, but only under the proper conditions.

Table 1. Small Signal Capacitances

	TYP (pF)	MAX (pF)
Gate Node C $_{(GS + GD + GB)}$	2.5	3.5
Drain Node C $_{(GD + DB)}$	1.1	1.5
Source Node C $_{(GS + SB)}$	3.7	5.5
Reverse Transfer C $_{DG}$	0.2	0.5

Table 1 shows capacitance characteristics for the SD210DE series from their data sheets. The characteristics of the SD211 and SD5000 are nearly identical.

The original data sheets also included the switching characteristics offered at various drain voltages (V_{DD}) and load resistances (R_L), as shown in Table 2.

The Problem

The data sheet values for t_{OFF} are much too high. If DMOS turn-off and turn-on times are essentially equal, the measured t_{OFF} can only be a circuit problem.

Before this problem can be dealt with, switching parameters must be defined. This may be done using the switching waveform shown in Figure 1 as a guide. Notice that the turn-on time parameters are measured from the input's 50% point, similar to the definition in digital circuitry. However, the turn-off time parameters are measured from the input voltage's 90% point.

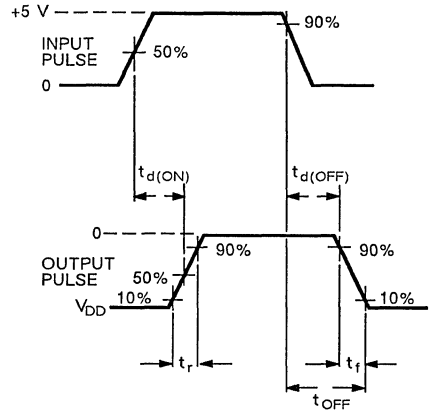


Figure 1. Typical Switching Waveform

Table 2. Switching Characteristics

V_{DD}	R_L (Ω)	$t_{d(ON)}$ (ns)	t_r (ns)	t_{OFF}[1] (ns)
5	680	0.6	0.7	9.0
10	680	0.7	0.8	9.0
15	1 K	0.9	1.0	14.0

[1] The value for t_{OFF} shown is that defined by the original data sheet.

To confirm that t_{OFF} is a circuit-related problem, use the data sheet's test circuit (see Figure 2).

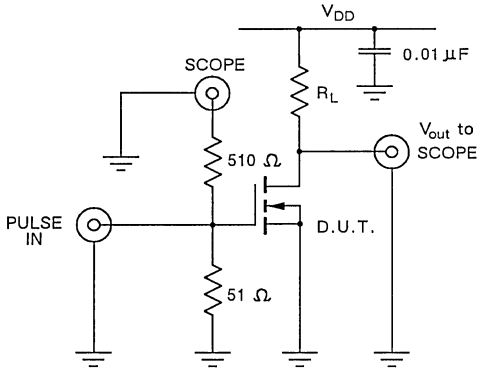


Figure 2. Switching Time Test Circuit

For V_{DD} = 10 V; R_L = 680 Ω. Let t_r for the SD210DE be ~0.8 ns and t_f for the circuit[2] be ~9.0 ns. For the external circuit, t_f is merely the difference, ~8.2 ns.

The traditional time-constant equation is

$$t = 2.2 \times R \times C \qquad (1)$$

Substituting known quantities into this equation yields

$$t = 2.2 \times 680 \times C = 8.2E\text{-}9$$

Solving for C yields C = 5.48 pF

To achieve a t_f of 8.2 ns requires approximately 5.48 pF of capacitance in the drain circuit.

First, consider stray and parasitic capacitances in the circuit layout and in the instrumentation. These can be itemized as

C stray	= 0.5 pF
C of R_L	= 1.0 pF
C scope	= 2.0 pF
	~ 3.5 pF

Add the drain-node capacitance to the total capacitance, but do not use the value from the data sheet.

Drain-node capacitance is a complex function of both the reverse transfer characteristics of the FET($-b_{21}$) and the movement of the drain-depletion region. The drain-node capacitance is best defined using

$$C_{drain\text{-}node} = C_{DG}(A_V + 1) \qquad (2)$$

where

$$A_V = g_{fs} \times R_L \qquad (3)$$

The operating drain current is calculated from ohm's law:

$$I_D = \frac{V_{DD}}{R_L} \qquad (4)$$

For values offered in Table 2, I_D = 15 mA, for V_{DD} = 10 V (with R_L= 680Ω) and V_{DD} = 15 V (with R_L= 1 kΩ).

At an I_D of 15 mA, the forward transconductance (g_{fs}) has been determined, from Figure 3, to be nominally 10.8 mS. Knowing the transconductance and load resistance, the drain-node capacitance can be calculated using Equations (2) and (3).

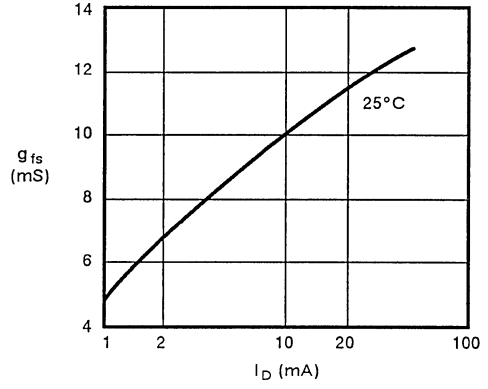


Figure 3. Effect of Drain Current on Transconductance

Using Equations (2) and (3) as described, if R_L = 680 Ω, A_V = 7.34, and if R_L = 1 kΩ, A_V = 10.8. Assume, in this case, that C_{DG} is 0.23 pF. The nominal contribution (for R_L = 680 Ω and A_V = 7.34) would be

$$C_{drain\text{-}node} = (0.23\ E\text{-}12)\ (7.34 + 1)$$

$$C_{drain\text{-}node} = 1.92 \text{ pF}$$

[2] This is the correct switching terminology. What the original data sheet identifies as t_{OFF} is really t_f.

Add this 1.92 pF to the calculated stray capacitances (3.5 pF) for a total of 5.42 pF. This agrees closely with the calculated value for drain-circuit capacitance (5.48 pF).

This analysis can now be applied to the 1-kΩ load. From Table 2, for R_L = 1 kΩ, $t_{OFF} - t_r$ = 13.0 ns.

The stray capacitances, aside from the drain-node capacitance, remain at 3.5 pF. The drain-node capacitance, as before, depends upon the reverse transfer characteristics.

To calculate the drain-node capacitance, use Equation (2), first calculating the voltage gain (A_V) using Equation (3).

For R_L = 1 kΩ and A_V = 10.8,

$$C_{drain\text{-}node} = (0.23\ E{-}12)\ (10.8 + 1)$$

$$C_{drain\text{-}node} = 2.71\ pF$$

The total drain capacitance is 3.5 pF + 2.71 pF or 6.21 pF. Use this to calculate the switching time, t_f, from Equation (1).

$$t = 2.2 \times 1000 \times 6.21\ E{-}12$$

$$t = 13.7\ ns$$

This is reasonably close to 14 ns, the value shown in Table 2.

The Solution

First, the test circuit shown in Figure 2 was modified to remove the effects of scope-probe capacitance (see Figure 4 for the modified circuit). As R_L was varied and t_f was monitored, the equivalent external capacitance was calculated using Equation (1) and the t_f scope plots (Figures 5-8). Table 3 displays the results.

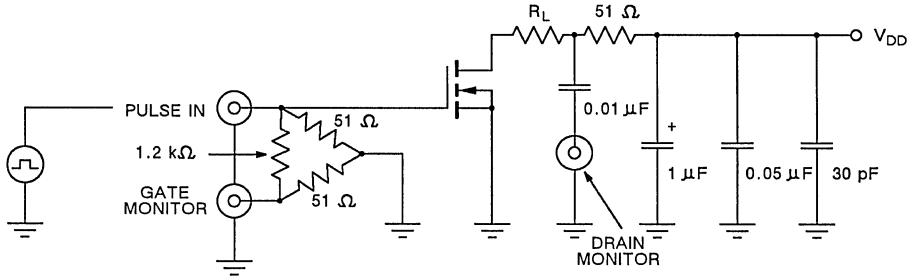


Figure 4. Switching Speed Test Monitor

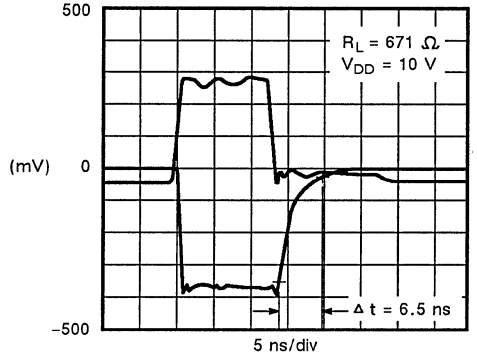


Figure 5.

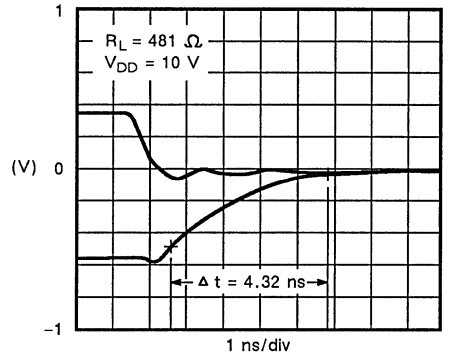


Figure 6.

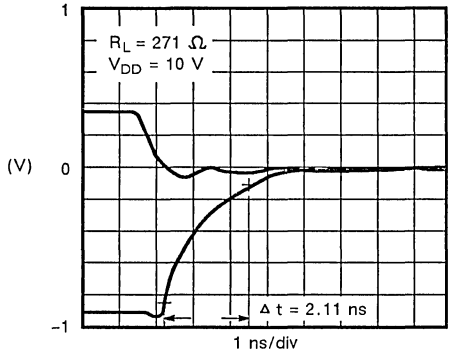


Figure 7. Fall Time for R_L = 271 Ω

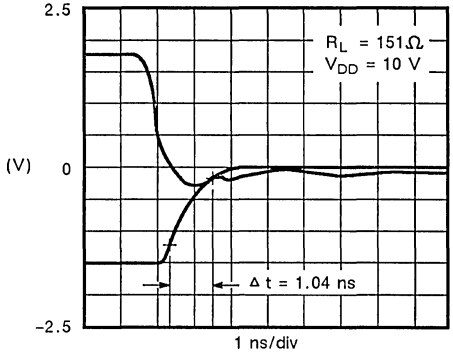


Figure 8. Fall Time for R_L = 151 Ω

Using Table 3's data, compute the capacitance using Equations (2) and (3). The results, shown in Table 4, become the new drain-node capacitance, replacing that originally offered in Table 1.

Estimating stray drain-circuit capacitance for the modified switching-speed test monitor in Figure 4 yields 2.5 pF. Add the calculated drain-node capacitance (C_{DN} from Table 4). This calculated value for total capacitance closely agrees with $C_{(equiv)}$ from Table 3; furthermore, t_f agrees remarkably well with that measured, as shown in Table 5.

Table 4.

Switching Characteristics,
Featuring New Drain-Node Capacity

V_{DD} (V)	R_L (Ω)	I_D* (mA)	g_{fs}** (mS)	C_{DN} (pF)
10	671	15	10.8	1.90
10	481	27	11.2	1.47
10	271	37	12.0	0.978
10	151	66	12.5	0.665

* pulsed drain current
** from Figure 3

Table 3.

Calculated External Equivalent Capacitance

V_{DD} (V)	R_L (Ω)	$C_{(equiv)}$ (pF)
10	671	4.4
10	481	4.0
10	271	3.54
10	151	3.13

Table 5.

Switching Characteristics,
Featuring Calculated and Measured Times

V_{DD} (V)	R_L (Ω)	C_T (pF)	t_f(calc) (ns)	t_f(meas) (ns)
10	671	4.4	6.5	6.5
10	481	3.97	4.2	4.32
10	271	3.48	2.07	2.11
10	151	3.16	1.05	1.04

These switching time data are graphed in Figure 9, extrapolated to show the switching time at a drain load of 51 Ω.

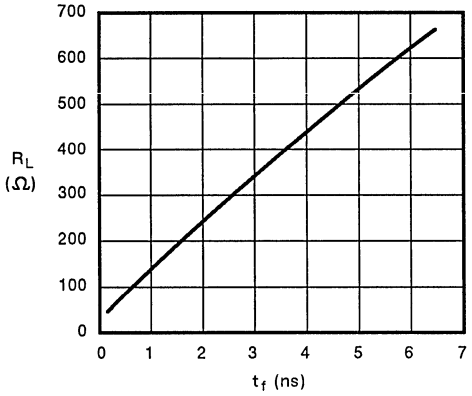


Figure 9. Fall times, Calculated and Measured

These results make it clear that turn-off is affected principally by circuit-related parameters. DMOS itself switches extremely fast, but the driver's and the circuit's effectiveness slow it down.

Driving the DMOS FET Fast

DMOS properties suggest that its devices can switch fast, and the preceding analysis confirms that they can. However, the question of how to attain these speeds remains. The answer lies in controlling the circuit parameters that surround the DMOS FET. The small-signal DMOS FET has low interelectrode capacitances. Switching involves charge transfer; the lower the value of capacity, the lower the charge transferred. For example, the current required to charge a capacitor is

$$i = C\frac{dV}{dt}$$

where

C is the capacitance in Farads
dV is the final voltage desired
dt is the switching time in seconds

Thus, to get the DMOS FET to switch fast, not only must the gate drive voltage have quick rise and fall times. but it must also have sufficient current drive to charge and discharge the gate.

Achieving a High-Speed Pulse

The step-recovery (or "snap") diode is a varactor diode with the normal ability to accumulate minority carriers during forward conduction, but with the unique ability of nearly instantaneous "snap," recovery. Under proper constraints this snap characteristic generates a very rapid, high-amplitude voltage spike. Selecting the snap-recovery diode involves two parameters: the minority carrier lifetime, which sets the lower input frequency, and the voltage breakdown of the diode, which must be sufficiently higher than the desired output pulse.

The simplest form of pulse shaping is shown in Figure 10. Capacitors C1 and C3 provide dc isolation. The snap-recovery diode (D1), in conjunction with L1, causes the rapid rise time. Current through the diode is derived from the bias supply (–V1) and R2. Figure 11 offers three views of the sequence of events that generates the fast voltage pulse. Region 1 is the charge-storage phase when the input signal current (the input of Figure 10) is zero. By virtue of the bias, the current through the diode stores charge in its junction. During this phase, the diode is a low-impedance shunt to ground. In Region 2, the input signal current is opposite in polarity and greater in magnitude than the bias current (limited by R2). This removes charge from the diode. Until all the charge is removed, the diode still appears as a low-impedance shunt. At the instant all charge is removed, the diode makes an almost instant transition (snaps) into Region 3. The abrupt cessation of signal current through L1 immediately results in a swift voltage spike. This spike becomes the leading edge of the output pulse.

R1 = 51 Ω
R2 = 510 Ω
R3 = 510 Ω
R4 = 51 Ω
C1 = 0.1 µF
C2 = 1.5 - 10 pF
C3 = 0.1 µF
L1 = 0.68 µH
D1 = HP5082-0815
D2 = HP5082-0815

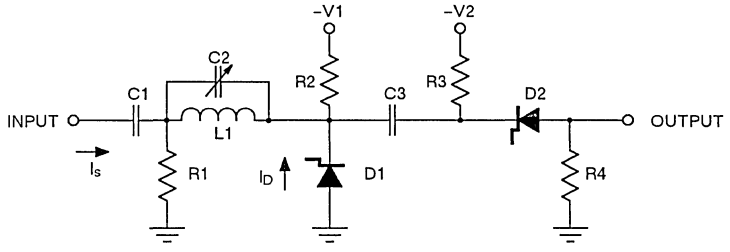


Figure 10. Nano-Second Pulser

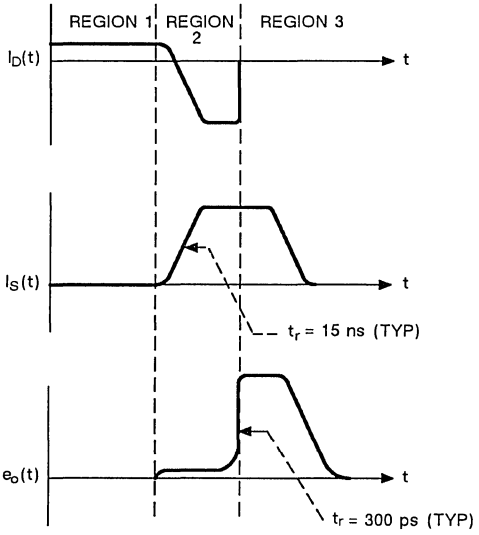


Figure 11. Rise Times of Pulse Shaping Network

Similarly, D2 sharpens the trailing edge of the output pulse. Bias (-V2) maintains D2 in conduction--a low-resistance path to the output port. The voltage pulse, having a polarity opposite to the bias current and sufficient energy to overcome it, causes D2 to snap. This abrupt transition not only sharpens the fall time but also improves the rise time.

Selecting R2 and R3 dictates the shunting of the driving signal, based on the nominal 50-Ω input impedance.

Capacitance C2, in shunt with L1, helps to improve the shape of the resulting output voltage pulse. Stray parasitic capacitances and inductances are critical aspects of any super-speed pulser. Leading-edge overshoot, shown in Figure 12, is generally attributed to series L di/dt effects, whereas rise time is often the result of shunting parasitic capacitance. Consequently, the pulser's design must maintain the characteristic impedance and must match to discrete components. For optimum performance, use leadless chip capacitors and resistors with minimal lead lengths. Likewise, the step-recovery diodes must have extremely small parasitic package inductance.

To achieve the +10-V output pulse sufficient to drive DMOS fully on, the driving signal needs to source considerable current — far more than the typical function generator can produce. A suitable driver, shown schematically in Figure 13, provides the necessary current. Impedance mismatch between the driver and the pulser required an impedance-controlling resistor in the pulser's input stage (see Figure 10).

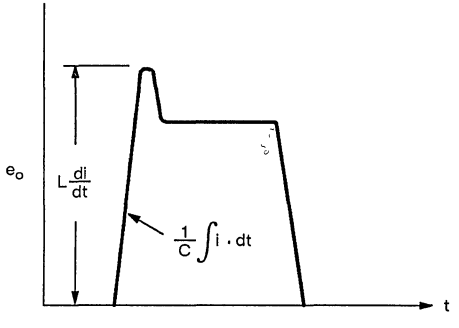


Figure 12. Effects of Parasitic Elements

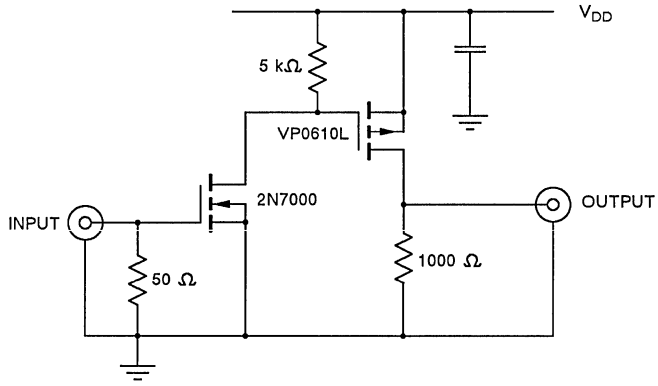


Figure 13. Driver Circuit

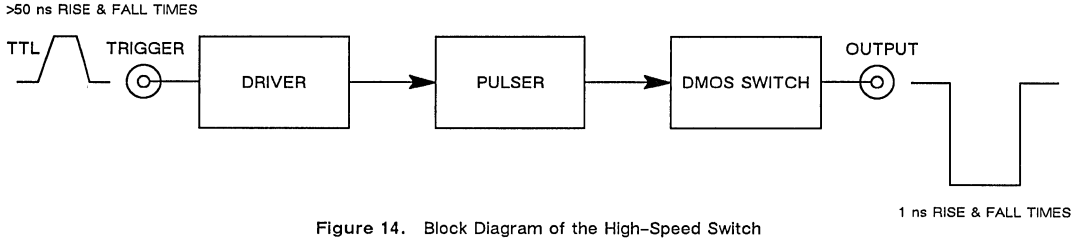


Figure 14. Block Diagram of the High-Speed Switch

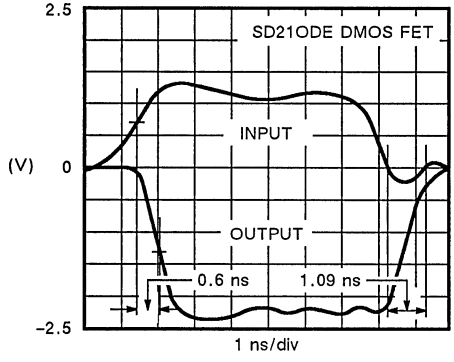


Figure 15.

Figure 14 is a block diagram of the complete high-speed switch capable of 1-ns turn-on and turn-off speeds. The transition time (between the initiating pulse that triggers the pulser and the resulting switch action) is 30 ns.

Conclusions

Figure 15 shows that fast switching action is possible. Note the positive gating pulse from the step-recovery diode pulser and the resulting switching of the DMOS FET. For a 150-Ω DMOS load resistor, the turn-off time[3] nearly matches that derived earlier (see Figure 9): 1 ns.

[3] To observe these rise and fall times requires an oscilloscope with a bandwidth of at least 500 MHz.

HIGH-SPEED DEPLETION-MODE DMOS FET FOR SMALL-SIGNAL APPLICATIONS

Alan Pritchard
July 1988

The SD2100 is an ultra high-speed n-channel depletion-mode lateral DMOS transistor geared for small-signal applications. This device boasts high-performance characteristics, produced by the Siliconix DMOS construction, which include:

- turn-on speeds of less than 1 ns
- low reverse-transfer capacitance of less than 2.5 pF
- high-frequency transconductance greater than 10 mS
- wide dynamic range
- low distortion

Figures 1 and 2 show idealized cross sections of the normally on depletion-mode and the normally off enhancement-mode devices. Because these device structures are similar, the device characteristics are also similar. In fact, the depletion-mode device may be thought of as an enhancement-mode device with a negative threshold voltage.

Unlike the enhancement-mode devices, such as the SD210DE whose drain current falls to zero when the gate-to-source voltage equals zero, the SD2100 has appreciable current at zero gate signal. In fact, the drain-to-source resistance is typically 100 Ω when V_{GS} = 0 V. As shown in Figure 3, the on-resistance ($r_{DS(on)}$) versus analog signal range is an almost flat response. This characteristic coupled with the low capacitance values of the device make the SD2100 particularly suitable as an analog switch for audio and video switching applications.

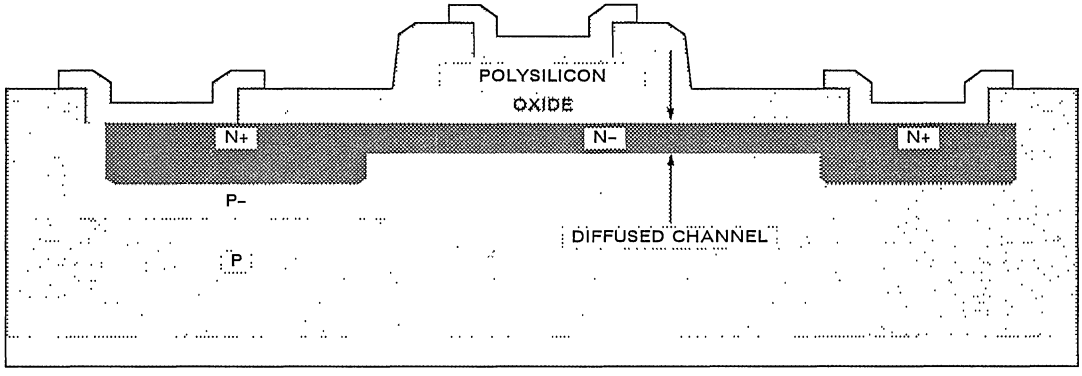


Figure 1. Depletion-Mode Device Cross Section

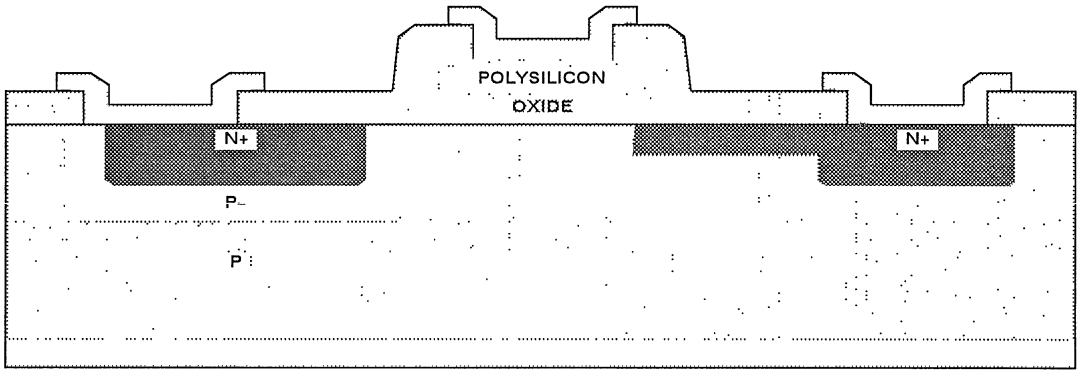


Figure 2. Enhancement-Mode Device Cross Section

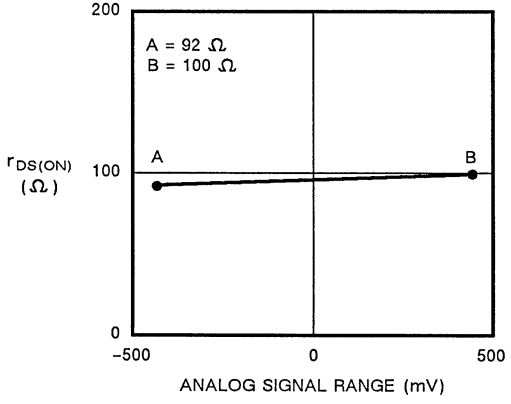


Figure 3. SD2100 On-Resistance vs. Analog Signal Range

The high-frequency gain of the device, along with its low capacitance values, produce a high figure of merit. An important factor in VHF and UHF amplification, figure of merit defines the gain bandwidth product (GBW) of the device, which may be expressed as

$$GBW = \frac{g_{fs}}{2\pi\ (C_{in} + C_{out})} \qquad (1)$$

For a common-source configured amplifier, C_{in} is the short-circuit input (Miller) capacitance

$$C_{in} = C_{gs} + C_{dg}(1 + |A_V|) \qquad (2)$$

where

C_{gs} = gate-source capacitance
C_{dg} = feedback capacitance

It is evident that the gain-bandwidth product is largely dependent on the device gain and the feedback capacitance. If typical values for the SD2100 are substituted in Equation 1, including the low feedback capacitance of 2.5 pF, the gain bandwidth product is found to be greater than 400 MHz, a useful value in VHF and UHF operation.

The high figure of merit is also reflected in the nanosecond turn-on times which allow the SD2100 to be used in applications which are normally monopolized by gallium arsenide devices. Turn-on times are important in applications such as sync-pulse generation for high-definition video systems, signal routing for high-speed digital video recording where data rates of greater than 100M bits/s are possible, and outside broadcasting systems where signal switching is required during blanking periods. Figure 4 shows a high-performance video dc restorer. In these applications, the low distortion characteristics are important.

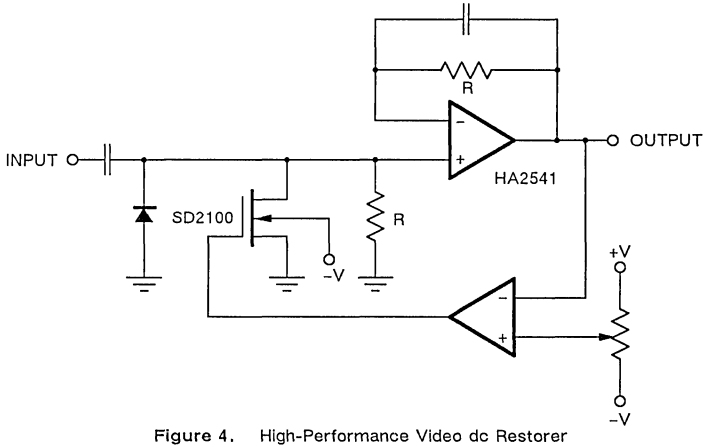


Figure 4. High-Performance Video dc Restorer

Additionally, the SD2100 is useful in applications which require both low charge injection and high switching speeds. For example, a deglitch circuit for the output of a high-speed digital-to-analog (D/A) converter, such as those found in video waveform generators, can take advantage of the SD2100's high speed, low capacitance, and low distortion.

Glitches at the D/A converter output, as shown in Figure 5, are generated during the switching transition times when time skews allow incoming and previous data to overlap. The worst-case occurrence is at MSB (most significant bit) switching (e.g., from 01111111 to 10000000).

A deglitch circuit effectively forms a sample-and-hold function which samples the output sometime after it has settled. As D/A converter performance improves, settling times approaching 10 ns have become possible; therefore, fast switching, low capacitance sample-and-hold circuits, such as the one shown in Figure 6 using the SD2100, are required.

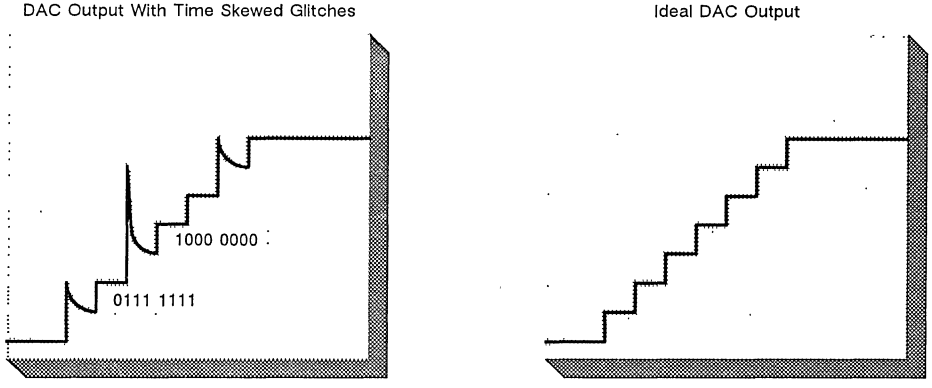
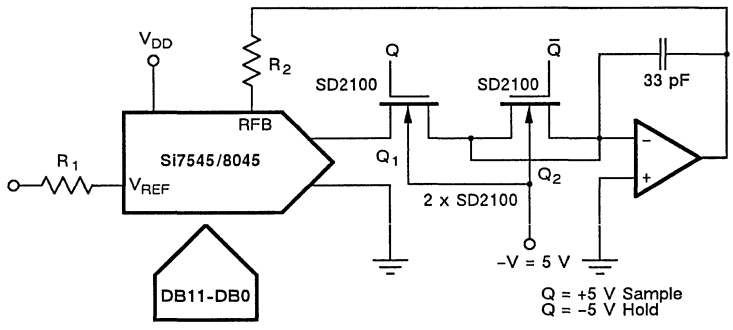


Figure 5. The Effect of Time Skew Glitches at the D/A Converter Output



Charge injection is reduced by complementary drive to Q1 and to Q2 which acts as a "dummy" capacitor.

Figure 6. Deglitched D/A Converter Using 2 x SD2100

Another advantage of the depletion-mode or normally on characteristic of this device makes the SD2100 useful for single-device current regulators. This type of circuit, usually associated with junction FETs, is shown in Figure 7. The value for R_S can be calculated from

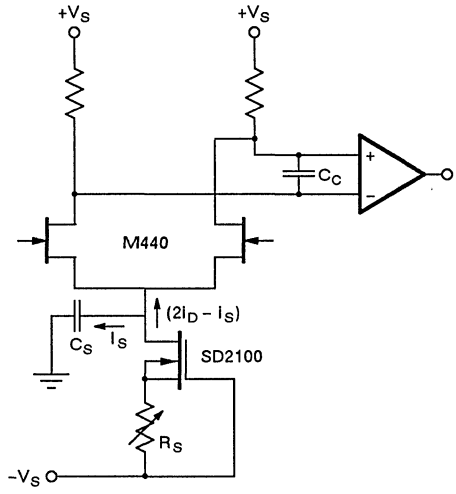
$$R_S = \frac{V_{GS(off)} \left[1 - (I_D / I_{DSS})^{1/2}\right]}{I_D} \qquad (3)$$

Where I_D is the required value of regulated current.

The major advantage of depletion-mode MOSFETs in current-source circuits is their low drain capacitance, which makes them suitable for biasing applications in low-input-leakage, medium-speed (>50 V/μs) circuits,

In general, each side of the M440 (high speed dual JFET) will be biased at I_D = 500 μA. Thus, the current available for charge compensation and stray capacitances is limited to 2 x I_D or, in this case, 1.0 mA. The M440 matching characteristics are production tested and guaranteed on the data sheet.

C_S represents output capacitance of the input stage "tail" current source. This capacitance is important in non-inverting amplifiers because the input stage undergoes considerable signal excursions in this connection, and the charging currents in C_S may be large. When using standard current sources, this tail capacitance may be responsible for marked slew-rate degradation in non-inverting applications as opposed to inverting applications where the charging currents in C_S are very small.



C_S reduces the maximum current swing available to charge C_C, thus reducing the slew rate.

Figure 7. Low Bias Current Differential Front-End

The slew-rate reduction may be shown as

$$\frac{1}{1 + (C_S / C_C)} \qquad (4)$$

As long as C_S is small compared to C_C (the compensation capacitor), little change in slew rate occurs. Using an SD2100, C_S is on the order of 2 pF. This approach yields a significant slew rate improvement.

Further applications result when currents greater than I_{DSS} (1 to 5 mA) are required. The SD2100 may be biased into the enhancement mode to produce up to 20 mA for a V_{GS} of +2.5 V maximum. Low output capacitance remains a major feature. Figure 8 shows a suitable enhancement-mode current source.

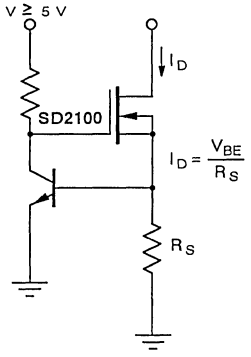


Figure 8. Enhancement-Mode Current Source

A final advantage of a normally on analog switch is that it may be constructed for applications where a default condition is required at supply failure, such as for automatic ranging of test equipment or for guaranteeing correct initialization of logic circuits at start up.

The low negative threshold voltage of the device gives simple drive requirements and allows low voltage operation. Figure 9 shows the typical bias conditions for a depletion-mode SD2100.

To turn the device off, a negative voltage is required on the gate. However, the on-resistance can be reduced if the device is further enhanced with a positive gate potential, allowing the SD2100 to be used in

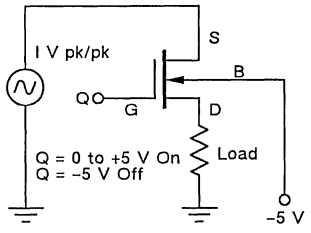


Figure 9. Normally On Analog Switch

the enhancement-mode region as well as in the depletion-mode region. This effect is shown in Figure 10.

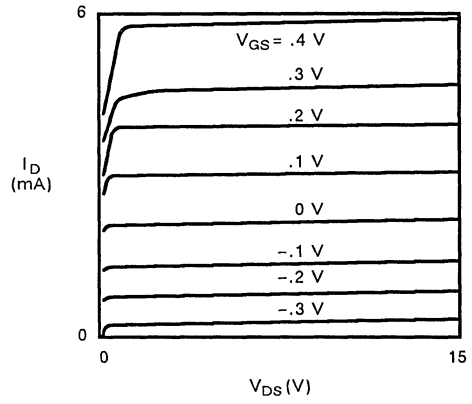


Figure 10. SD2100 Current vs. Drain-to-Source Voltage

The SD2100 is an easy-to-use, cost-effective device that is suitable for a wide range of high-speed applications. To improve the flexibility and high-frequency performance, Siliconix now offers the SST2100 which is housed in a SOT-143 surface-mount package.

Siliconix incorporated

DMOS – UNDERSTANDING THE BODY EFFECT

Ed Oxner

The body effect is a common problem with many DMOS components. To avoid the unexpected performance degradation it can cause, designers should be aware of this effect and its consequences.

DMOS, like all MOS products, and quite unlike the JFET, is a four-terminal structure. The terminals are the source, drain, gate, and the body or structure. Many MOSFETs, FETlingtons in particular, have the body electrically bridged to the source. In small-signal DMOS components, however, the body is frequently available as a separate connection.

Often, the body is simply tied to the source. While this is a perfectly acceptable solution for many applications, there are exceptions. For example, consider a Zener-gate protected DMOS, such as the SD211DE, used as an analog switch. Under no circumstances may the Zener be forward-biased; consequently, the gate must never be more negative than the body/substrate. Yet, to ensure an off condition, the gate-to-source potential must be less than the threshold voltage. If the analog signal being switched swings negative, the gate must be more negative to maintain proper control. The body must, in turn, be more negative than the gate to prevent forward-biasing of the Zener.

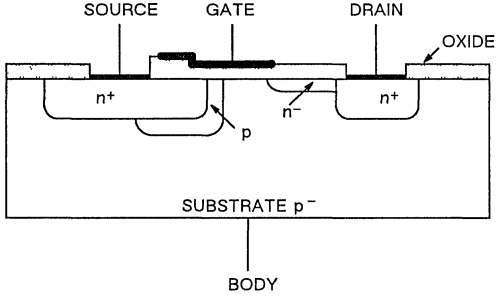


Figure 1. Cross-Sectional View of Enhancement-mode DMOS

Examine the cross-sectional view of a DMOS FET offered in Figure 1. The substrate/body of this enhancement-mode, n-channel DMOS is p-doped silicon, but a positive gate voltage inverts the p-region beneath the gate. The resulting channel, spanning the n-doped source and the n-doped drain, is bounded by oxide above and p-doped silicon below. During conduction, this n-enhanced channel bounded by the p-doped substrate resembles that of an n-channel JFET. Figure 2 offers an idealized comparison.

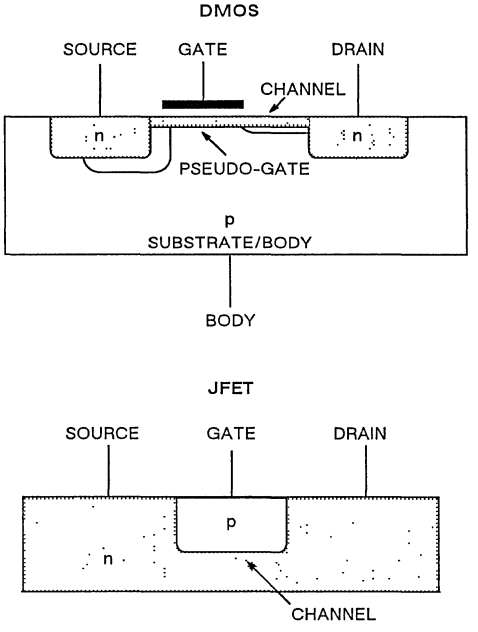


Figure 2. Comparing the DMOS Channel to the JFET Channel

Together, the n-enhanced channel and the p-doped substrate/body form a diode; the p-substrate is the anode and the inverted region is the cathode. Diode conduction occurs whenever the forward bias exceeds the barrier potential, which for a silicon p-n junction is nominally 0.55 V.

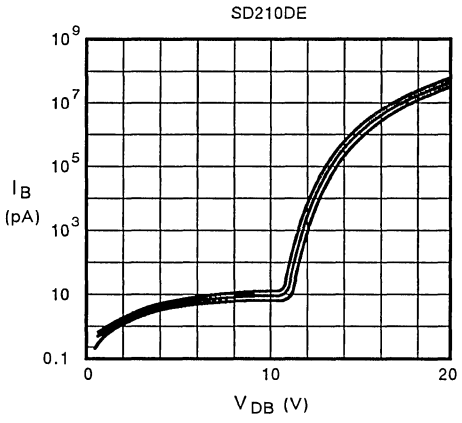


Figure 3. Leakage current vs. voltage

This channel-substrate diode is the key to the body effect. Figure 3 identifies its reverse leakage. As with any diode, some nominal leakage occurs until reverse breakdown is reached and the current rises dramatically. Especially dramatic, though, is the apparent low breakdown voltage evident in Figure 3. When the nominal drain/body potential passes 10 V, an abrupt increase in body current results: the body effect.

Returning to the analog switch scenario: If the body is biased negatively to where the drain-body voltage approaches 10 V (as per Figure 3), substantial channel-body current flow. Among other observable problems, this will strongly offset the analog voltage being switched (I_{Body} R_{Load}).

This problem is not limited to the analog switch scenario. Any application (with or without a Zener gate diode) where the drain-to-substrate potential exceeds 10 V may result in undue drain-substrate current flow.

In addition to this current flow effect, there are other body-related phenomena to be considered. Threshold voltage and on resistance both rise quite dramatically as the source-body voltage increases. For more information on these effects, see Application Note LPD-10.

In conclusion, generally a good rule of thumb is to tie the substrate/body terminal to the most negative voltage that the DMOS will experience (including the gate potential). Under no circumstances should the substrate float as carrier-induced charges will lead to threshold and on-state instabilities.

DESIGNING FET BALANCED MIXERS FOR HIGH DYNAMIC RANGE

Ed Oxner
Central Applications

SECTION 1: FETS IN SINGLE BALANCED MIXERS

INTRODUCTION

When high-performance, high-frequency junction field-effect transistors (JFETs) are used in the design of active balanced mixers, the resulting FET mixer circuit demonstrates clearly superior characteristics when compared to its popular passive counterpart employing hot-carrier diodes. Comparison of several types of mixers is made in Table I. The advantages and disadvantages of semiconductor devices currently used in various mixer circuits are shown in Table II.

Table 1

Characteristic	MIXER TYPE		
	Single-Ended	Single Balanced	Double Balanced
Bandwidth	Several decades possible	Decade	Decade
Relative 1M Density	1.0	0.5	0.25
Interport Isolation	Little	10-20 dB	>30 dB
Relative L. O. Power	0 dB	+3 dB	+6 dB

Why an Active Mixer?

Active mixing suggests high-level mixing capability. High level mixing in turn infers that active mixers outperform passive mixer circuits in terms of wide dynamic range and large-signal handling capability. Additionally, the active mixer offers improved conversion efficiency over the passive mixer, permitting relaxation of the IF amplifier gain requirements and even possible elimination of the customary RF amplifier front end.

Initial evaluation of the active FET mixer will imply a disadvantage because of local oscillator drive requirements; bipolar devices in low-level mixers require very little drive power. However, in high-level mixing this disadvantage is overcome in that drive requirements at such mixing levels are generally the same, no matter whether bipolar or FET devices are used.

Table 2

DEVICE	ADVANTAGES	DISADVANTAGES
Bipolar Transistor	Low Noise Figure High Gain Low D.C. Power	High IM Easy Overload Subject to Burnout
Diode	Low Noise Figure High Power Handling High Burn-out Level	High L. O. Drive Interface to I.F. Conversion Loss
JFET	Low Noise Figure Conversion Gain Excellent IM products Square Law Characteristic Excellent Overload High Burn-out Level	Optimum Conversion Gain Not Possible at Optimum Square Law Response High Lo Power
Dual-Gate MOS FET	Low IM Distortion AGC Squre Law Characteristic	High Noise Figure Poor Burnout Level

Why FETs for Balanced Mixers?

The performance priorities of modern communication systems have stringent requirements for wide dynamic range, suppression of intermodulation products, and the effects of cross-modulation. All of the foregoing parameters must be considered before noise figure and gain are taken into account.

Since FETs have inherent transfer characteristics approximating a square-law response, their third-order intermodulation distortion products are generally much smaller than those of bipolar transistors. Harmonic distortion and cross-modulation effects are third-order-dependent, and thus are greatly reduced when FETs are used in active balanced mixers.

A secondary advantage derives from available conversion gain, so that the FET mixer becomes simultaneously equivalent to both a demodulator and a preamplifier.

First Order Balanced Mixer Theory

Essential details of balanced mixer operation, including signal conversion and local oscillator noise rejection, are best illustrated by signal flow vector diagrams (Figure 1).

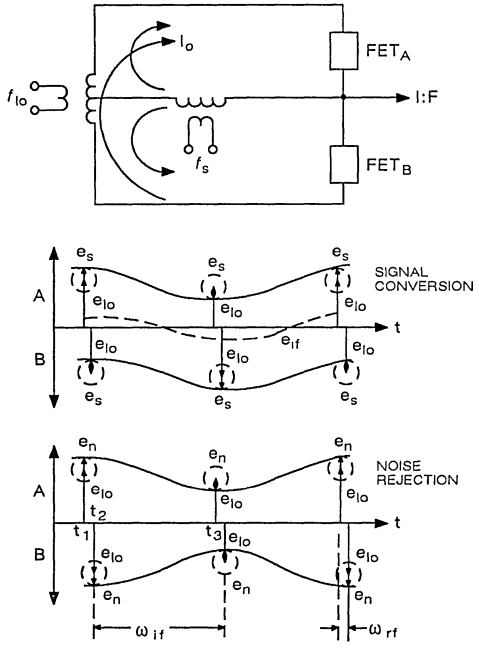


Figure 1. Signal and Noise Vectors

Energy conversion into the intermediate frequency (IF) pass-band is the major concern in mixer operation. In the following analysis, both the signal and noise vectors are shown progressing (rotating) at the IF rate (ω_{ift}); the resulting wave occurs through vector addition.

The analysis of local oscillator noise rejection (Figure 1) assumes, for simplicity of explanation, that noise is coherent. Thus at some point in time (t_1) the noise component (e_n) is "in phase" with the local oscillator vector (e_{lo}) and FET "A" (the rectifying element) is ON; the JFET mixer acts as a switch, with the local oscillator acting as the switch drive signal. One-half cycle later, at time t_2, the signal flow is reversed for both the local oscillator vector and the noise component, FET "A" is OFF and FET "B" is ON. Moving ahead an additional one-half of the IF cycle, FET "A" is again ON, but the noise component has advanced 180° (ω_{ift}) through the coupling structure, and is now "out of phase". The process continually repeats itself.

The end result of this averaging (detection) is the cancellation of the noise which originated in the local oscillator, providing that the mixer balance is precise [1].

The analysis of the conversion of the signal to the IF pass-band is similar, but the signal is injected into the coupling structure at the equipotential tap. Thus at time t_2, the signal vector (e_s) is "out of phase" with the local oscillator vector, e_{lo}. The resulting envelope develops a cyclic progression at the IF rate, since the signal is "demodulated" by the mixing action of the FETs.

A schematic of a prototype balanced mixer is shown in Figure 2. Design criteria, in order of priority, include the following:

1. Intermodulation and Cross-Modulation
2. Conversion Gain
3. Noise Figure
4. Selecting the Proper FET
5. Local Oscillator Injection
6. Designing the Input Transformer
7. Designing the IF Network

Intermodulation and Cross-Modulation

A basic aim in mixer design is to avoid the effects of intermodulation product distortion and cross-modulation. Part of the problem may be resolved by using a balanced mixer circuit.

The active transfer function of the FET is represented by a voltage-controlled current source. For both cross-modulation and intermodulation, the amount of distortion is proportional to the amplitude of the gate-source voltage. Since input power is proportional to input voltage, and inversely proportional to input impedance, the best FET IM and cross-modulation performance is obtained in the common-gate configuration where the impedance is lowest [2].

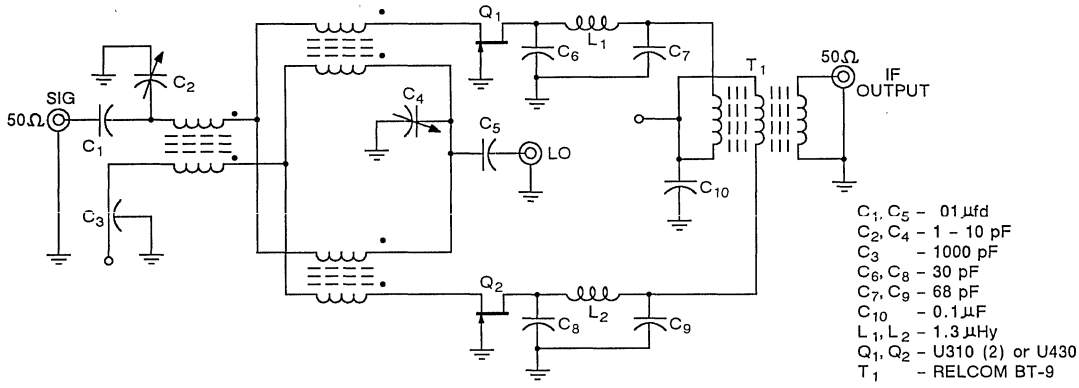


Figure 2. Prototype Active Balanced Mixer

When JFETs are used as active mixer elements, it is important that the devices be operated in their square-law region. Operation in the FET square-law region will occur with the device in the depletion mode. Considerable distortion will result if the FET is operated in the enhancement mode (positive, for an n-channel FET); by analogy, the problems encountered are similar to those which arise when positive drive is placed on the grid of a vacuum tube.

Square-law region operation emphasizes the importance of establishing proper drive levels for both quiescent bias and the local oscillator. The maximum conversion transconductance, g_c, is achieved at about 80% of the FET gate cutoff voltage, $V_{GS(off)}$, and amounts to about 25% of the forward transconductance, g_{fs}, of the FET when used as an amplifier. Since conversion gain (or loss) must be considered, it is common to equate voltage gain A_V, as:

$$A_V = g_c R_L \qquad (1)$$

where g_c is the conversion transconductance and R_L is the FET drain load.

An attempt to achieve maximum conversion gain by indiscriminately increasing the drain load resistance will adversely affect any design priority concerning distortion - particularly intermodulation product distortion.

Distortion takes different forms in mixers. Most obvious is that distortion which will occur if the FET is driven into the enhancement mode, as noted earlier. A more pernicious form is drain load distortion. And finally, there is the so-called "varactor effect."

The most frequent cause of poor mixer performance stems from signal overloading in the drain circuit. Excessive drain load impedance degrades the intermodulation characteristics and produces unwanted cross-modulation signals[3]. A characteristic of the FET balanced mixer is that the correct drain load impedance is inversely proportional to the value of the conversion transconductance. Figure 3 shows the improvement in the IM characteristics obtained in the prototype mixer with the drain load impedance reduced to 1700 Ω from 5000 Ω. Specifically, the dynamic load line must be plotted so that the signal peaks of the instantaneous peak-to-peak output voltage are not permitted to enter into the non-saturated ("triode") region of the FET. Suitable and unsuitable drain load lines are shown in Figure 4. Load impedance selection is quantified in Equations 21 through 23.

Distortion from the "varactor effect" is of secondary importance, and arises from an excessive peak voltage signal swing, where the changing drain-to-source voltage can cause a change in parasitic capacitance, C_{rss}, and give rise to harmonics[4]. A FET tends to be voltage-dependent when the drain voltage falls appreciable below 6 volts. If the source voltage (from the power supply) is also low and the drain load impedance in high, then distortion will develop. However, if proper steps are taken to prevent drain load distortion, the varactor effect will also be inhibited.

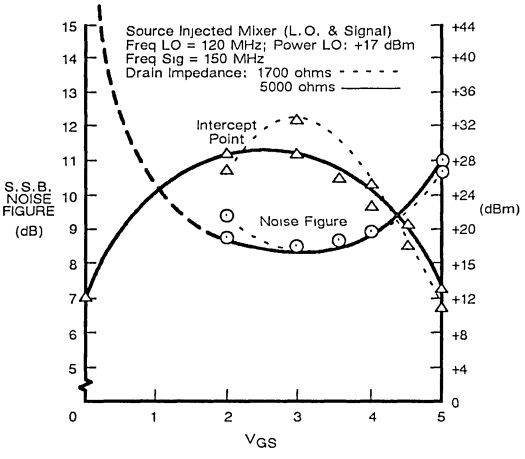


Figure 3. Comparison of Mixer IM Characteristics

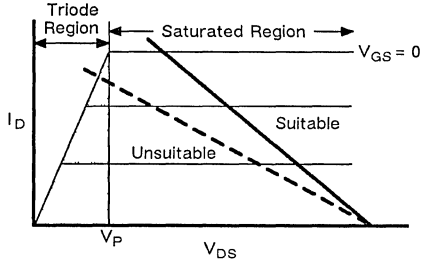


Figure 4. Plotting Drain Load Lines

Conversion Gain

In a FET, forward transconductance is defined as

$$g_{fs} = \frac{dI_D}{dV_{gs}} \qquad (2)$$

and conversion transconductance is defined as

$$g_c = \frac{dI_D(\omega i)}{dV_{gs}(\omega r)} \qquad (3)$$

where ωi = the intermediate frequency and ωr = the signal frequency.

The effects of time-varying local oscillator voltage, V_2, and the much smaller signal voltage, V_1, must be considered:

$$V_{gs} = V_1 \cos\omega_1 t + V_2 \cos\omega_2 t \qquad (4)$$

For square law operation

$$V_2 + V_{GS} \leq V_{GS(off)} \qquad (5)$$

Drain current is approximately defined by

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2 \qquad (6)$$

or

$$I_D \approx \frac{g_{fso}V_{GS(off)}}{2}\left[1 - \frac{V_{gs}}{V_{GS(off)}}\right]^2 \qquad (7)$$

or

$$I_D \approx \frac{g_{fso}}{2\,V_{GS(off)}}\left[V_{GS(off)} - V_{gs}\right]^2 \qquad (8)$$

then

$$I_D \approx \frac{g_{fso}}{2\,V_{GS(off)}} \text{ (complex Taylor expansion)} \qquad (9)$$

which can be reduced

$$I_{D(IF)} \approx \frac{g_{fso}}{2\,V_{GS(off)}} V_1 V_2 \cos(\omega_1 - \omega_2)\,t \qquad (10)$$

and the conversion transductance is

$$g_c = \frac{g_{fso}}{2\,V_{GS(off)}} |V_2| \qquad (11)$$

Equation 11 suggests that g_c increases without limit as V_2 increases without limit. However, to avoid operation of the FET in the "triode" region, the peak-to-peak swing of V_2 should not exceed $V_{GS(off)}$.

Thus

$$2\,V_2 \text{ peak} \leq V_{GS(off)} \qquad (12)$$

or

$$V_2 \text{ peak} \leq \frac{V_{GS(off)}}{2} \qquad (13)$$

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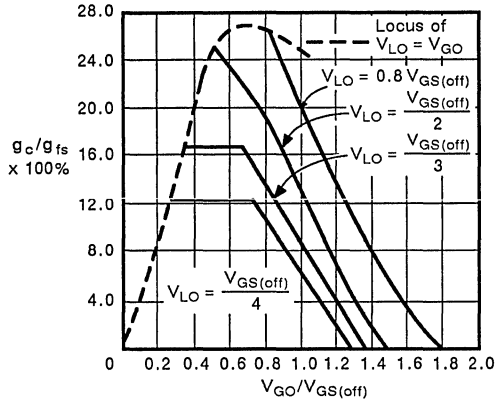

Figure 5. Normalized g_c/g_f vs. $V_{GS}/V_{GS(off)}$ (from "FET RF Mixer Design Technique", S.P. Kwok, WESCON Convention Record (1970) 8/1, p.2.) Used with Permission

Figure 5 shows plots of normalized conversion transconductance, g_c/g_{fs} versus normalized quiescent bias, $V_{GS}/V_{GS(off)}$, for different oscillator injections.

Noise Figure

Like the common-gate FET amplifier, the common-gate FET balanced mixer is sensitive to generator resistance, R_g [5]. A change of a decade in R_g can produce a noise figure variation of as much as 3 dB.

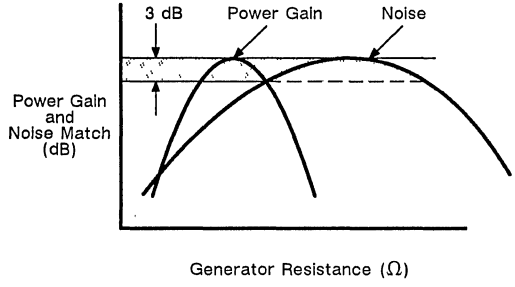

Figure 6. Power Gain and Noise Matching

In the design of the prototype FET active balanced mixer, the generator resistance of the FETs is established by the hybrid coupling transformer. Two important criteria for the FETs in the circuit are high forward transconductance, and a value of power-match source admittance, g_{lgs}, which closely matches the output admittance of the coupling transformer. In the common-gate configuration, match points for optimum power gain and noise do not occur at the same value of generator resistance (Figure 6). Optimum noise match can only be achieved at the sacrifice of bandwidth.

How to Select the Proper FET

Conversion efficiency is determined by conversion transconductance, g_c, which in turn is directly related to such FET parameters are zero-bias saturation current, I_{DSS}, and the gate cutoff voltage, $V_{GS(off)}$):

$$g_c = \frac{I_{DSS}}{2\,V_{GS(off)}^2}\,|V_2| \qquad (14)$$

$$\approx \frac{g_{fso}}{2\,V_{GS(off)}}\,|V_2| \qquad (15)$$

Equation 14 appears to indicate that FETs with high I_{DSS} are to be preferred. However, I_{DSS} and $V_{GS(off)}$ are related, and Figures 7a and 7b show that devices from a family selected for high I_{DSS} do not provide high conversion transconductance, but actually produce a lower value of g_c.

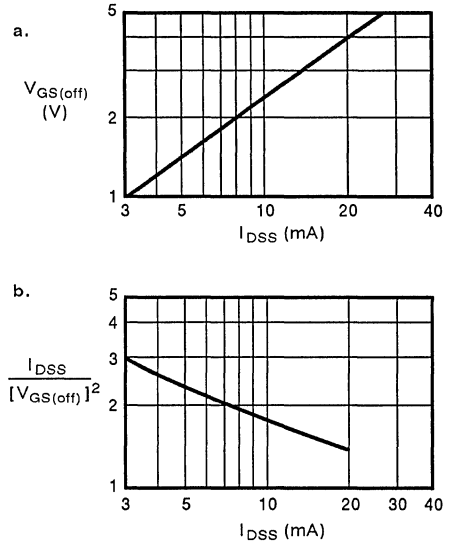

Figure 7. Relationship of I_{DSS} and $V_{GS(off)}$

Best mixer performance is achieved with "matched pairs" of JFETs. Basic considerations in selecting FETs for this application are gate cutoff voltage, $V_{GS(off)}$, for good conversion transconductance, and zero-bias saturation current, I_{DSS}, for dynamic range. A match to 10% is generally adequate. Among currently available devices, the Siliconix U310 and the dual U431 offer excellent performance in both categories; common-gate forward transconductance is 14,000 mmhos typical at V_{DS} = 10 V, I_D = 10 mA, and f = 1 kHz.

Criteria for FET Selection

In balanced mixers using FETs, conversion efficiency of the devices is determined by conversion transconductance, g_c, which in turn is directly related to such FET operating parameters as zero-bias drain current, I_{DSS}, and gate cutoff voltage, $V_{GS(off)}$.

It can be shown that

$$\frac{I_{DSS}}{2\ V_{GS(off)}^2}\ |V_2| \approx \frac{g_{fso}}{2\ V_{GS(off)}}\ |V_2| \qquad (16)$$

where V_2 is the time-varying local oscillator voltage. To maintain operation in the square-law region, we repeat Equation 13,

$$V_2\ (\text{peak}) \leq \frac{V_{GS(off)}}{2} \qquad (17)$$

where now, under optimum performance conditions, we merge Equation 11 with Equation 13 to find

$$g_c \approx \frac{g_{fso}}{2\ V_{GS(off)}}\ \frac{V_{GS(off)}}{2} = \frac{g_{fso}}{4} \qquad (18)$$

which agrees with Equation 15.

For the highest level of conversion transconductance, it would appear initially that for any given FET geometry, units with high I_{DSS} are to be preferred. But as we saw in Figure 7, since I_{DSS} and $V_{GS(off)}$ are related, a performance tradeoff is necessary; however, an increased value of I_{DSS} provides increased dynamic range. Since balanced mixer design involves many tradeoffs for best performance, this I_{DSS} vs. $V_{GS(off)}$ problem is generally inconsequential.

There is, of course, the possibility that FET cost is a major consideration in evaluating the active balanced mixer approach - the familiar price/performance tradeoff. If this is the case, there are a number of other Siliconix FETs which will provide suitable alternatives to the U310 (Table 3). Remember, however, that conversion transconductance, g_c, can never be more than 25% of forward transconductance. Thus as tradeoff considerations begin, the first sacrifice to be made will be the degree of achievable conversion gain. Intermodulation performance will follow with the third tradeoff being available noise figure.

Table 3

Typical Characteristics	DEVICE TYPE			
	U310*	2N5912	2N4416*	2N3823
g_m	15 K	6 K	5 K	3.5 K
I_{DSS}	40 mA	15 mA	10 m	10 mA

*Similiar products are available in TO-92:
U310 (J310)
2N4416 (2N5486)

Local Oscillator Injection

Low IM distortion products and noise figure, plus best conversion gain, will be achieved if the voltage swing of the local oscillator across the gate-to-source junction is held to the values presented in Figure 5. V_{LO} is expressed in terms of peak-to-peak voltage, while $V_{GS(off)}$ is a d.c. voltage.

Local oscillator injection can be made either through a brute-force drive into the JFET source through the hybrid input transformer, or through a direct-coupled circuit to the JFET gates where less drive will be required for the desired voltage swing. Two circuits to obtain direct gate coupling are suggested in Figure 8.

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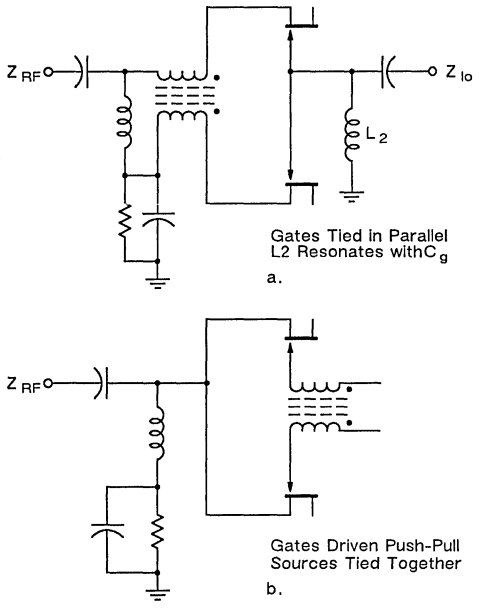


Figure 8. Alternate Forms of L.O. Injection

The source-injection method is used in the design of the present mixer to maintain the inherent stability of a common-gate circuit. A minor disadvantage with the direct-drive method is that the required gate-to-source voltage swing requires considerable local oscillator input power. For source injection through the transformer, best mixer performance is obtained with a local oscillator drive level of +12 to +17 dBm across a 50-Ω load.

Conversely, direct coupling to the FET gates occurs at a higher impedance level and less local oscillator drive power is required. The functional tradeoff resulting when the gates are tied together is that shunt susceptance requires some form of conjugate matching, and thus brings about an undesirable reduction of instantaneous mixer bandwidth.

Designing the Input Transformer

Five criteria are important to the design of the hybrid input coupling transformer for best mixer performance. The impedance transformer must

1. Consist of four single-ended terminals, for the local oscillator, the input signal and FETs A and B
2. Offer a match between either input to a symmetrical balanced load
3. Provide as much isolation as possible between the signal and local oscillator ports (Figure 9)
4. Maintain a differential phase of 180° across the symmetrical balanced loads
5. Introduce the least possible amount of loss

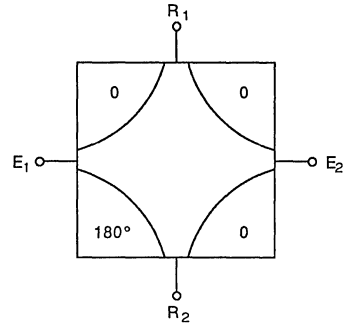


Figure 9. 4-Port Hybrid with Phase and Isolation

A transformer using ferrite cores and meeting these five requirements is derived from elementary transmission-line theory (Figure 10). Transmission line transformers have a low-frequency cutoff determined by the falloff of primary reactance as frequency is decreased. This reactance is determined by the series inductance of the transmission line conductors. On the other hand, high-frequency performance is enhanced by minimizing the physical length of the transmission line. Minimizing overall line length while maintaining suitable reactance can be accomplished by using a high-permeability core material such as a ferrite. The transformer constructed for the balanced FET mixer closely resembles the balanced 4-port unsymmetrical 180° hybrid device described by Ruthroff [6].

Although Ruthroff does not discuss the method of determining the winding length of bifilar wire, a solution is offered by Pitzalis[7]. The Pitzalis definitions for wire length are as follows (Figure 11):

$$\text{max length} = \frac{7200n}{f_{upper}} \text{ (inches)} \qquad (19)$$

$$\text{min length} = \frac{20R_L}{(1 + \mu/\mu_O)\, f_{lower}} \text{ (inches)} \qquad (20)$$

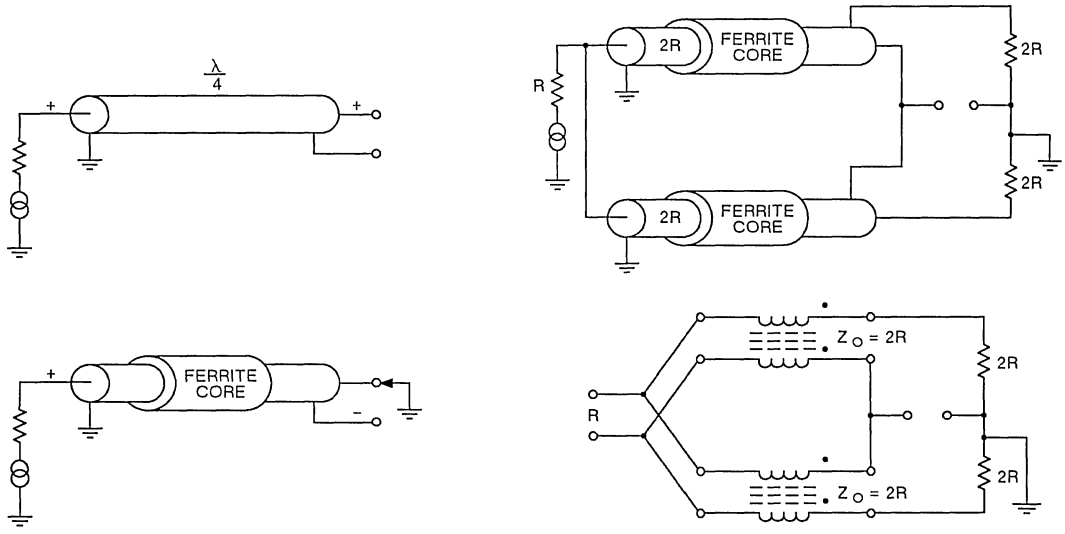


Figure 10. Hybrid Input Coupling Transformer

where R_L = the load impedance, $\mu/\mu o$ = the relative permeability of the ferrite at the lower frequency, and n = a fractional wavelength determined by the amount of allowable phase error.

Selection of the ferrite core material is determined mainly by performance requirements. A prime consideration for wideband performance is the temperature coefficient of the ferrite, which must have a low loss tangent over the required temperature range, i.e., high Q.

In addition, an important design factor involves the relative permeability of the core, since inductance of a conductor is proportional to the permeability of the surrounding medium. A high permeability material placed close to the transmission line conductors acts upon the external fringe field present, appreciably magnifying the inductance and providing a lower cutoff frequency. Power transferred from input to output is coupled directly through the dielectric medium separating the transmission line conductors; thus a relatively small cross-section of ferrite material can operate in an unsaturated state at impressively high power levels. For the FET balanced mixer, ferrite core material with a permeability of 40 provides satisfactory operation from 50 to 250 MHz. Figure 11 also demonstrates that a lower transmission line impedance, Z_O, is to be preferred over a higher Z_O. Both 50-Ω and 100-Ω transmission lines are required for the mixer transformer; twisted pairs will provide satisfactory results. A characteristic impedance of 45 Ω is obtained from 3 turns-per-inch of Belden No. 24 AWG enamel wire, while $3^1/_2$ turns-per-inch of No. 24 (7X32) Belden plastic covered wire provide Z_O = 100 Ω. Each core is wound with 2 inches of proper twisted pair, with min/max lengths calculated from Pitzalis' data (Formulae 19,20).

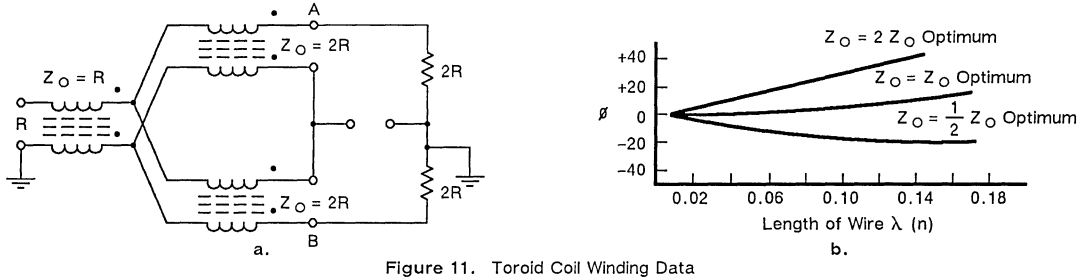


Figure 11. Toroid Coil Winding Data

As with all broadband transformers, the coil has an inherent parasitic inductance which must be capacitor-compensated (C_2, C_4, Figure 2). A trim capacitor is required at the two input terminals, and is adjusted *only once* to optimize the differential phase shift across the symmetrical balanced FETs. Phase match of the hybrid structure may be tracked to within ±2 degrees (about 180°) to 250 MHz. Effective resistance transformation is useful from 50 to 550 MHz (Figure 12) – but phase track beyond 250 MHz *may* show too much deterioration.

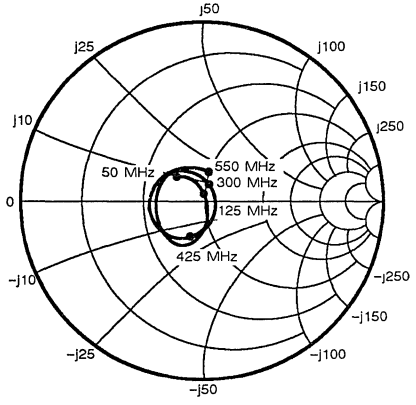


Figure 12. 50 Ω – 200 Ω Balun

Designing the IF Network for Single-Balanced Mixers

The IF network performs two important functions in the FET balanced mixer circuit. It provides for optimum match between the FETs and the IF amplifier, and it effectively bypasses the circuit RF components (signal and local oscillator).

In network design, it is essential that the RF and local oscillator signals be sufficiently isolated from the intermediate frequency signal to maintain rejection levels of at least 20 dB. If this isolation is not maintained, conversion gain and noise figure are degraded.

The simplest technique for design of the IF network is to use the well-known pi (π) match structure from each FET drain to a common balanced output transformer network. This pi match technique is especially suitable for a narrow-band intermediate frequency output, serving three useful functions. First, it serves to achieve the proper drain load match between the FETs and the IF structure. Second, it provides the very necessary isolation of the intermediate frequency signal. And third, it serves as a simple filter to provide a monotonic decrease in impedance as frequency departs from the IF center frequency, f_o[8]. This third function, shown in Figure 13, prevents the drain load impedance from skyrocketing out of control and giving rise to distortion products.

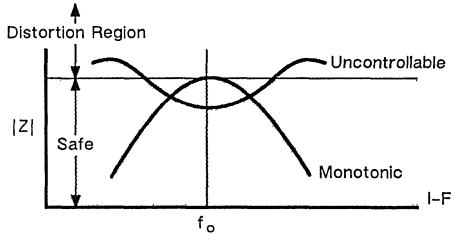


Figure 13. Pi (π) Match Filter Function

Selection of the dynamic drain impedance value in the IF network is a critical point in design of the structure. Intermodulation product distortion and cross-modulation will be both affected by the instantaneous peak-to-peak output voltage of the FETs, if the value of the dynamic drain impedance allows these signal peaks to enter either the pinch-off voltage or breakdown voltage regions of the transistors. If the impedance is too high, the dynamic range of the mixer will be severely limited; if the impedance is too low, useful conversion gain will be sacrificed.

A first-order approximation to establish the proper load impedance may be obtained when

$$R_L = \frac{V_{DD} - 2V_{GS(off)}}{i_d} \tag{21}$$

where

$$i_d = I_{DSS}\left[1 - \frac{V_{gs}}{V_{GS(off)}}\right]^2 \tag{22}$$

and

$$V_{gs} = V_{GS} + V_1 \sin \omega_1 t \tag{23}$$

For the U310 FET, the optimum drainload impedance is established at slightly less than 2000 Ω, with sufficient local oscillator drive and gate bias determined from the conversion transconductance curve in Figure 5.

The output IF coupling structure is an 800-Ω CT to 50-Ω trifilar-wound transformer (Relcom BT-9 or equivalent). The pi (π) match into this transformer provided a dynamic drain load impedance of 1700 Ω on each FET; excellent IM performance was obtained. Value of operating Q was established at 10 as the best compromise to insure that the tolerance of the pi match components would permit the IF output to peak within the allowable bandwidth at the associated IF amplifier. A Q of more than 10 would result in a greatly restricted bandwidth, while a Q of less than 10 would result in excessively high capacitance, excessively low inductance, and unsatisfactory filter performance.

Single-Balanced Mixer Performance

Tests of the operational prototype FET single-balanced mixer demonstrated that the active mixer has several characteristics superior to those of passive mixer counterparts. These comparisons are made in Table 4 (measurements of all three mixers were made under laboratory conditions).

Insertion loss measurements on the IF network amounted to 3 dB in the center of the passband, while insertion loss on the hybrid assembly measured 1.2 dB. The network exhibited a Q of 10. Gain and noise figures were measured over the full 50-250 MHz bandwidth, with a single-sideband noise figure ranging from 7.2 dB at 50 MHz to 8.6 dB at 250 MHz. Conversion gain was a flat +2.5 dB.

Two-tone third-order intermodulation is expressed in terms of the intercept point[9]. With two signals 300 kHz apart, the balanced mixer suppressed third-order products −89 dB with both signals at −10 dB, representing an intercept point of +32 dBm.

Table 4

50-150 MHz Mixer Performance Comparison

Characteristic	JFET	Schottky	Bipolar
Intermodulation Intercept Point	+32 dB	+28 dBm	+12 dBm†
Dynamic Range	100 dB	100 dB	80 dB†
Desensitization Level (the level for an unwanted signal when the desired signal first experiences compression)	+8.5 dBm	+3 dBm	+1 dBm†
Conversion Gain	+2.5 dB*	−6 dB	+18 dB
Single-sideband Noise Figure @ 50 MHz	7.2 dB	6.5 dB	6.0 dB

* Conservative minimum † Estimated

Figure 14 shows a comparison of third-order IM products emanating from both the JFET balanced mixer and a typical low-level double-balanced diode mixer, under similar operating conditions. Noise figure and intercept point are shown at various bias and local oscillator drive levels in Figure 15.

The performance of the active mixer is clearly superior to that of the diode mixers, contributing overall system gain in areas critical to telecommunications practice, and reducing associated amplifier requirements.

CONCLUSION

The reason for using the three-core bifilar transformer (Figure 11A) in this tutorial article stemmed

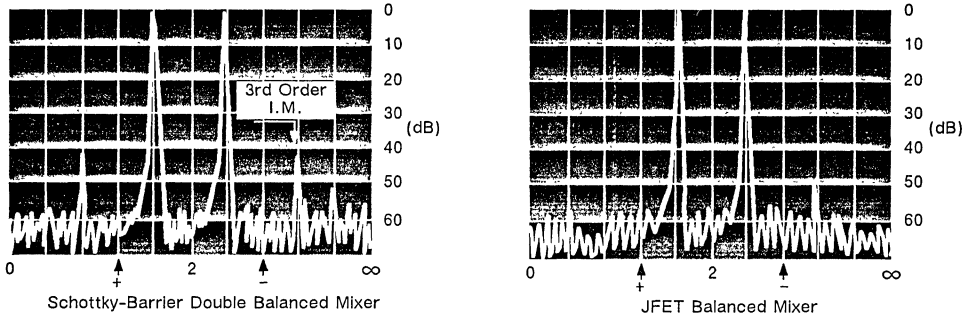


Figure 14. Comparison of 3rd Order IM Products

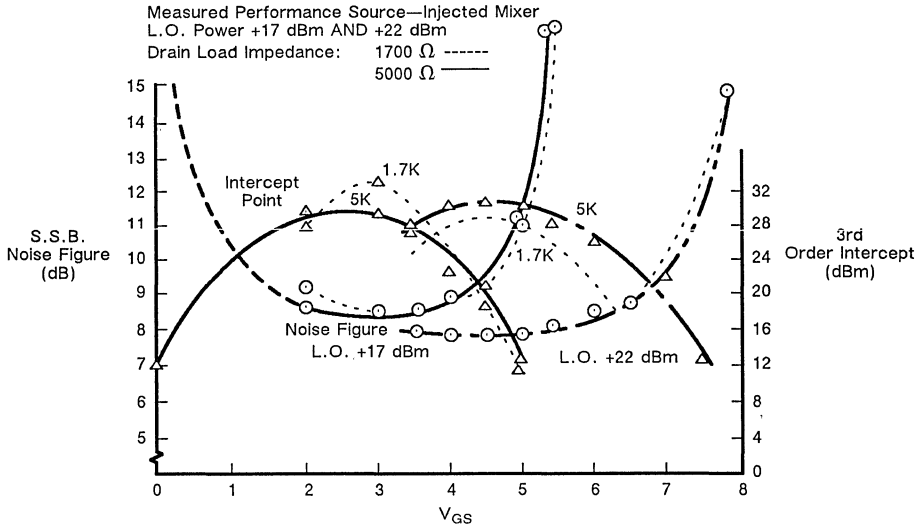


Figure 15. Noise Figure and Intercept Point Performance Single-Balanced Mixer

from the relative analytical simplicity of such a design. An alternative transformer is the single-core trifilar-wound design. The definitions for wire lengths (Equations 19 and 20) are equally applicable to trifilar as they are for bifilar.

SECTION 2: JUNCTION FETS IN DOUBLE-BALANCED MIXERS

INTRODUCTION

Dynamic range is probably the most important consideration in modern receiver design. Table 1 provides a comparison between the harmonic distortion characteristics of a simple mixer, a single-balanced mixer, and a double-balanced mixer. The comparison clearly shows those performance characteristics of the double-balanced mixer which have made it one of the most popular of all mixer types. Among these attributes are greatly improved interport isolation and a significant degree of rejection of local oscillator carrier amplitude modulation.

When used in double-balanced mixers, however, passive devices such as Schottky-barrier (hot carrier) diodes have certain fundamental shortcomings, such as high conversion loss and high local oscillator drive requirements. Thus the active balanced mixer which employs field-effect transistors is a welcome innovation: conversion gain and improved intermodulation distortion characteristics alone place the FET double-balanced mixer far ahead of its passive counterparts. The high saturation levels possible with modest local oscillator power make such a mixer useful for mixing both small and large signals.

First Order Double-Balanced Mixer Theory

In either single or double-balanced mixer design, the prime requirement is that when the mixer is excited by the local oscillator carrier, the circuit must be capable of rejecting the amplitude-modulated wave which exists about the L.O. Also, the mixer must reject any AM signal entering from the local oscillator port. (This signal rejection is usually known as AM local oscillator noise cancellation).

A second requirement for balanced mixers is the establishment of interport isolation between the signal, local oscillator, and IF ports. A third desirable characteristic is the reduction of intermodulation distortion products.

Careful attention to design of double-balanced mixers will satisfy the foregoing criteria.

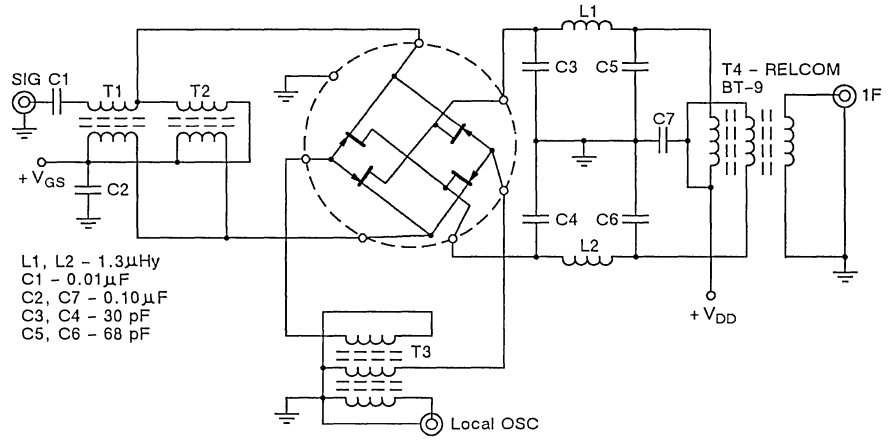


Figure 16. Double-Balanced Mixer

The schematic of a prototype double-balanced mixer (Figure 16) employs four high-performance junction FETs chosen for closely matched characteristics. (The significance of the quad-FET configuration will be dealt with later).

If the schematic in Figure 16 is reduced to show only the local oscillator circuit (Figure 17a), the rejection mechanism of AM signals, either on the L.O. carrier on entering through the local oscillator port, is readily understood.

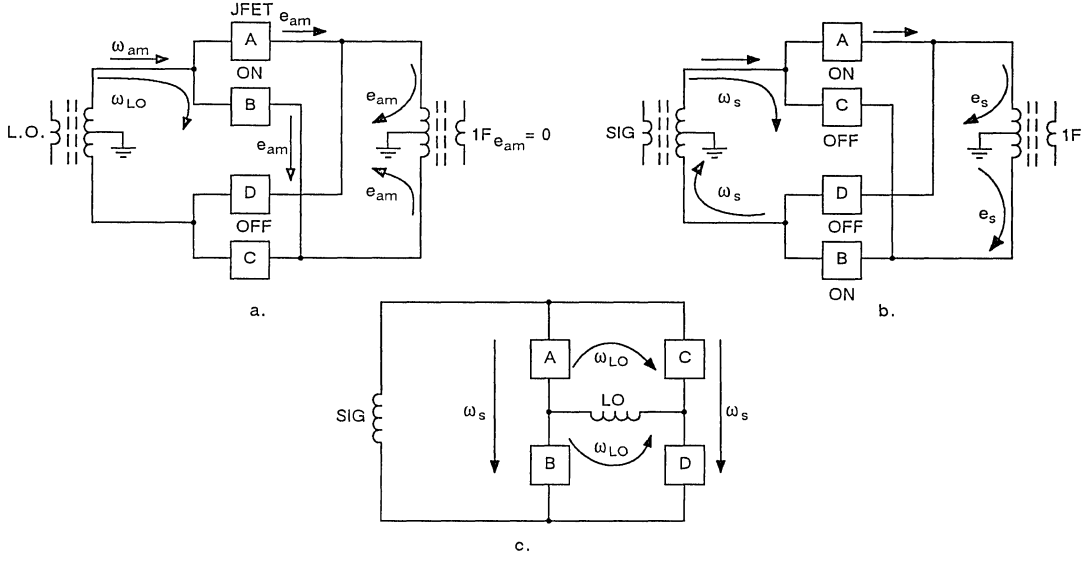


Figure 17.

Likewise, the equivalent circuit in Figure 17b demonstrates how the signal is enhanced at the IF output. Both local oscillator AM cancellation, as well as signal enhancement, are dependent upon the precise balance of the IF transformer, as well as on the match of the four FETs which make up the quad network. In Figure 17c, the schematic has been rearranged to show both the local oscillator and the signal input transformers; the mechanics of interport isolation may be easily visualized. Signal excitation provides an equipotential at the junctions of the local oscillator transformer and FET pairs AB and CD; in the same manner, excitation of the local oscillator produced an equipotential balance at the junctions of the signal transformer and FET pairs AC and BD.

Harmonic distortion products are reduced by the balance between the signal and local oscillator (inputs) and the IF (output), where even-integer harmonics of the signal and local oscillator frequencies are effectively canceled. A sixth-order summary of such products in both single- and double-balanced mixers is shown in Table 5. Note how the relative densities agree with Table 1. The effects of harmonic distortion can be reduced by a judicious selection of the IF passband response[10]. Third-order IMD (Intermodulation Distortion) products are reduced by virtue of the characteristics of junction FETs, which approximate a square-law response. Care must be taken in FET operation, however, to avoid driving the device into forward conduction by the application of too much local oscillator power.

Table 5

Comparison of Modulation Products in Single and Dougle Balanced Mixers to 6th Order	
Single-Balanced	**Double-Balanced**
f_s	
$3f_s$	
$5f_s$	
$f_o \pm f_s$	$f_o \pm f_s$
$f_o \pm 3f_s$	$f_o \pm 3f_s$
$f_o \pm 5f_s$	$f_o \pm 5f_s$
$2f_o \pm f_s$	
$2f_o \pm 3f_s$	
$3f_o \pm f_s$	$3f_o \pm f_s$
$3f_o \pm 3f_s$	$3f_o \pm 3f_s$
$4f_o \pm f_s$	
$5f_o \pm f_s$	$5f_o \pm f_s$

Harmonic Distortion, Intermodulation Products, and Cross-Modulation

Spurious output signals in mixers fall into three categories:

1. Spurious mixer products derived from harmonic mixing of the signal and local oscillator frequencies;
2. Two-tone, odd-order intermodulation products;
3. "Chirping" which arises from undesired mixing frequencies falling in the IF passband.

The harmonics of a single-signal frequency, when mixed with the harmonics of the local oscillator, produce spurious outputs which are level-dependent on the signal amplitude. These products are greatly reduced by the double-balanced mixer, where the even harmonics are effectively canceled; when FETs are used, the Taylor-series power expansion falls quickly to zero above the second order.

However, modulation products of a similar nature will arise if the broadband down-converting mixer is not preceded by signal preselection, because of the mixer's equal response to the "image" frequency. Here, perfectly valid signals will mix with the local oscillator producing interfering i-f signals whose only difference, when compared to the desired i-f signal, is that it moves counter to the desired i-f signal when the local oscillator is shifted.

Two-tone, odd-order IM products differ markedly from other spurious signals. This form of harmonic distortion consists of interactions between two or more input signals and their respective harmonics. In turn, these products are mixed with the fundamental and harmonics of the local oscillator, generating spurious products which may fall within the IF passband, on or very near to the desired signal.

Cross-modulation in the active JFET balanced mixer does not pose a serious problem, provided the signal input is maintained at a high conductance, which will occur with source injection. Cross-modulation is very dependent on and directly related to the impedance across which the signal is impressed. In the active JFET double-balanced mixer this impedance is very low, typical 35 Ω. Consequently, the effects of cross-modulation may be disregarded.

In the mixing process of any active device, the value of the FET drain current may be derived from a knowledge of the transconductance of the device, and the impressed signal voltage, e_g. This is obtained from the Taylor-series power expansion:

$$i_d = g_m e_g + \frac{1}{2!}\frac{\delta g_m}{\delta V_G} e_g^2 + \frac{1}{3!}\frac{\delta^2 g_m}{\delta V_G^2} e_g^3 \ldots \frac{1}{n!}\frac{\delta^{n-1} g_m}{\delta V_G^{n-1}} e_g^n \quad (24)$$

which can be reduced to the terms in Table 6.

Table 6

Term	Output	Transfer Characteristic
$g_m e_g$	F1, F2	Linear
$\frac{1}{2!}\frac{\delta g_m}{\delta V_G} e_g^2$	2 F1, 2 F2 F1 ± F2	Second-order Square-law
$\frac{1}{3!}\frac{\delta g_m}{\delta V_G^2} e_g^3$	3 F1, 3 F2 2 F1 ± F2 2 F2 ± F1	Third order

In FET theory, the second and higher-order derivatives of g_m are absent, and the device thus offers a considerable reduction of both intermodulation products and higher-order harmonics. In the double-balanced mixer, where F1 = F2 is the desired result, it is well to manipulate mixer design and bias conditions to render $\frac{\delta g_m}{\delta V_G}$ as large as possible, simultaneously reducing all other terms.

Criteria for FET Selection

For best performance in the single-balanced mixer, matched FET pairs were used. A 10% match in gate cutoff voltage, $V_{GS(off)}$, saturated drain current, I_{DSS}, and forward transconductance was sufficient; a wide selection of junction FET pairs is available for single-balanced mixer applications. However, in a double-balanced mixer using a ring-style (quad) demodulator, the match must be extended to four discrete devices. Although high forward transconductance remains desirable, the selection of FETs becomes sharply limited for most users.

Early in the development of the prototype double-balanced mixer, evaluation was made of the potential effect of physical FET packaging on mixer performance. Four selected discrete JFETs were arranged in a matrix which was electrically and schematically identical to the circuit shown in Figure 16. At the same time, four FET chips were mounted in a TO-116 dual in-line package, with the lead bonds arranged to form the ring demodulator. Comparison of the two quad-FET configurations at operating frequencies through 100 MHz indicated that the single-package arrangement had definitely superior characteristics. Physical assembly into the mixer circuit is easier, and less PC board space is required. Improved performance was noted on the following parameters:

- Lower lead inductance
- Lower distributed capacitance
- Better isolation
- Better rejection of AM noise

All of the mixer performance achievements discussed in this presentation have been made with the single-package quad-FET matrix; it behooves the user to follow this design philosophy, and to limit JFET candidates for selection to those high-performance (high transconductance, low capacitance) devices which are available packaged as matched ring-quad demodulators.

The FET chips used in the single-package configuration were Siliconix U310s, which offer saturated drain current, I_{DSS}, of 20 to 60 mA, and a typical forward transconductance of 14 mmho at $V_{GS} = 0$. Parasitic chip capacitance averages about 4 pF (C_{iss}), which allows for operation well into the UHF region. Table 7 shows the performance match achieved when adjacent chips were selected from the same wafer.

Table 7

Quad-FET Chip Matching			
Quad S/N	$V_{GS(off)}$ (V)	I_{DSS} (ma)	g_{fs} (m℧)
04720	3.39	29.2	13.1
	3.54	31.0	12.8
	3.53	30.8	13.0
	3.43	29.4	13.1
04724	3.78	35.6	12.8
	3.74	35.3	12.6
	3.84	35.7	12.7
	3.83	37.2	12.6
04728	5.23	53.4	11.6
	5.14	53.3	11.7
	5.03	51.1	11.5
	5.19	53.3	11.8

All of the quad arrays shown were tested in the mixer assembly, and all provided a maximum dynamic unbalance of only 0.17 dB, ample proof that the practice of adjacent chip selection is valid for close matching.

The pin assignments of four JFETs in the 14-pin TO-116 dual in-line carrier were arranged to avoid crossovers and maintain sufficient separation between the signal and local oscillator ports to keep stray coupling leakage to a minimum. Siliconix offers the U350, a quad-ring demodulator consisting of matched U310 JFETs.

Local Oscillator Injection

Local oscillator drive for active FET mixers, either balanced or unbalanced, differs from the drive characteristics of passive diode mixers. For best IMD performance, the gate of the FET must never be driven positive with respect to the source - - a case equivalent to the hard ON condition of the diode. Consequently, local oscillator drive for the balanced mixer is less than that required for a passive balanced mixer with comparable performance characteristics.

The double-balanced mixer relies on balanced drive from both the local oscillator and the signal source. Since conversion efficiency, optimum noise figure, and good cross-modulation effects can best be served with the signal entering through the common quad JFET source, the local oscillator excitation may be applied directly at the gates of the FET array.

A balanced trifilar-wound toroidal-coil broadband transformer, exhibiting high even-mode rejection, provides the balanced drive for the local oscillator excitation of the quad FET gates. The gates of the quad array have very low conductance; hence there will be some degree of mismatch to the local oscillator, which normally could not be tolerated for the signal port. The high gate impedance, however, allows a moderate level of local oscillator power to bring about the necessary gate voltage swing.

Transformer Design

The design problems encountered in a single-balanced mixer are compounded in the double-balanced mixer: the full-wave JFET quad differs markedly from the half-wave single-balance JFET pair, in that the quad is represented as a 4-terminal input structure, while the JFET pair is represented as a 2-terminal structure. Consequently, the double-balanced mixer transformer design requires two separate solutions, each offering entirely different structures. While each transformer design will be treated separately, it is important to note the design goals which are common to both.

The transformers must:

1. Consist of three single-ended terminal pairs, an input and a balanced output;
2. Offer a broadband match between the unbalanced input and a symmetrical balanced load;
3. Maintain (over a wide bandwidth) a differential phase of 180° across the symmetrical balanced loads; and
4. Introduce a minimum of insertion loss.

Signal Input Transformer Design

In general, design and fabrication of broadband transformers has been limited to the popular ferrite-core varieties derived from transmission-line theory[11], where exceptional bandwidths are possible. The more popular transformer designs frequently result in a 4:1 impedance transformation, as in the single-balanced mixer or in most trifilar designs. Other popular transformers offer either simple constant-impedance phase inversion or unbalanced-to-balanced configurations.

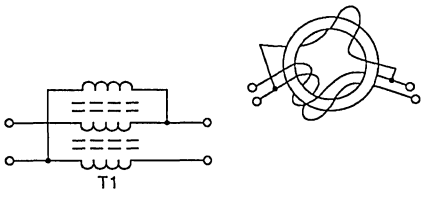


Figure 18. Signal Input Transformer

The JFET quad signal input terminals consists of shunt pairs of JFET source terminals which offer a combined load impedance of about 35 Ω as contrasted to a 100 Ω impedance value which would have suited a 4:1 transformer. It was thus necessary to design a broadband unbalanced-to-split-balance transformer which produced, in effect, a 50 Ω asymmetrical input to a 25-0-25 Ω output.

Such a transformer would require an unbalanced 50 Ω input and a symmetrically-balanced output having near-perfect 180° phase differential and an equipotential, (even-mode) center tap. Consequetly, a two-step design procedure was indicated.

The first step was to design a transformer which would provide the unbalanced-to-balanced transition while maintaining a constant impedance of 50 Ω and a 180° phase differential across the balanced output, over a 50-250 MHz band. The design was straightforward, and is shown schematically in Figure 18. The extra winding was required to complete the necessary magnetization current path.

Design of the core windings required selection of the proper ferrite, and establishment of the actual winding length. The latter was resolved to a first-order approximation by the formulas of Pitzalis (Equations 19 and 20).

Having established the approximate length limits, the final solution came by experiment. A Hewlett-Packard 8405A vector voltmeter was invaluable during this phase of the work.

According to Ruthroff the simple balun, to which the signal input transformer can be most readily compared, is equivalent to "an ideal reversing transformer plus a length of transmission line. If the characteristic impedance of the line is equal to the terminating impedance, the transformer is inherently broadband." The true equivalent of the simple Ruthroff balun is shown in Figure 19, where the "length of transmission line" is in effect a shunt element of characteristic admittance, Y_S. If $Y_O = Y_{In} = Y_A$, then it can be shown that $Y_S = Y_A$, thus providing a flat admittance transfer through the transformer[12]. Construction of the "ideal reversing transformer" required three turns-per-inch of Belden #24 enamel wire for a characteristic admittance of 0.22 $\mho$.

Core permeability was established by selection from three possible choices of Indiana General ferrite (Q1 for a permeability, μ/μ_O of 125; Q2 for $\mu/\mu_O = 40$; and Q3 for $\mu/\mu_O = 16$). Figure 20a provides a performance comparison between identically-wound transformers with different core permeabilities; Figure 20b shows the effects of winding length on the selected core, Q2. (Core material Q3 might have offered a better permeability, but its cost was prohibitive). A winding length of 1.5 inches was used for this first-stage transformer design. An identical length of single conductor was wound about the core in the

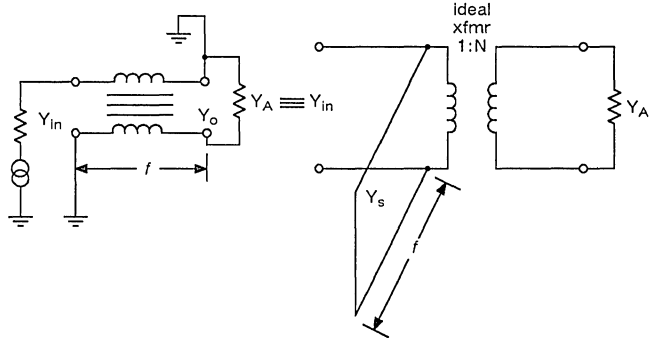
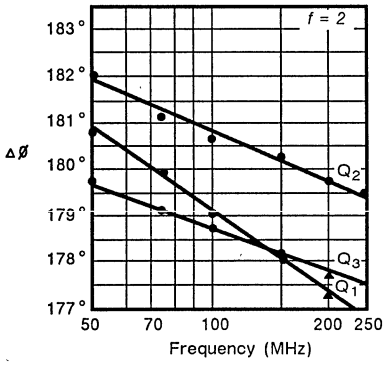
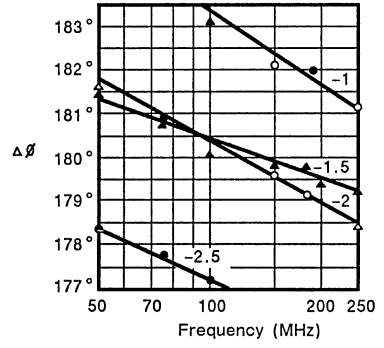


Figure 19. Equivalence of Simple Balun



a.



b.

Figure 20. Differences in Core Permeability

same winding direction for the magnetization requirements.

The second phase of the signal input transformer design is to provide a circuit that maintains the precise impedance and phase balance of the reversing transformer, while offering in combination a center-tapped junction with high even-mode rejection. The transformer was wound after the fashion of Ruthroff's 4:1 ratio impedance design, with 2 inches of twisted pair wire on a Q2 core. The resulting transformer, in combination with the reversing transformer discussed earlier, provided the degree of phase balance shown in Figure 21.

The center tap is typically decoupled in excess of 50 dB. The completed signal input transformer is shown in Figure 22. If the design offers the assurance

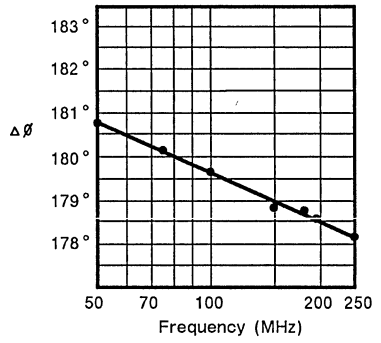


Figure 21. Input Transformer Phase Balance

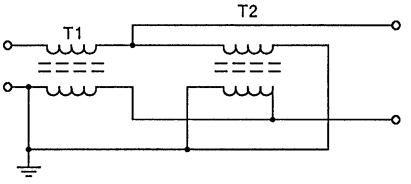


Figure 22. Completed Signal Input Transformer

that the center tap will be grounded, then the magnetization winding may be omitted.

Local Oscillator Input Transformer

Design of the local oscillator transformer is somewhat simpler than that of the signal input transformer, because two design rules may be relaxed. First, the gates operate at a higher impedance than that imposed on the sources; thus it is only necessary to insure that the peak-to-peak voltage swing at the gates is sufficient for proper FET operation. Second, close impedance match is not so critical as in the signal input transformer, since the local oscillator excitation is generally derived directly from a nearby source.

In those situations where the existence of a mismatched load is bothersome (as in high-frequency operation, where a long coaxial feed will tend to exhibit a "long lines effect" and produce erratic mixer performance) a simple precaution will avoid the problem. If the FET gates are clamped with fixed noninductive resistors (value approximately 200 Ω) to ground, such loading of the LO transformer secondary will insure a reasonable input match.

In the design shown in Figure 23, a simple trifilar-wound toroidal-core transformer produced excellent results. The transformer was constructed from three strands of Belden #24 enamel wire, twisted to 3 turns per inch. The trifilar winding, 2 inches long, was wrapped around an Indiana General F625-9 (CF102) Q2 toroidal core. Care must be taken when winding multifilar transformers with heavy wire, to insure that the wire is wrapped tightly around the ferrite for good even-mode isolation and balance.

Simplicity of design of the combined transformers made detailed analysis of performance unnecessary; indicators such as isolation and dynamic unbalance are sufficient to show symmetry for both transformers and the FET quad.

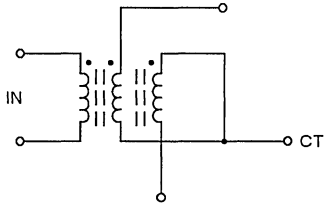


Figure 23. Local Oscillator Input Transformer

(For the prototype mixer feasibility study, relatively large ferrite cores were used, as a matter of winding convenience. The practice of using large cores, however, can lead to excessive transformer losses, resulting in degraded mixer efficiency, high noise figures, high LO drive requirements and reduced gain. For best results, cores no larger than those commonly used in the CATV industry should be chosen).

AM Local Oscillator Noise Rejection

Originally, balanced mixers were used for the specific purpose of canceling spurious AM signals existing on or about the local oscillator carrier (the function of the mixer in establishing good inter-port isolation was a side-effect). These signals could be either spurious AM signals generated on or about the carrier (Figure 24) or actual signals existing at the signal frequency. In the latter case, the signals enter the mixer through the local oscillator, having found their way in through some leakage coupling phenomenon.

Regardless of the type or source of AM signals entering through the local oscillator port, the balanced mixer should effectively reject these signals so that

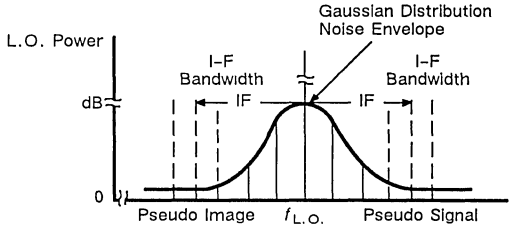


Figure 24. Generation of Spurious AM Signals

their products do not occur at the intermediate frequency. In the early days of balanced mixers, a 20 dB rejection of AM noise was considered good; today's sophisticated techniques for selection of dynamically-matched semiconductors can provide ultimate AM rejection in excess of 30 dB. Figure 25 provides an insight into the degree of AM noise rejection available in the double-balanced mixer.

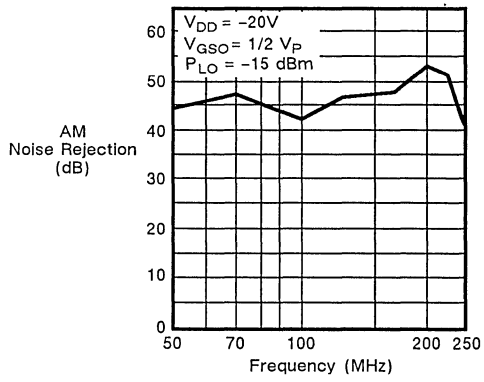


Figure 25. AM Noise Rejection in Double-Balance Mixer

(Insofar as FM noise is concerned, it should be noted that no mixer is capable of rejecting frequency-modulated signals entering through the local oscillator).

An interesting point not generally considered in discussions of balanced mixers is that the dynamic range of the mixer can be limited by the conversion of local oscillator *noise* into the intermediate frequency, which tends to blank out a weak signal and place a bottom on sensitivity.

Interport Isolation

Like AM noise rejection and dynamic unbalance, interport isolation is very dependent on mixer balance (symmetry). Matching aspects of the JFET quad array and the phase/amplitude balance of the signal input and local oscillator input transformers play important roles in achieving interport isolation. Capacitive and magnetic coupling between the transformers add to problems of interport isolation in balanced mixers.

(In the prototype mixer, the JFET quad was packaged in a 14-pin dual in-line housing, as a matter of construction convenience.) The U350 is recommended for double-balanced mixer designs.

Interport isolation was also enhanced in the prototype mixer through careful parts layout. As a measure of the overall effects of unbalance, a quantitative measurement of interport isolation vs dynamic unbalance is made in Figure 26.

In Figure 27, the interport isolation between the local oscillator and signal input ports is shown to be 35 dB typically.

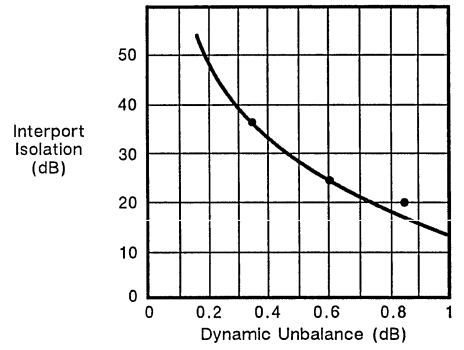


Figure 26. AM Noise Rejection in Double-Balance Mixer

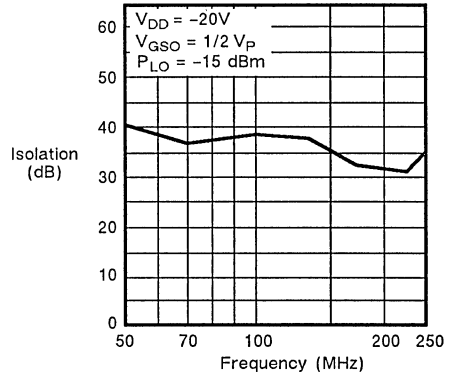


Figure 27. Interport Isolation

Dynamic Unbalance

Dynamic unbalance may be regarded as another expression for AM noise rejection, except that the latter does not provide a ready insight into the effects of symmetry, balance, and quad matching.

Dynamic unbalance also affects the intermodulation distortion performance of the mixer. As the unbalance approaches a degree of true balance, the IMD tends to optimize; conversely, when unbalance is excessive the IMD approaches an asymptotic state. This effect is shown in Figure 28.

Designing the IF Network

The IF network performs three important functions in the FET double-balanced mixer. As with the single-balanced mixer, it provides for best match between the quad FETs and the intermediate frequency amplifier; it effectively bypasses the RF components (signal and local oscillator); and unique to the double-balanced mixer, it provides a reduction of simple harmonic distortion, by virtue of its balance.

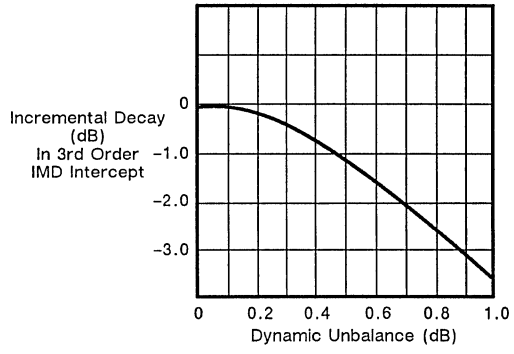


Figure 28. Dynamic Unbalance vs. Incremental Decay

Selection of the dynamic drain impedance value in the IF network is a critical point in the design of the structure. Both IM product distortion and cross-modulation will be affected by the instantaneous peak-to-peak voltage of the FETs if the dynamic drain impedance allows the signal peaks to enter either the pinchoff or breakdown voltage regions of the transistors. Here another design tradeoff must be considered. If the impedance is too high, the dynamic range of the mixer will be limited; if the impedance is too low, useful conversion gain will be sacrificed, as shown in Figure 29.

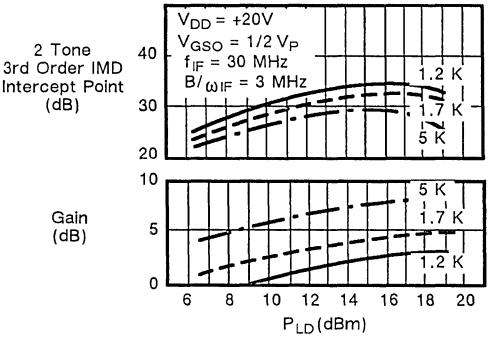


Figure 29. Gain and IMD vs. Local Oscillator Drive

Mixer Performance

Quad FET arrays with both high and low pinchoff voltage levels were used in evaluation of the active double-balanced mixer; the prototype mixer exhibited clearly superior characteristics, compared to equivalent small-signal passive double-balanced mixers. The low- to medium-level pinchoff voltage quad FET array performed slightly better than the high-level pinchoff devices (5.5 V), solely because of a limitation in available local oscillator power. Performance of several types of mixers is made in Table 8.

Conclusion

It may be concluded that performance of the active double-balanced mixer contributes overall system gain in areas critical to telecommunications practice, and reduces associated amplifier requirements.

SECTION 3: A COMMUTATION DOUBLE-BALANCED MOSFET MIXER OF HIGH DYNAMIC RANGE

INTRODUCTION

Heretofore, most mixers sporting a high dynamic range have been either the passive diode-ring variety - available from numerous vendors - or the active FET mixer. The latter is often implemented, using either the Siliconix U310 or the Siliconix U350, as described in Sections 1 and 2.

Common to both the diode and FET is their square-law characteristic so important in maintaining low distortion during mixing. However, equally important for high dynamic range is the ability to withstand overload that has been identified as a principle cause of distortion in mixing[13]. Some passive diode-ring mixer designs have resorted to paralleling of diodes to effect greater current handling, yet the penalty for this apparent improvement is the need for a massive increase in local-oscillator power.

Here we examine a new FET mixer where communication achieves high dynamic range without exacting the anticipated penalty of increased local-oscillator drive. Using the Siliconix Si8901 monolithic quad-ring small-signal double-diffused MOSFET, third-order intercept points upward of +39 dBm (input) have been achieved with only +17 dBm of local-oscillator drive. A comparison between the Si8901 double-balanced mixer and the conventional diode ring double-balanced mixer is offered in Figure 30 where we see an order-of-magnitude improvement in performance at local-oscillator power levels substantially lower than heretofore possible with the conventional mixer.

Conversion Efficiency Of The Commutation Mixer

Unlike either the conventional diode-ring mixer or the active FET mixer, the commutation mixer relies on the switching action of the quad-FET elements to effect mixing action. Consequently, the commutation mixer is, in effect, no more than a pair of switches reversing the phase of the signal carrier at a rate determined by the local-oscillator frequency. Ideally, we would anticipate little noise contribution, and

Table 8
Comparison Between Active, Passive, and MOSFET Double-Balanced Mixers

Characteristic	Active FET	Passive Low-Level	Passive High-Level	MOSFET Switch
Frequency Range (MHz)	50-250	0.5-500	0.5-500	0.2-100
AM Local Oscillator Noise Rejection (dB)	45	Unknown	Unknown	Unknown
Dynamic Unbalance (dB)	0.15	Unknown	Unknown	Unknown
Isolation RF-Local Oscillator (dB)	35	35	40	30
Isolation Local Oscillator - RF (dB)	60	25	30	25
Overall Noise Figure (SSB) (dB)	8.0	8.5	8.5	9.0
Local Oscillator Drive Level (dBm)	+15	+7	+17	+30
Two-Tone IMD Intercept Point* (dBm)	+34	+15	+28	35
Conversion Gain (db)	+4	-8	-8	-8
1 dB Compression (dBm)	+13	+1	+8	+29
Desensitization Level** (dBm)	+13	+1	+8	+29

* Output - measured at recommended LO drive level.

** The level for a nearby unwanted signal (separated 200 kHz) to compress a desired signal of -15 dBm by 1 dB.

since the switching mixer - consisting of four MOSFET "switches" - has finite ON-state resistance, performance is similar to that of a switching attenuator. As a result, the conversion efficiency of the commutation mixer may be expressed as a loss.

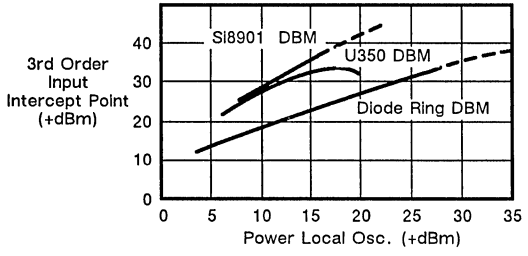


Figure 30. Performance Comparison of Double Balanced Mixers

This loss results from two related factors. First, is the r_{DS} of the MOSFET relative to the signal impedance (R_g) and intermediate frequency (IF) impedance (R_L); second - and a more common and expected factor - is the loss attributed to signal conversion to undesired frequencies. The latter signal conversion involves the image and harmonic frequencies. There are, however, ways to reduce the effects of undesired frequency generation by filtering.

The effect of r_{DS} of the MOSFETs may be determined from the analysis of the equivalent circuit shown in Figure 31, assuming that our local oscillator wave form is an idealized square wave. It is not, but if we assume that it is, our analysis is greatly simplified; and for a commutation mixer, a high local-oscillator voltage begins to approach the ideal waveform of a square wave.

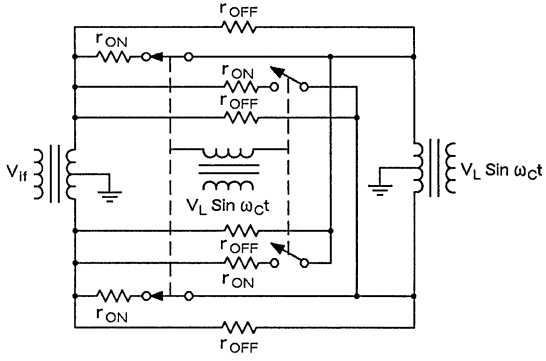


Figure 31. Equivalent Circuit of Communication Mixer

Figure 31, showing switches rather than MOSFETs, also identifies the ON-state resistance, r_{DS}, as well as the OFF-state resistance, r_{OFF}. The latter can be disregarded in this analysis as it is generally extremely high ($2 \cdot 10^9\ \Omega$). On the other hand, the ON-state resistance, r_{DS}, together with the source and load impedances (i.e. signal and intermediate-frequence impedances) directly affects the conversion efficiency.

If we assume that our local-oscillator excitation is an idealized square wave, the switching action may be represented by the Fourier series as,

$$f(x) = \frac{1}{2} + \frac{2}{\pi} \sum_{n=1}^{\infty} \frac{\sin(2n-1)\,\omega t}{(2n-1)} \qquad (25)$$

The switching function, $\epsilon(t)$, shown in the derivative equivalent circuit of Figure 32, is derived from the magnitude of this Fourier series expansion as a *power* function by squaring the first term, i.e. $(2/\pi)^2$.

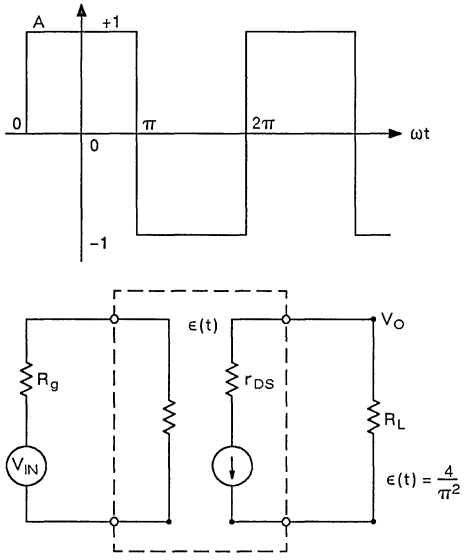


Figure 32. Derivative Equivalent Circuit

The available power that can be delivered from a generator of RMS open-circuit terminal voltage, V_{IN}, and internal resistance, R_g, is

$$P_{av} = \frac{V_{IN}^2}{4R_g} \qquad (26)$$

or, in terms shown in Figure 33

$$P_{av} = \frac{V_{IN}^2}{\pi^2 R_g} \qquad (27)$$

the output power, deliverable to the intermediate-frequency port, is

$$P_{out} = \frac{V_O^2}{R_L} \qquad (28)$$

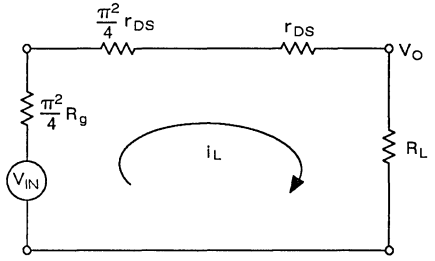


Figure 33. The Power-Loop Circuit with All Elements Equivalent Based on the Transfer Function, $\epsilon(t) = \frac{4}{\pi^2}$

To arrive at V_o, we first need to obtain the loop current, i_L, which from Figure 33 offers

$$i_L = \frac{V_{in}}{\frac{\pi^2}{4}(R_g + r_{DS}) + R_L + r_{DS}} \qquad (29)$$

then

$$V_O = \frac{V_{in} R_L}{\frac{\pi^2}{4}(R_g + r_{DS}) + R_L + r_{DS}} \qquad (30)$$

Combining Equations 28 and 30,

$$P_{out} = \frac{V_{in}^2 R_L}{\left[\frac{\pi^2}{4}(R_g + r_{DS}) + R_L + r_{DS}\right]^2} \qquad (31)$$

9

Conversion efficiency - in the case for the commutation mixer, a loss - may be calculated from the ratio of P_{av} and P_{out}

$$L_C = 10 \text{ Log } \frac{P_{av}}{P_{out}} \text{ dB} \quad (32)$$

Substituting Equation 27 for P_{av}, and Equation 31 for P_{out}, we obtain

$$L_C = 10 \text{ Log} \frac{\left[\frac{\pi^2}{4}(R_g + r_{DS}) + R_L + r_{DS}\right]^2}{\pi^2 R_L R_g} \text{ dB} \quad (33)$$

The conversion loss represented by Equation 33 is for a broadband double-balanced mixer with the image and sum frequency (RF + LO) ports shorted and the signal frequency (RF) matched to the characteristic line impedance. The ideal commutating mixer operating with resistive source and load impedances will result in having the image and all harmonic frequencies dissipated. For this case, the optimum conversion loss reduces to

$$L_C = 10 \text{ Log } \frac{\pi^2}{4} \text{ dB} \quad (34)$$

or -3.92 dB

However, a truly optimum mixer also demands that the MOSFETs exhibit an ON-state resistance of zero ohms and, of course, an ideal square-wave excitation. Neither is possible in a practical sense.

Equation 33 can be examined for various values of source and load impedances as well as r_{DS} by graphical representation, as shown in Figure 34, remembering that a nominal 3.92 dB must be added to the values obtained from the graph.

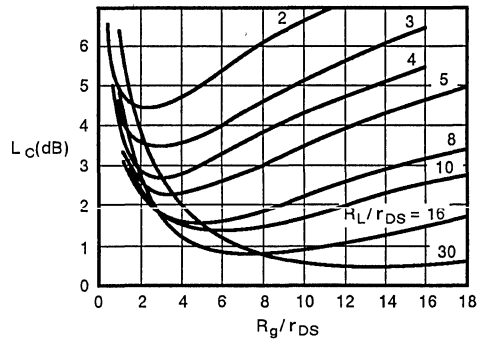


Figure 34. Insertion Loss As A Function of r_{DS}, R_L & R_g

To illustrate how seriously the ON-state resistance of the MOSFETs affects performance, we need only to consider the Si8901 with a nominal r_{DS} (at V_{GS} = 15V) of 23 Ω. With a 1:1 signal transformer (50 to 25-0-25 Ω), R_g/r_{DS} = 1.1. Allowing a 4:1 IF output transformer to a 50-Ω preamplifier, the ratio R_L/r_{DS} approximates 4. From Figure 34 we read a conversion loss, Lc, of approximately 3.7 dB, to which we add 3.92 dB for a total loss of 7.62 dB. Additionally, we must also include the losses incurred by both the signal and IF transformers. The result compares favorably with measured data.

A careful study of Figure 34 reveals what appears as an anomalous characteristic. If we were to raise R_g/r_{DS} from 1.1 to 4.3 (by replacing 1:1 transformer with a 1:4 to effect a signal-source impedance of 100-0-100 Ω), we would see a dramatic improvement in conversion efficiency. The anomaly is that this suggests that a mismatched signal-input port improves performance.

Caruthers[14] first suggested that reactively terminating all harmonic and parasitic frequencies would reduce the conversion loss of a ring demodulator to zero. This, of course, would also require that the active mixing elements (MOSFETs in this case) have zero r_{DS}, in keeping with the data of Figure 34.

A double-balanced mixer is a 4-port - consisting of a signal, image, IF, and a local-oscillator port. Of these, the most difficult to terminate is the image frequency port simply because, in theory, it exists as a separate port, but in practice it shares the signal port. Any reactive termination would, therefore, be narrow-band irrespective of its proximity to the active mixing elements.

The performance of an image-termination filter offering a true reactance to the image frequency (100% reflective) may be deduced to a reasonable degree from Figure 34, if we first presume that the conversion loss between signal and IF compares with that between signal and image. The relationship is displayed in Figure 35 where we see the expected variation in amplitude proportional to conversion efficiency (inversely proportional to conversion loss).

Image-frequency filtering affects more than conversion efficiency. As the phase of the detuned-short position of the image-frequency filter is varied, we are able to witness a cyclical variation in the intermodulation distortion as has been confirmed by measurement, shown in Figure 36. By comparing Figure 35 with Figure 36, we see that any improvement in conversion loss appears to offer a corresponding degradation in intermodulation distortion!

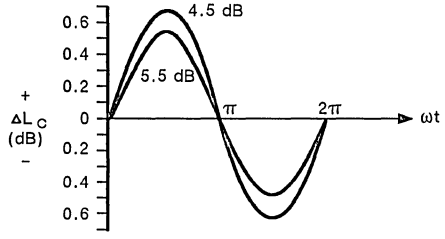


Figure 35. Effect of Image Termination on Conversion Loss

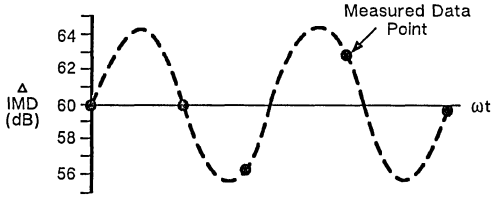


Figure 36. Effect of Image Termination on 3rd-Order Distortion

Intermodulation Distortion

Unbalanced, single-balanced, and double-balanced mixers are distinguished by their ability to selectively reject spurious frequency components, as defined in Table 5. The double-balanced mixer, by virtue of its symmetry, suppresses twice the number of spurious frequencies as the single-balanced mixer suppresses.

In the ideal mixer, the input signal is translated to an intermediate frequency without distortion, that is without imparing any of the contained information. Regrettably, the ideal mixer does not occur in practice. Because of certain non-linearities within the switching elements (MOSFETs in this case) as well as imperfect switching resulting in phase modulation, distortion results.

Identifying Intermodulation Distortion Products

The most damaging intermodulation distortion (IMD) products in receiver design are generally those attributed to odd-order and, in particular, those identified as the third-order IMD.

Earlier, in Equation 24, we saw that any non-linear device may be represented as a power series which can be reduced to the terms shown in Table 6.

The second-order term is the desired intermediate frequency we seek, all other higher-orders are undesirable but, unfortunately, are present to a varying degree.

There are both fixed-level IMD products and level-dependent IMD products. The former are produced by the interaction between a fixed-level signal, such as the local oscillator and the variable-amplitude signal. The resulting frequencies may be identified by

$$n f_1 \pm f_2 \qquad (35)$$

where, n is an integer greater than 1.

Level-dependent IMD products result from the interaction of the harmonics of the local oscillator and those of the signal. The resulting frequencies may be identified by

$$n f_1 \pm m f_2 \qquad (36)$$

where, m and n are integers greater than 1.

9

For a mixer to generate IMD products at the intermediate frequency, we must account for at least a two-step process. First, the generation of the harmonics of the signal and local oscillator; and second, the mixing or conversion of these frequencies to the intermediate frequency. Consequently, the mixer may be modeled as a series connection of two non-linear impedances, the first to generate the harmonic products and the second to mix or convert to the intermediate frequency. Although many harmonically-related products are possible, we will focus principally on the odd-order IMD products.

If we allow two interfering signals, f1 and f2, to impinge upon the first non-linear element of our mixer model, the result will be 2f1 - f2 and 2f2 - f1. These are identified as third-order intermodulation products (IMD_3). Other products are also generated taking the form 3f1 - 2f2 and 3f2 - 2f1, called fifth-order IMD products (IMD_5). Unlike the even-order products, odd order products lie close the the fundamental signals and, as a consequence, are most susceptible to falling within the passband of the intermediate frequency and thus degrading the performance of the mixer.

A qualitative definition of linearity based upon intermodulation distortion performance is called the intercept point. Convergence occurs when

- the fundamental output (IF) response is directly proportional to the signal input level;
- the second-order output response is proportional to the square of the signal input level; and,
- the third-order output response is proportional to the cube of the signal input level.

The point of convergence is termed the intercept point. The higher the value of this intercept point, the better the dynamic range.

Intermodulation Distortion in the Commutation Mixer

Although the double-balanced mixer outperforms the single-balanced mixer as we saw in Table 5, a more serious source of intermodulation products results when the local-oscillator excitation departs from the idealized square wave[15,16]. This phenomena is easily recognized by a careful examination of Figure 37, where a sinusoidal local-oscillator voltage reacts not only upon a varying transfer characteristic but also on a varying non-linear, voltage-dependent capacitance (not shown in Figure 37). Although the effects of this sinusoidal transition are not easily derived, Ward[17] and Rafuse[18] have concluded that lowering R_g will provide improved intermodulation performance! This conflicts with low conversion loss, as we saw in Figure 34, but agrees with Equation 37.

$$20 \text{ Log} \left(\frac{\frac{V_S}{t_r \, \omega_{LO} \, V_C}}{8} \right)^2 \text{dB} \qquad (37)$$

where,

V_C is the peak-to-peak local-oscillator voltage,

V_S is the peak signal voltage,

t_r is the rise and fall time of V_C,

ω_{LO} is the local-oscillator frequency.

Further examination of Figure 37 reveals that the sinusoidal local-oscillator excitation results in phase modulation. That is, as the sinusoidal wave goes through a complete cycle, the resulting gate voltage, acting upon the MOSFET's tranfer characteristic, produces a resulting non-linear waveform. Since all FETs have some offset - a JFET has cut-off voltage, and a MOSFET has threshold voltage - it is important,

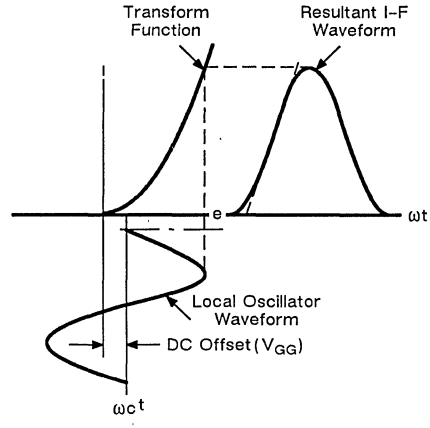


Figure 37. Effect of Sinusoidal L.O. Waveform on I-F Linearity

both for symmetry as well as for balance, to offer some dc offset voltage to the gates. Optimum IMD performance demands that the switches operate in a 50% duty cycle; that is, the switches must be fully ON and fully OFF for equal time. Without some form of offset bias, this would be extremely difficult unless we were to implement an idealized square-wave drive.

Walker[19] has derived an expression showing the predicted improvement in the relative level of two-tone third-order intermodulation products (IMD_3) as a function of the rise and fall times of the local-oscillator waveform.

Equation 37 offers us several interesting aspects on performance. Since any reduction in the magnitude of V_S improves the IMD, we again discover that by lowering R_g (which, in turn, decreases the magnitude of V_S) appears to benefit performance. Second, the higher the local-oscillator voltage, the better the IMD performance. Third, if we can provide the idealized square-wave drive, we achieve an infinite improvement in IMD performance!

An additional fault of sinusoidal local-oscilaltor excitation results whenever the wave approaches the zero-crossing at half-period intervals. As the voltage decays, we find that any signal voltage may overload the MOSFETs causing intermodulation and crossmodulation distortion[20]. This can be easily visualized from Figure 38 where we see the classic i-e characteristics of the MOSFET at varying gate voltages. Only at substantial gate voltage do we witness reasonable linearity and, consequently, good dynamic range.

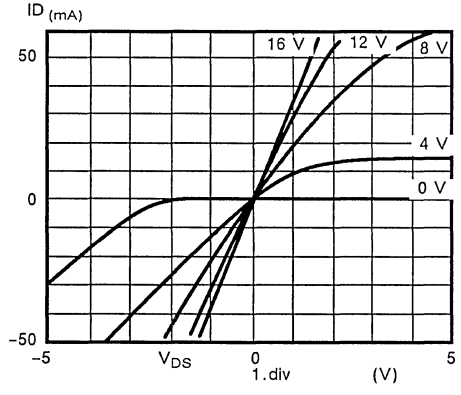


Figure 38. First & Third Quadrant I-E Characteristics Showing Effect of Gate Voltage Leading to Large-Signal Overload Distortion

Dynamic Range Of The Commutation Mixer

As the two-tone intercept point increases in magnitude, we generally expect a like improvement in dynamic range results. Yet, as we have concluded from earlier study, the intermodulation products appear to be a function of both the generator or source impedance as well as ratio R_g/r_{DS} and R_L/r_{DS} (Figure 34).

In any receiver, performance can be quantified by the term *dynamic range*. Dynamic range can be extended by improving the sensitivity to low-level signals and by increasing the power handling ability without being overcome by interfering intermodulation products or the effects caused from desensitization.

There are rules to follow if we are to improve the low-level signal sensitivity. Ideally we would like a mixer to be transparent, acting only to manipulate the incoming signals for easy processing by subsequent equipment. The perfect mixer would have no conversion loss and a low noise figure. However, in the preceding analysis we discovered that optimum intermodulation performance occurred when the signal input port is mismatched to the quad MOSFETs (Figure 34). It now becomes clear that a performance trade-off appears necessary. Either we seek low conversion loss and with it a higher noise figure, or we aim for the highest two-tone third-order intercept point. Fortunately, as we seek the latter, our dynamic range will actually improve since a mismatched signal port has less effect upon the signal-to-noise performance of the mixer than does a matched signal port have upon intermodulation distortion.

Convention has identified minimum sensitivity to be the weaker signal which will produce an output signal that is 10 dB over that of the noise in a prescribed bandwidth (usually 1kHz), or

$$\text{Sens.} = 20 \text{ Log} \frac{V_S + V_N}{V_N} + \text{dB} \qquad (38)$$

Desensitization occurs whenever a nearby unwanted signal causes the compression of the desired signal. The effect appears as an increase in the mixer's conversion loss.

The Si8901 As A Commutation Mixer

Because of package and parasitic constraints, the Si8901 is best suited for performance in the HF to low VHF region. A surface-mount version may extend performance to somewhat higher frequencies.

In our review of intermodulation distortion, we recognized that to achieve a high intercept point the local-oscillator drive must

- approach the ideal square-wave,
- ensure a 50% duty cycle,
- offer sufficient amplitude to ensure a full ON and OFF switching condition, as well as to offer reduced r_{DS} when ON.

Furthermore, to maintain superior overall performance - both in conversion loss, dynamic range (noise figure) and intercept point - some form of image-frequency termination would be highly desirable even though, understandably, the mixer's bandwidth would be restricted.

Consequently, the principal effort in the design of a high dynamic range commutation mixer is two-fold. First, and most crucial, is to achieve a gating or control voltage sufficient to ensure a positive and hard turn-ON as well as a complete turn-OFF of the mixing elements (MOSFETs). Second, and of lesser importance, is to properly terminate the parasitic and harmonic frequencies developed by the mixer.

Establishing the Gating Voltage

Local oscillator injection to the conventional diode ring, FET, or MOSFET double-balanced mixer is by the use of the broadband, transmission-line transformer, as shown in Figure 39. For the diode-ring mixer where switching is a function of loop current, or for active FET mixers that operate on the principle of transconductance and thus need little gate voltage, the broadband transformer is adequate. If this approach is used for the commutation mixer, we would need extraordinarily high local-oscillator drive to ensure positive turn-ON. Rafuse and Ward used a minimum of 2 W to ensure mixing action; Lewis and Palmer achieved high dynamic range using 5 Watts! The MOSFETs used in these early designs were p-channel, enhancement-mode (2N4268 devices with moderately high threshold (6 V maximum) and high input capacity (6 pF maximum). All of these early MOSFET double-balanced mixers relied on the conventional 50 to 100-0-100 Ω transformer for local-oscillator injection to the gates.

A major goal is the conservation of power. This goal cannot be achieved using the conventional design. Simply increasing the turns ratio of the coupling transformer is thwarted by the reactive load presented by the gates.

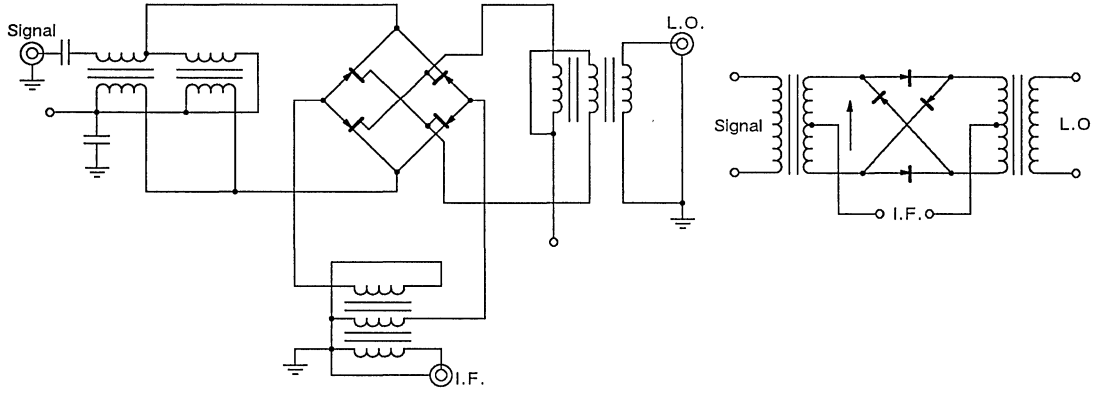


Figure 39. Local Oscillator Drive Using Conventional Broadband Transformers

The obvious solution is to use a resonant gate drive. The voltage appearing across the resonant task - and thus on the gates - may easily be calculated.

$$V = (P \cdot Q \cdot X)^{1/2} \qquad (39)$$

Where, P is the power delivered to the resonant tank circuit,

Q is the loaded Q of the tank circuit, and

X is the reactance of the gate capacity.

Since the gate capacitance of the MOSFET is voltage dependent, the reactance of the gate becomes dependent upon the impressed excitation voltage. To allow this would severely degrade the IMD performance of the mixer. However, we can minimize the change in gate capacitance and remove its detrimental influence using a combination of substrate and gate bias, as shown in Figure 40. Not only does this show itself beneficial in this regard, but as we saw in Figure 37, a gate bias is necessary to ensure the required 50% duty cycle. Furthermore, a negative substrate voltage ensures that each MOSFET on the monolithic substrate is electrically isolated and that each source-/drain-to-body diode is sufficiently reverse biased to prevent half-wave conduction.

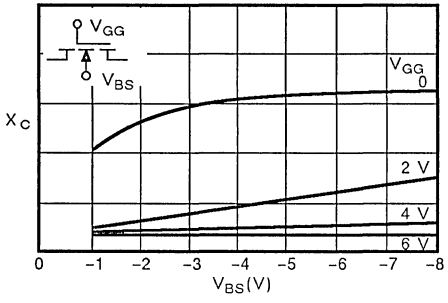


Figure 40. Effect of Bias on Gate Reactance

Implementing the resonant gate drive may take any of several forms. The resonant tank circuit may be merged with the oscillator, or it can be varactor-tuned Class B stage, or as in the present design, an independent resonant tank, shown in Figure 41.

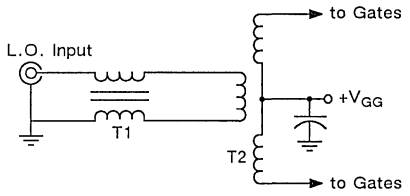


Figure 41. Resonant - Gate Drive. T2 is Tuned to Resonate with C_{gs} of Si8901

To ensure symmetrical gate voltage in 180-degree anti-phase, if the local-oscillator drive is asymmetrical, i.e., fed by unbalanced coax, an unbalanced-to-balanced balun must be used (T1 in Figure 41); otherwise, capacitive unbalance results with an attendant loss in mixer performance.

Table 9 offers an interesting comparison between a resonant-gate drive with a loaded tank Q of 14 and a conventional gate drive using a 50 to 100-0-100 Ω transformer. The importance of a high tank Q is graphically portrayed in Figure 42. The full impact of a high gate voltage swing can be appreciated by using Equation 37. Here, as V_C (gate voltage) increases the intermodulation performance (IMD) also improves, as we might intuitively expect. Calculated and measured results are shown in Figure 43 and demonstrate reasonable agreement. The difference may reflect problems encountered in measuring V_C as any probe will inadvertently load, or detune, the resonant tank even with the special care that was taken to compensate.

Table 9

Power in (mW)	NR Gate Voltage (V)	Res Gate Voltage (V)
10	0.20	5.4
20	0.29	7.7
30	0.33	9.4
60	0.44	13.3

Comparison of a-c gate voltage versus local-oscillator drive between a non-resonant (NR) and resonant (Res) tank with a loaded Q of 14 (Freq. 150 MHz)

If we have the option to choose "high side" or "low side" injection - i.e., having the local-oscillator frequency above (high) or below (low) the signal frequency - a closer inspection of Equation 37 should convince us to choose low-side injection.

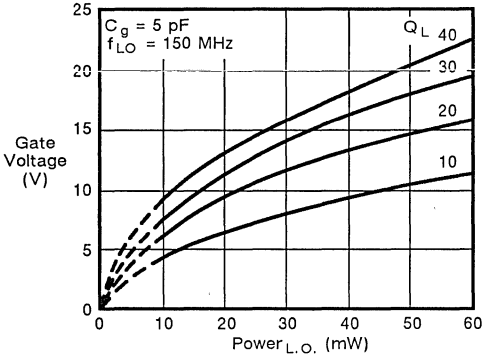


Figure 42. Influence of Loaded Q on Gate Voltage vs. L.O. Power

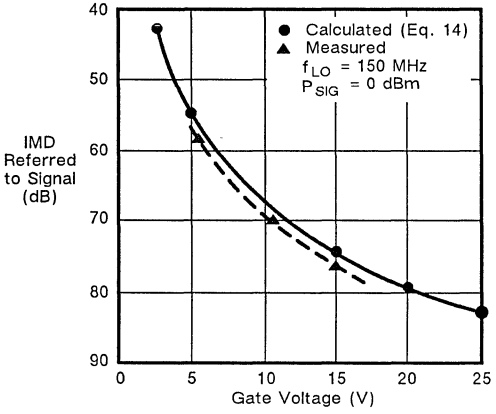


Figure 43. Effect of Gate Voltage on IMD Performance

Terminating Unwanted Frequencies

If our mixer is to be operated over a restricted frequency range where the local oscillator and signal frequencies can be manipulated, image-frequency filtering may be possible. Image-frequency filtering does affect performance - for high-side local-oscillator injection, an elliptic-function low-pass filter, or for low-side injection, a high-pass filter might offer worthwhile improvement. In either case, the filter offers a short-circuit reactance to the image frequency forcing the image to return once again for demodulation. The results of using a low-pass filter with the prototype commutation mixer are known from our earlier examination of Figures 35 and 36.

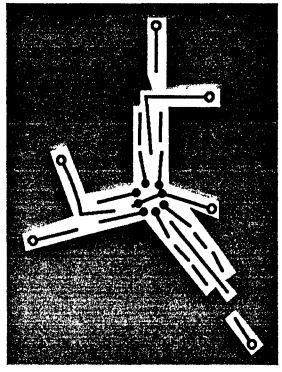


Figure 44. Mask Layout PCM Prototype Commutation Mixer

The resonant-gate drive consisting of a high-Q tank offers adequate bypassing of the intermediate frequency and image frequency.

If the IF port is narrow band, filtering may be possible by simply using a resonant L-C network across the primary of the transformer.

Design Techniques in Building the Mixer

The mixer was fabricated on a high-quality double-copper clad board shown in Figure 44. An improvised socket held the Si8901.

The signal and IF ports used Mini-Circuits, Inc., plastic T-case RF transformers. For the intermediate frequency, the Mini-Circuits T4-1 (1:4) was used; for the signal, the Mini-Circuits T1-1T (1:1) was used. The resonant tank was wound on a one-quarter-inch-diameter ceramic form with no slug. The unbalanced-to-balanced resonant tank drive used a T4-1. The schematic diagram, Figure 45, is for a commutation mixer, operating with an IF of 60 MHz.

The principle effort involved the design of the resonant-gate drive. This necessitated an accurate knowledge of the gate's total capacitive loading effect. To accomplish this, a precision fixed capacitor (5 pF) was substituted for the Si8901, and at resonance, it was a simple matter to calculate the inductance of the resonant tank. Substituting the Si8901 made it again a simple task to determine the capacitive effects of the Si8901. Once known, a high-Q resonant tank can be quickly designed and implemented. To ensure good interport isolation, symmetry is important, so care is necessary in assembly to maintain mechanical symmetry, especially with the primary winding.

Performance of the Si8901 Prototype Commutation Mixer

The primary goal in developing a commutation double-balanced mixer is to achieve a wide dynamic range. If this task can be accomplished with an attendant savings in power consumption, then the resulting mixer design should find wide application in HF receiver design.

The following tests were performed.

- conversion efficiency (loss)
- two-tone, 3rd order intercept point
- compression level
- desensitization level
- noise figure

Conversion loss and the intercept point are directly dependent upon the magnitude of the local-oscillator power. The prototype mixer's performance is offered in Figure 46, where the input intercept and conversion loss are plotted.

Both the compression and desensitization levels may appear to contradict reason. Heretofore, conventional diode-ring demodulators exhibited compression and desensitization levels an order of magnitude below the local-oscillator power level. However, with a commutation MOSFET mixer, switching is not accomplished by the injection of loop current but by the application of gate voltage. At a local-oscillator power level of + 17 dBm (50 mW), the 2-dB compression level and desensitization level were +30 dBm!

The single-sideband HF noise figure of 7.95 dB was measured at a local oscillator power level of +17dBm.

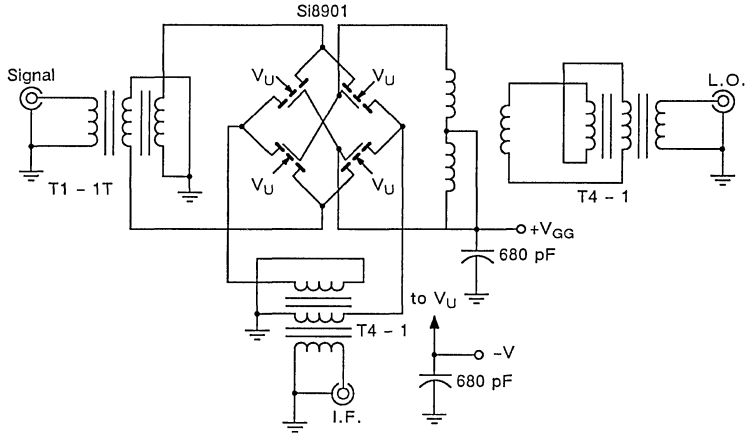


Figure 45. Prototype Commutation Double-Balanced Mixer

CONCLUSION

Achieving a high gate voltage to effect high-level switching by means of a resonant tank is not a handicap. Although one might, at first, label the mixer as narrow-band, in truth the mixer is wide-band. For the majority of applications, the intermediate frequency is fixed, that is, narrow band. Consequently, to receive a wide range of signal frequencies, the local oscillator is tuned across a similar band. In modern technology the tuning can be accomplished by numerous methods, not the least of which might be electronically using varactors. The resonant tank also may take several forms. It can be part of the oscillator, it can be varactor-tuned driver electronically tracking the local oscillator[21].

If the local-oscillator drive was processed to offer a more rectangular waveform, approaching the idealized square wave, we might then anticipate even greater dynamic range as predicted by Equation 37.

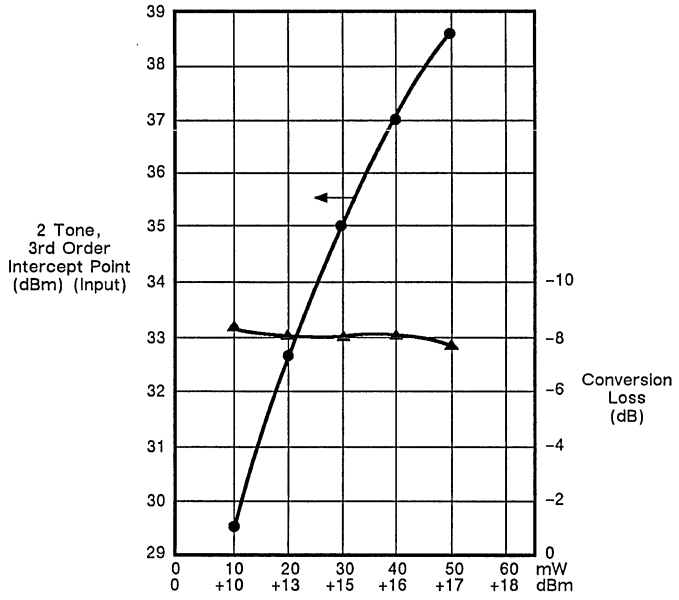


Figure 46. Intercept Point & Conversion Loss

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THE FET CONSTANT-CURRENT SOURCE

INTRODUCTION

The combination of low associated operating voltage and high output impedance make the FET attractive as a constant-current source. An adjustable-current source (Figure 1) may be built with a FET, a variable resistor and a small battery. For good thermal stability, the FET should be biased near the zero temperature coefficient point.

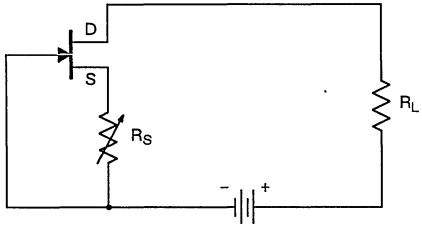


Figure 1. Field-Effect Transistor Current Source

Whenever the FET is operated in the saturated region, its output conductance is very low. This occurs whenever the drain-source voltage V_{DS} is significantly greater than the cut-off voltage $V_{GS(off)}$. The FET may be biased to operate as a constant-current source at any current below its saturation current I_{DSS}.

For a given device where I_{DSS} and $V_{GS(off)}$ are known, the approximate V_{GS} required for a given I_D is

$$V_{GS} = V_{GS(off)}\left[1 - \left(\frac{I_D}{I_{DSS}}\right)^{1/k}\right] \quad (1)$$

where k can vary from 1.7 to 2.0, depending upon device geometry. The series resistor R_S required between source and gate is

$$R_S = \frac{V_{GS}}{I_D} \quad (2)$$

A change in supply voltage or a change in load impedance, will change I_D by only a small factor because of the low output conductance g_{oss}.

$$\Delta I_D = (\Delta V_{DS})\ (g_{oss}) \quad (3)$$

The value of g_{oss} is an important consideration in the accuracy of a constant-current source. As g_{oss} may range from less than 1 μS to more than 50 μS according to the FET type, the dynamic impedance can be greater than 1 MΩ to less than 20 kΩ. This corresponds to a current stability range of 1 μA to 50 μA per volt. The value of g_{oss} depends also on the operating point. Output conductance g_{oss} decrease approximately linearly with I_D, becoming less as the FET is biased toward cut-off. The relationship is

$$\frac{I_D}{I_{DSS}} = \frac{g_{oss}}{g'_{oss}} \quad (4)$$

where

$$g_{oss} = g'_{oss} \quad (5)$$

when

$$V_{GS} = 0 \quad (6)$$

So as $V_{GS} \longrightarrow V_{GS(off)}$, $g_{oss} \longrightarrow$ Zero. For best regulation, I_D must be considerably less than I_{DSS}.

It is possible to achieve much lower g_{oss} per unit I_D by cascading two FETs, as shown in Figure 2.

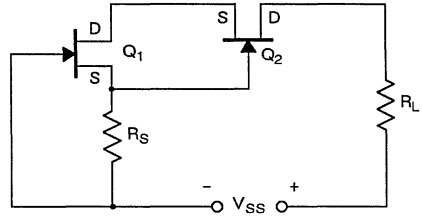
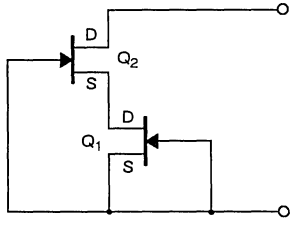


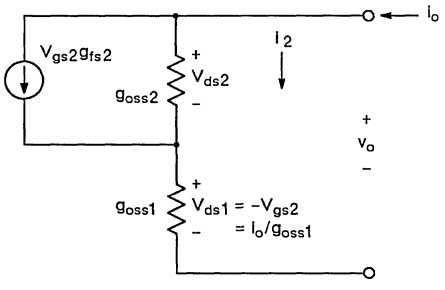
Figure 2. Cascade FET Current Source

Now, I_D is regulated by Q_1 and $V_{DS1} = -V_{GS2}$. The dc value of I_D is controlled by R_S and Q_1. However, Q_1 and Q_2 both affect current stability. The circuit output conductance is derived as follows:

Figure 2 is redrawn in Figure 3 for the condition $V_{GS1} = 0$.



(A)



(B)

Figure 3.

$$i_o = i_2 + v_{GS2}g_{fs2} = v_{ds2}g_{oss2} - i_o\frac{g_{fs2}}{g_{oss1}} \quad (7)$$

$$i_o = \frac{v_{ds2}g_{oss2}g_{oss1}}{g_{oss1} + g_{fs2}} \quad (8)$$

$$v_o = v_{ds1} + v_{ds2} = v_{ds2} + \frac{i_o}{g_{oss1}} \quad (9)$$

$$v_o = v_{ds2}\frac{g_{oss1} + g_{oss2} + g_{fs2}}{g_{oss1} + g_{fs2}} \quad (10)$$

$$g_o = \frac{i_o}{v_o} = \frac{g_{oss1}g_{oss2}}{g_{oss1} + g_{oss2} + g_{fs2}} \quad (11)$$

If $g_{oss1} = g_{oss2}$ (12)

$$g_o = \frac{g_{oss}}{2 + g_{fs}/g_{oss}} \quad (13)$$

when $R_S \neq 0$ as in Figure 2

$$g_o = \frac{g_{oss}^2}{2g_{oss} + g_{fs} + R_S(g_{fs}^2 + g_{oss}g_{fs} + g_{oss}^2)} \quad (14)$$

$$\approx \frac{g_{oss}^2}{g_{fs}(1 + R_S g_{fs})} \quad (15)$$

In either case ($R_S = 0$ or $R_S \neq 0$), the circuit output conductance is considerably less than the g_{oss} of a single FET.

In designing any cascaded FET current source, both FETs must be operated with adequate drain-gate voltage V_{DG}. That is,

$V_{DG} > V_{GS(off)}$, preferably $V_{DG} > 2\,V_{GS(off)}$ (16)

If $V_{DG} < 2\,V_{GS(off)}$, the g_{oss} will be significantly increased, and circuit g_o will deteriorate. For example: A JFET may have a typical $g_{oss} = 4\ \mu S$ at $V_{DS} = -20$ V and $V_{GS} = 0$. At $V_{DS} \sim -V_{GS(off)} = 2$ V, $g_{oss} \sim 100\ \mu S$.

The best FETs for current sources are those having long gates and consequently very low g_{oss}. The Siliconix 2N4869 exhibits typical $g_{oss} = 1\ \mu S$ at $V_{DS} = 20$ V. A single 2N4869 in th circuit of Figure 4 will yield a current source adjustable from 5 μA to 1 mA with internal impedance greater than 2 MΩ.

9

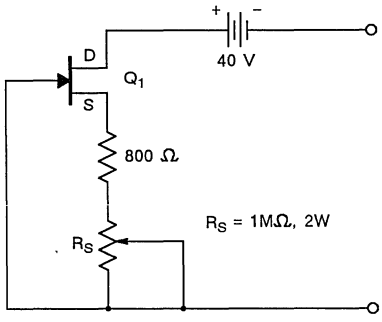
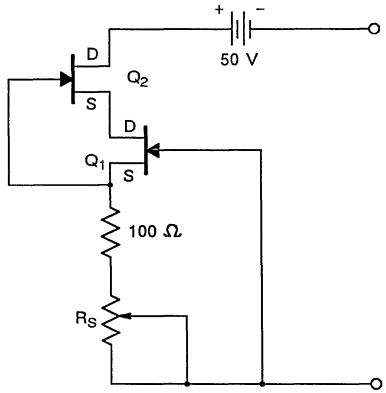


Figure 4. Adjustable Current Source
R_S = 1 MΩ, 2 W



Q_1 = 2N4340
Q_2 = 2N4341
R_S = 1MΩ, 2W

Figure 5. Cascade FET Current Source

The cascade circuit of Figure 5 provides a current adjustable from 2 μA to 1 mA with internal resistance greater than 10 MΩ.

Siliconix also offers a line of JFETs with a resistor fabricated on the device, thus creating a 10% current range. The series is called the CR022 (0.22 mA range) through the CR530 (5.3 mA range). See the data sheet section for specific part types. The devices allow precision designs using a single device versus the typical approach using several components.

LOW-POWER MOSFETS FOR "SMART" TELEPHONES

Deregulation of the telephone industry has brought fierce competition among electronic telephone manufacturers. "Smart" phones now provide special services, such as automatic re-dial, elapsed time indicators, repertory dialing, visual display, and many other attractive consumer aids. One circuit described in this article uses low-power MOSFETs to provide all the basic high-voltage switching functions needed in an electronic telephone set.

This article also describes a basic remote-isolation device or RID* circuit implemented using low-power MOSFETs. RIDs are used to identify telephone link problems that result from faults in customer's equipment rather than faults in the phone company system. A RID is placed on the telephone line at the interface between the telephone line and the customer-owned wiring. When the telephone company tests the line, a standard test signal activates the RID, momentarily disconnecting the customer-owned equipment and leaving a standard termination connected. If the problem is isolated to the customer-owned equipment, the telephone company can save from $50 to $80 for an unnecessary service call. This savings easily justifies the modest cost of the RID, and recent legislation encourages their installation on all new central office lines in the U.S.

Electronic Telephone Handset

Figure 1 shows a block diagram of the essential functions of a telephone set. On the left side, the telephone lines (known as tip and ring in the U.S. or as A and B in Europe) enter the handset (known as a station set in the U.S.). In Europe, there may also be a third line which allows one to signal the operator by momentarily connecting this line to the B conductor. On the right side of the diagram, separate pairs of wires go to the microphone and earpiece. These transmit and receive functions are separated by circuitry known as a hybrid. On the two-wire (left) side of the hybrid, tip and ring carry both incoming and outgoing signals. However, on the four-wire (right) side, incoming and outgoing signals are separated. This prevents speech signals generated by the microphone from being repeated with deafening force into the ear of the person speaking. Traditionally, the hybrid function was provided with a transformer circuit; however, in recent times, electronic circuits have been contrived to perform the same function.

A pair of buttons on the top of most handsets operate a simple closure switch known as the hookswitch. (Named from early telephones that switched when the earpiece was hung on a hook.) The hookswitch can also be used for pulse dialing. In pulse dialing, the loop is repeatedly opened and closed to signal dialing instructions to the exchange. Traditionally, this is done at a rate of 10 pulses per second. In tone dialing, special oscillators (known as dual-tone multi-frequency generators) generate tones representing the dialing instructions. These tones are normally applied across the loop without interruption.

The bridge circuit shown in Figure 1 is a polarity guard that protects the telephone circuitry against accidental polarity inversion of the linefeed voltage or accidental crossing and substitution of the telephone lines. Since this is normally done with pn diodes, the 1.5 V dropped across these diodes can limit telephone circuits designed to operate on long loops where only a few volts are available at the end of the loop to run the handset.

The surge protection block prevents the telephone circuitry from being damaged by high-voltage surges. Telephone lines are typically routed in bundles with a metallic grounded shield around the bundle. If the metallic shield is struck by lightning, a high-voltage surge is produced on all of the lines in the bundle. This surge may run to tens of thousands of volts. The most important feature of the protector circuit is a carbon block spark gap, which arcs over at about 400 V to 800 V. When electronic components are used in the telephone set, this surge needs to be further reduced by a circuit comprising resistors and a metal oxide varistor which breaks over at 200 V.

The ring detection circuit is designed to recognize the 20-Hz waveform of an incoming ring signal and thus produce a ringing tone or a logical output which operates a separate ringing-tone generator. In an electronic phone, it is often desirable to disable the

*This device has other common names, such as maintenance termination unit and remote disconnect unit.

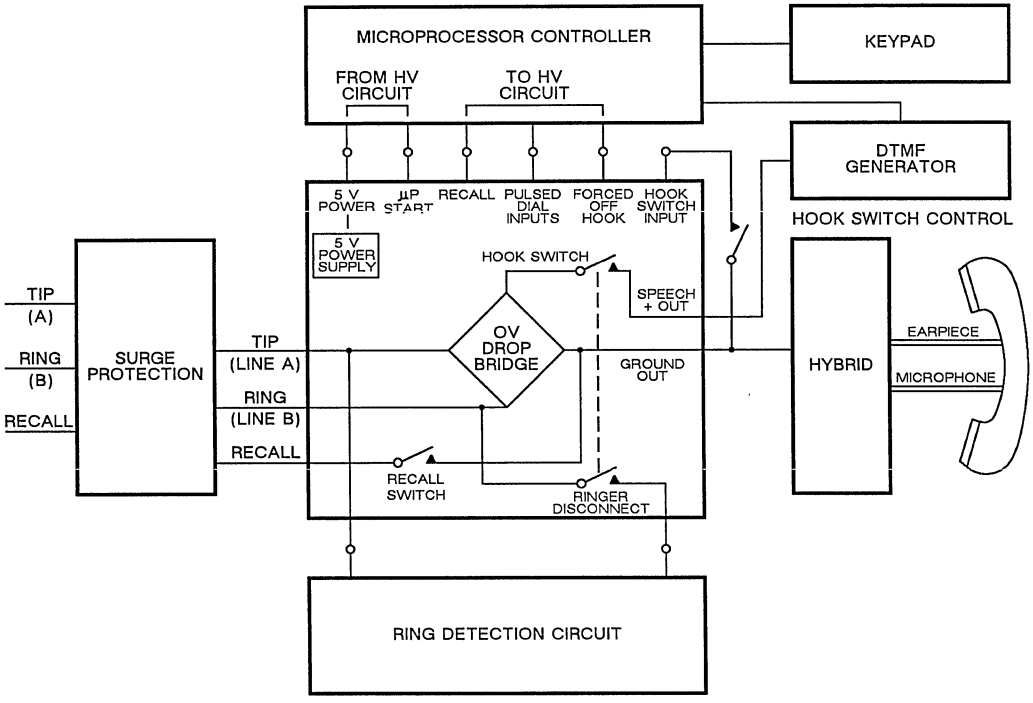
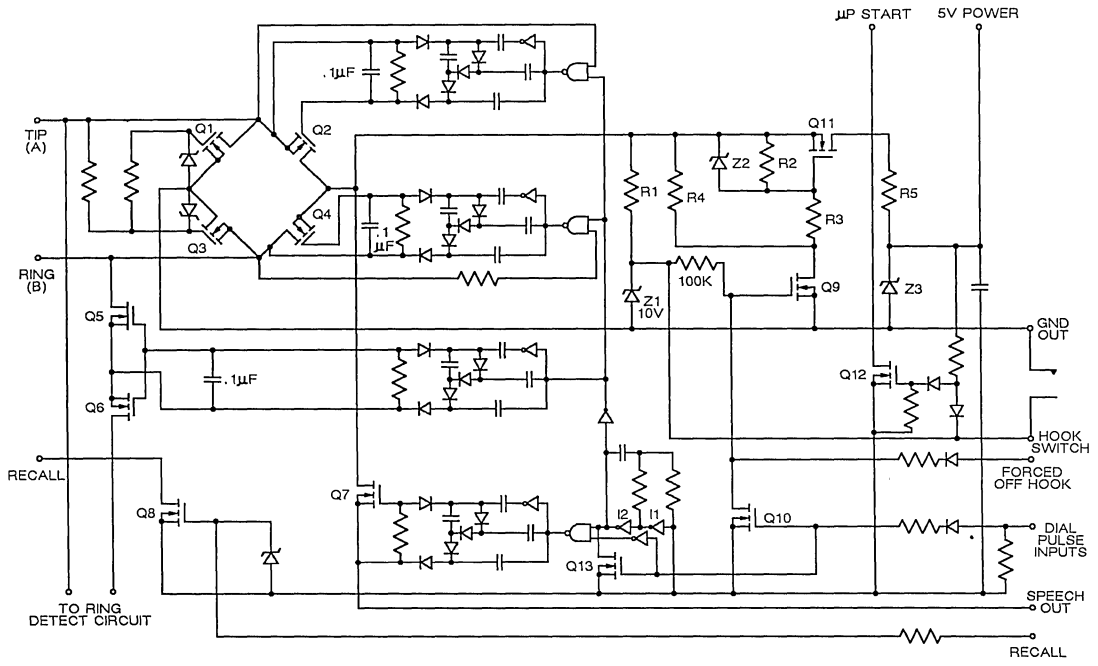


Figure 1. Electronic Telephone with Solid-State High-Voltage Switching Elements

ring detection circuit when the handset is picked up, thus preventing accidental triggering of the ring detection circuit. If the station set is used in a hands-free telephone application, an off-hook condition must be generated to draw current from the line while the handpiece is resting on the hookswitch. This function, the "forced off hook" capability, along with the generation of dial pulse or dial tone signals, is initiated by the microprocessor controller, the hallmark of a smart phone.

In Figure 1, a number of telephone handset functions associated with high-voltage switching are illustrated. These switching functions are ideally provided using low-power MOSFETs, regardless of how the controller, DTMF generator, hybrid, and other components are implemented. Inside this box, a 5-V power supply draws a small amount of power from the telephone line and generates the 5 V of power needed to run the low-power CMOS logic in the handset. The polarity-guard diode bridge is synthesized from low-cost power MOSFETs which provide the same protection as the diode bridge without interposing a fixed 1.5-V drop into the telephone loop. A switch provides the hookswitch function, and when pulsed on and off, it can also be used for dial pulse signaling. A ring disconnect switch disconnects the ring detector when the handpiece is picked up, and a recall switch momentarily connects the recall line to the more negative of the two telephone conductors when a 5-V signal is applied to the recall input. Logic signals tell the microprocessor when its power supply has reached full voltage so the microprocessor functions can begin.

Figure 2 shows the detailed implementation of the handset switching circuit. At all times, the intrinsic diodes of the MOSFET bridge, consisting of transistors Q1 through Q4, bleed through small amounts of current of the correct polarity. This current passes through the 10-MΩ resistor, R1, to the 10-V zener diode, Z1, connected by a 100-kΩ resistor to the gate of Q9. Thus the 10-MΩ resistor is permanently



Q1	VN2010L	Q8	VN2010L
Q2	VN2010L	Q9	VN2010L
Q3	VN2010L	Q10	2N7000
Q4	VN2010L	Q11	VP2410L
Q5	ND2406 Depletion Mode	Q12	2N7000
Q6	ND2406 Depletion Mode	Q13	2N7000
Q7	VN2010L		

10 pf capacitors have 250 V blocking

All non-zener diodes are in 814

CD74HC04E

MC14011B

Figure 2. High-Voltage Switching Circuit for Telephone Handset

connected across the telephone loop. The 4.8 µA drawn from the -48-V central office battery is acceptable in most telephone systems; however, if necessary, a 50-MΩ resistor may be substituted for the 10-MΩ resistor without any significant deleterious effect. Normally, when the handpiece is on the hook, Z1 is shorted to ground by the hookswitch. This hookswitch, by the way, carries only this extremely small current and thus can be a very low-cost item without any of the mechanical precautions needed for switching telephone loop currents. When the hookswitch is opened, 10 V from Z1 is applied to the gate of transistor Q9, turning it on. Q9 provides two functions. First, it allows sufficient current to be drawn through the 4.7-kΩ resistor, R4, to tell the telephone exchange that the receiver is off the hook, thus stopping the ring and providing a dial tone. Second, Q9 causes current to be pulled through Z2 and R3, turning on the p-channel transistor, Q11. When turned on, Q11 allows the telephone loop current to pass through the 3.9-kΩ resistor, R5, and into the 5-V zener diode, providing a 5-V power supply for all the parts of the handset circuit that require it. If this is primarily low-current-drain CMOS logic, adequate current should be available, although a more elaborate voltage regulator could be provided.

The 5-V supply powers the two CMOS inverters, I1 and I2, which act as a 2 MHz oscillator. (This oscillator will work only with the exact components called out; different resistors or capacitors might be needed with substitute parts.) The outputs from this oscillator power the four resistor diode networks that produce approximately 8 V to drive the gates of Q2, Q4, Q5, Q6, and Q7. The nand gates in front of the networks driving Q2 and Q4 are gated by sensing

signals obtained from the polarity of the incoming telephone lines, so Q4 and Q2 act as highly efficient rectifier diodes. Q5 and Q6 are depletion-mode or normally-on transistors which allow ring signals to come through the ring signal detector. (Capacitive coupling is used to the ring detector.) When the power supply is brought up, Q5 & Q6 are turned off, and from then on, the ring detector is disconnected. Transistor Q7 serves the function which most nearly replaces the original switch hook function. When the power supply comes up, it turns on, connecting the speech circuit (another name for the hybrid) to the telephone lines. Finally, when the 5-V power supply comes up, Q12 turns on, giving a low output to the microprocessor start pin and telling the microprocessor that it can safely commence functioning.

One of the first controller functions is to initiate dialing. This can be done using tone dialing, using a DTMF generator placed across the telephone lines (as shown in Figure1), or by using pulse dialing in which case logic signals are applied to the dial pulse input pin. This turns off the current to the power supply, causing the current from the loop to be low enough to register as a dial pulse at the exchange. To keep the power rail from dropping to zero, Q13 is used to shut down the oscillator temporarily so that it does not drain more current from the 10-μF power supply capacitor. Meanwhile Q2, Q4, Q5, and Q6 are maintained in their states for the 100-ms pulse by the 0.1-μF capacitors placed between gate and source. Thus, the immediate effect of a dial pulse input is to turn off Q7 and Q9, so that no more current is drawn from the loop while the rectifier bridge and ringer disconnect switches are unaffected. The application of a logic signal to the forced off-hook terminal when the hookswitch is closed turns on Q9 and the 5-V power supply regardless of the state of the hookswitch.

Application of a 5-V signal to the recall pin simply turns on the recall switch, Q8, regardless of the state of the rest of the circuit.

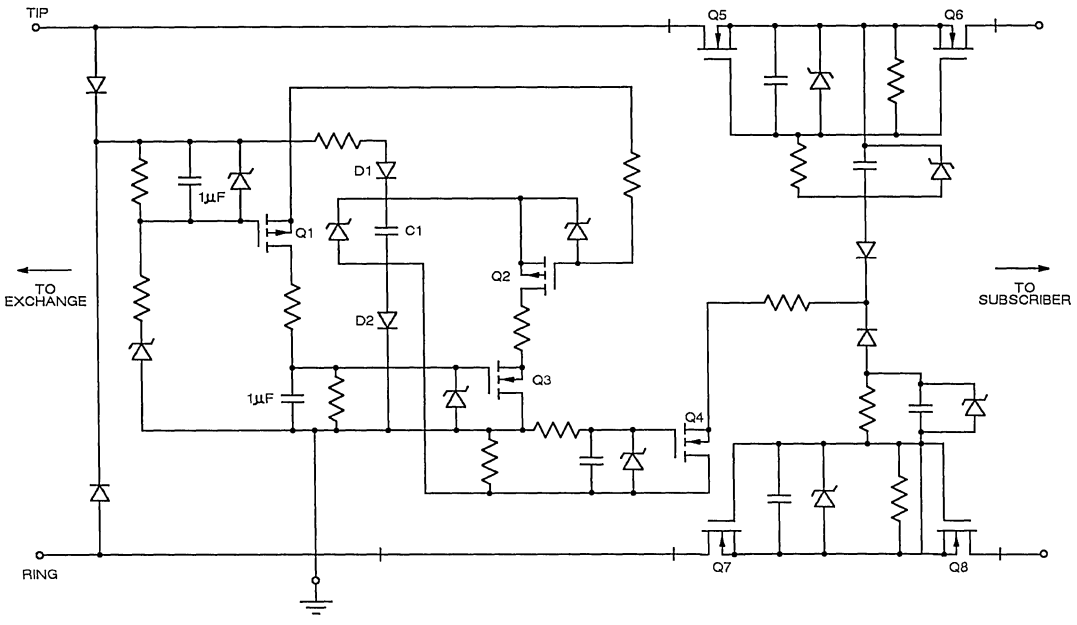
The switching circuit closely mimics the functioning of the mechanical switches in a traditional telephone. When an off-hook condition is detected from the hookswitch or commanded by the controller, current is drawn from the loop and the speech circuit is connected to the telephone loop. Application of dial pulses to the dial pulse input causes momentary current cessations to simulate pulse dialing. The polarity guard rectifies the incoming signal with no voltage drop, producing an output with constant polarity, regardless of misconnections. The circuit produces a 5-V power rail for operation of the entire system, and sends a low signal to the microprocessor when this has been achieved.

The Remote Isolation Device (RID)

A remote disconnect circuit is shown in Figure 3. Several types of remote disconnect circuits are employed internationally. In the U.S., the Bell System uses a device called a maintenance termination unit or MTU, which uses TRIACS to momentarily disconnect the customer during line testing. In Europe, a remote disconnect circuit is planned to both disconnect the customer and send a standard-test tone on the line to the exchange. Independent telephone companies in the U.S. call their circuit a remote isolation device.

Each of these circuits has slightly different triggering conventions. It is critical to avoid accidental triggering, so these circuits use a sustained positive voltage that is larger than normally encountered in regular telephone service. The circuit described here uses a 1-s, +130-V signal to either tip or ring to activate the device. The circuit must not be triggered by brief transient voltages above this level, like those associated with longitudinal pickup or ringing signals. In addition, it must be essentially transparent to all the normal telephone signals.

Figure 3 shows that when a positive voltage above ground potential is applied to either tip or ring, it is steered by the diodes to the top end of capacitor C1, charging it up to the line potential. If the voltage exceeds 90 V for more than a second, Q1 turns on, which, in turn, turns on Q3. If the voltage is then reduced, diode D1 will reverse bias as the line voltage decreases below the voltage on C1. When the reverse bias exceeds 2 V, Q1, a p-channel device, is biased on. When this happens, the potential of the node at the top end of C1 is abruptly pulled down to either the new line potential or ground, whichever is more positive. The potential on the lower side of C1, which is now large and negative, is then applied through Q4 to the gates of Q5, Q6, Q7, and Q8, turning off these depletion-mode transistors. Q4 ensures that there is no path to ground from tip and ring through D2 when the switching mechanism has not been triggered. The resistor diode network associated with the sources and gates of Q5, Q6, Q7, and Q8 ensures that charging the 1-μF capacitors is not prematurely terminated by turning off the switches.



Q1	VP2410L	Q5	ND2406 Depletion Mode	All Diodes have >300 V Breakdown
Q2	VP2410L	Q6	ND2406 Depletion Mode	
Q3	VN2010L	Q7	VN2406 Depletion Mode	
Q4	VN2010L	Q8	VN2406 Depletion Mode	

Figure 3. Remote Isolation Device Circuit

The circuit will respond to a 1-s, +100-V or greater potential on tip or ring by turning off both switches for approximately 10 s. It is not triggered by transient pulses above 100 V, nor by sharp pulses or noise on the line, and it is not affected by the normal negative voltages used in telephone service. When the +135-V signal is applied, the disconnect does not occur until the voltage is reduced below the original level. Once triggered, the disconnect cannot be negated by the application of other potentials, even if they are greater than 130 V. The functioning is not affected if tip and ring are interchanged.

Conventionally, telephone companies place a recognizable impedance across the line in front of the remote isolation device. This is frequently a diode in series with a 400-kΩ resistor, so the variation of impedance with polarity can be observed when the customer has been disconnected.

Those who plan to build a remote isolation device should consult the detailed network requirements of the telephone companies involved to make sure that all applicable regulatory requirements, such as those imposed by the FCC, are met. The circuit shown here requires a resistor and varistor protector to protect it against overvoltages in excess of 240 V, such as those associated with a power cross where a power line touches the telephone line.

The low-power MOSFETs that provide all the basic high-voltage switching functions for the telephone set and the RID circuits presented in this article are available from Siliconix. In addition to standard enhancement-mode MOSFETs, we also offer depletion-mode options that provide a convenient interface with the economical gate-drive circuits used in many telephone systems. Siliconix has a well-established history as a supplier of rugged, high-voltage MOSFETs for the worldwide telecommunications industry.

P-CHANNEL MOSFETS THE BEST CHOICE FOR HIGH-SIDE SWITCHING

Ed Oxner
Central Applications

Historically, p-channel FETs were not considered as useful as their n-channel counterparts. The higher resistivity of p-type silicon resulting from its lower carrier mobility put it at a disadvantage compared to n-type silicon.

Getting n-type performance out of p-type FETs has meant larger area geometries with correspondingly higher inter-electrode capacitances. Consequently, a truly complementary pair — a p-channel and an n-channel device that match in *all* parameters — is impossible.

Another obvious shortcoming is that, despite the availability of low-threshold devices, no p-channel MOSFET is "logic compatible."

Yet, despite its shortcomings, the p-channel MOSFET performs a vital "high-side" switch task that the n-channel simply cannot equal.

Used as a high-side switch, a p-channel MOSFET in a totem-pole arrangement with an n-channel MOSFET will simulate a high-current, high-power CMOS (complementary MOS) arrangement. Although the p-channel MOSFET cannot complement the n-channel in both on-resistance and capacitance simultaneously, such combinations as the low-threshold p-channel TP0610 and the n-channel 2N7000 together offer outstanding performance as a complementary pair.

CIRCUIT APPLICATIONS

Switching Ground-Return Loads

The principal application of the p-channel, enhancement-mode MOSPOWER FET is in switching power (or voltage) to grounded (ground return) loads.

To drive the FET properly, the gate voltage must be referenced to its source. For enhancement-mode MOSFETs, this gate potential is of the same polarity as the MOSFET's drain voltage. To turn on, the n-channel MOSFET requires a positive gate-source voltage, whereas the p-channel MOSFET requires a negative gate-source potential.

During switching, a MOSFET's source voltage must remain fixed, as any variation will modulate the gate and thus adversely affect performance. Figure 1 shows this degradation by comparing n-channel and p-channel MOSFET high-side switching.

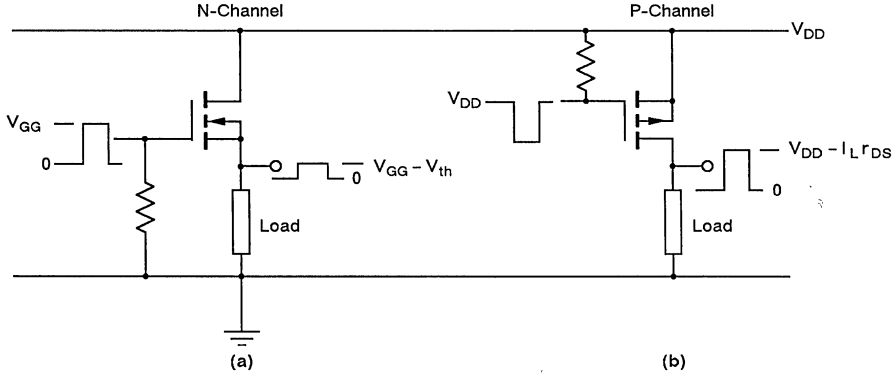


Figure 1. Comparing the Performance Between N-Channel and P-Channel Grounded-Load Switching

If an n-channel, enhancement-mode MOSFET were switching a positive-polarity voltage to a grounded load, the output would be limited to $V_{GG} - V_{th}$.

The equations describing performance of the n-channel ground-switching MOSFET with a ground-reference gate drive are based on the relationship between V_{DD} and V_{GG} :

If $V_{DD} \geq V_{GG}$, then $V_O = V_{GG} - V_{th}$;

If $V_{DD} < V_{GG}$, then $V_O = V_{DD} - I_L r_{DS(on)}$.

Sustaining a more acceptable gain with an output in direct relation to V_{DD} would require an isolated gate drive referenced to the source, as shown in Figure 2.

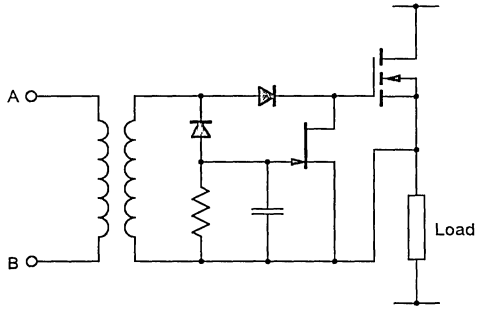


Figure 2. Floating Gate Drive

Bootstrapping the n-channel MOSFET (see Figure 3) is quite satisfactory for short turn-on times of a few milliseconds. In this arrangement, both MOSFETs must have breakdown voltage specifications that match or exceed the rail voltage.

Using a p-channel MOSFET in the configuration shown in Figure 1(b) may place some severe restraints upon the gate drive, since the gate must be close to V_{DD}. To return gate control to a more acceptable logic format, add an n-channel MOSFET as shown in Figure 4.

Using an n-channel MOSFET in this way simplifies the gate drive for a high-voltage, high-side, p-channel MOSFET. Placing a Zener diode between the gate and rail ensures that $V_{(BR)GSS}$ will not be exceeded. Again, both MOSFETs must withstand the full rail voltage.

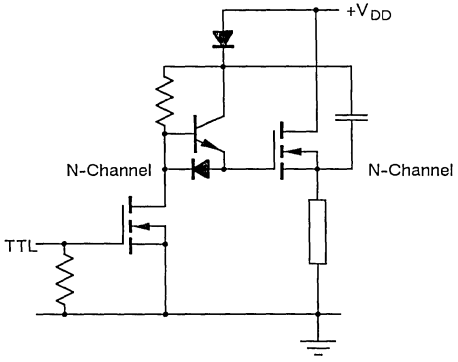


Figure 3. Bootstrapping for N-Channel Ground-Loaded Switching

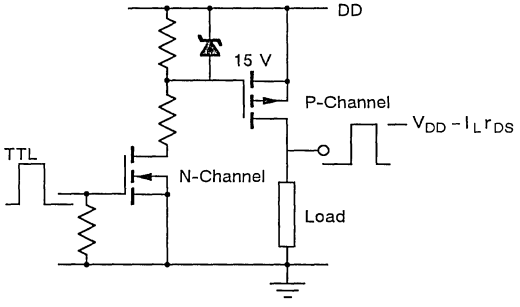


Figure 4. Using an N-Channel Level-Shifter Simplifies Driving from Logic

Half-Bridge (Totem Pole)

The high-side p-channel MOSFET coupled to a low-side n-channel MOSFET with common drains (shown in Figure 5) makes a superb high-current "CMOS equivalent" switch. One fault common to such circuits has been the excessive crossover current during switching that may occur if the gate drive allows both MOSFETs to be on simultaneously.

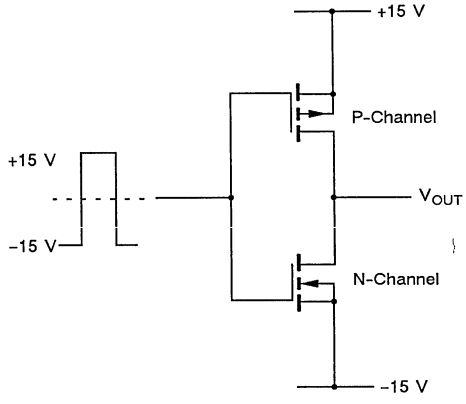


Figure 5. Low-Voltage Complementary MOSPOWER Array

At high rail voltages (both $+V_{DD}$ and $-V_{DD}$), properly driving the MOSFET gates can minimize unwanted crossover current, as Figure 6 shows. When the output stage uses high-power MOSFETs, a resistively-coupled lower-power complementary pair offers extremely low crossover current. The Zener, Z1, and resistors, R1 and R3, act as a level shifter, properly driving the low-power MOSFETs. The Zener may be selected according to the equation

$$V_{ZENER} = 2\,V_{DD} - \left|V_{th}\right|$$

where $+V_{DD} = -V_{DD}$

Whatever crossover current that might occur in the low-power drivers is dramatically reduced by the series resistor, R4. Additionally, driving the high-power complementary pair using this resistor divider scheme all but eliminates crossover current in this critical output driver. This increases both the driver's efficiency and its reliability.

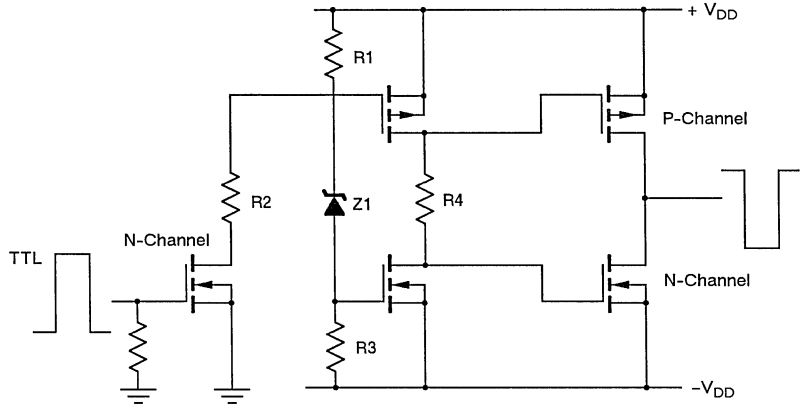


Figure 6. High-Voltage Complementary Pair Driven by Logic-Compatible MOSFET

DEPLETION-MODE MOSFETS EXPAND CIRCUIT OPPORTUNITIES

Ed Oxner & Richard Bonkowski

INTRODUCTION

A principal advantage of the depletion-mode MOSFET is its ability to perform at higher operating voltages than its JFET counterpart. As a depletion-mode structure, the MOSFET permits the added flexibility of allowing the gate potential not only to be higher but to be of either polarity. Earlier, small-signal MOSFETs were classed as being quite sensitive to ESD. With the introduction of the ND2020 and ND2410 series, sensitivity to ESD has been greatly reduced.

Perhaps the only short coming for the depletion-mode MOSFET is its higher-than-JFET noise performance. Where the JFET has been perceived as a "noiseless" transistor, the MOSFET does not share that renown.

Depletion-Mode vs. Enhancement-Mode

Three Classes of FETs

There are three classes of FETs, both n- and p-channel, that are identified by the mnemo A, B and C. Class A encompasses the whole field of junction FETs (JFETs). Class B includes those that are identified as depletion-mode MOSFETs, and Class C includes those recognized as enhancement-mode MOSFETs. Figure 1 illustrates the basic differences that distinguish the various classes and also demonstrates how these classes differ with respect to biasing.

In the symbols used in Figure 1, the solid bar identifies a depletion-mode FET (current conduction at zero bias); the broken bar identifies an enhancement-mode MOSFET (zero conduction at zero bias).

Note that although Class A and B are both classified as depletion-mode, Class B radically differs in that depletion-mode MOSFETs are also capable of performance in the enhancement-mode region. This distinction is only achievable for Class B. Although neither Class A (JFETs) nor Class C (MOSFETs) can perform beyond their respective mode, Class B – the depletion-mode MOSFET – is capable of operation in both modes!

Perhaps the simplest definition of depletion-mode operation is shown by the transfer characteristic (biasing) curves offered in Figure 1(b). Drain current is reduced to zero when the gate voltage reaches a critical cutoff voltage, opposite in polarity to that of the drain voltage. The n-channel JFET (or Class B MOSFET) has a positive-polarity drain voltage and is controlled by a negative-polarity gate voltage. Why the Class B MOSFET may also perform in the enhancement-mode is made clear by study of the structure.

The Structure of MOSFETs

All MOSFETs are classified as either depletion-mode or enhancement-mode. Although they can be fabricated as n- or p-channel, generally we find n-channel MOSFETs in either mode and p-channel MOSFETs available only as enhancement-mode devices.

There are, however, three fundamental styles of MOSFETs regardless of mode. The classic planar MOSFET, shown in cross-section in Figure 2, the short-channel double-diffused MOSFET (DMOS FET), shown in Figure 3, and the vertical power MOSFET, shown in Figure 4. The features of each style are distinguished by performance.

When viewing the cross section, the distinguishing feature that quickly identifies the mode is whether a diffused channel spans the gap from source to drain. No visible channel (Figure 2a, 3a, and 4a) identifies the enhancement-mode MOSFET.

The Performance of a Depletion-Mode MOSFET

Regardless if the MOSFET is n- or p-channel, the fundamental difference in performance focuses on whether the MOSFET is a depletion-mode or an enhancement-mode device. An important, but secondary difference lies in the style of MOSFET: planar, DMOS, or vertical. The principal differences are clarified as we study the transfer characteristics (biasing), shown in Figure 1.

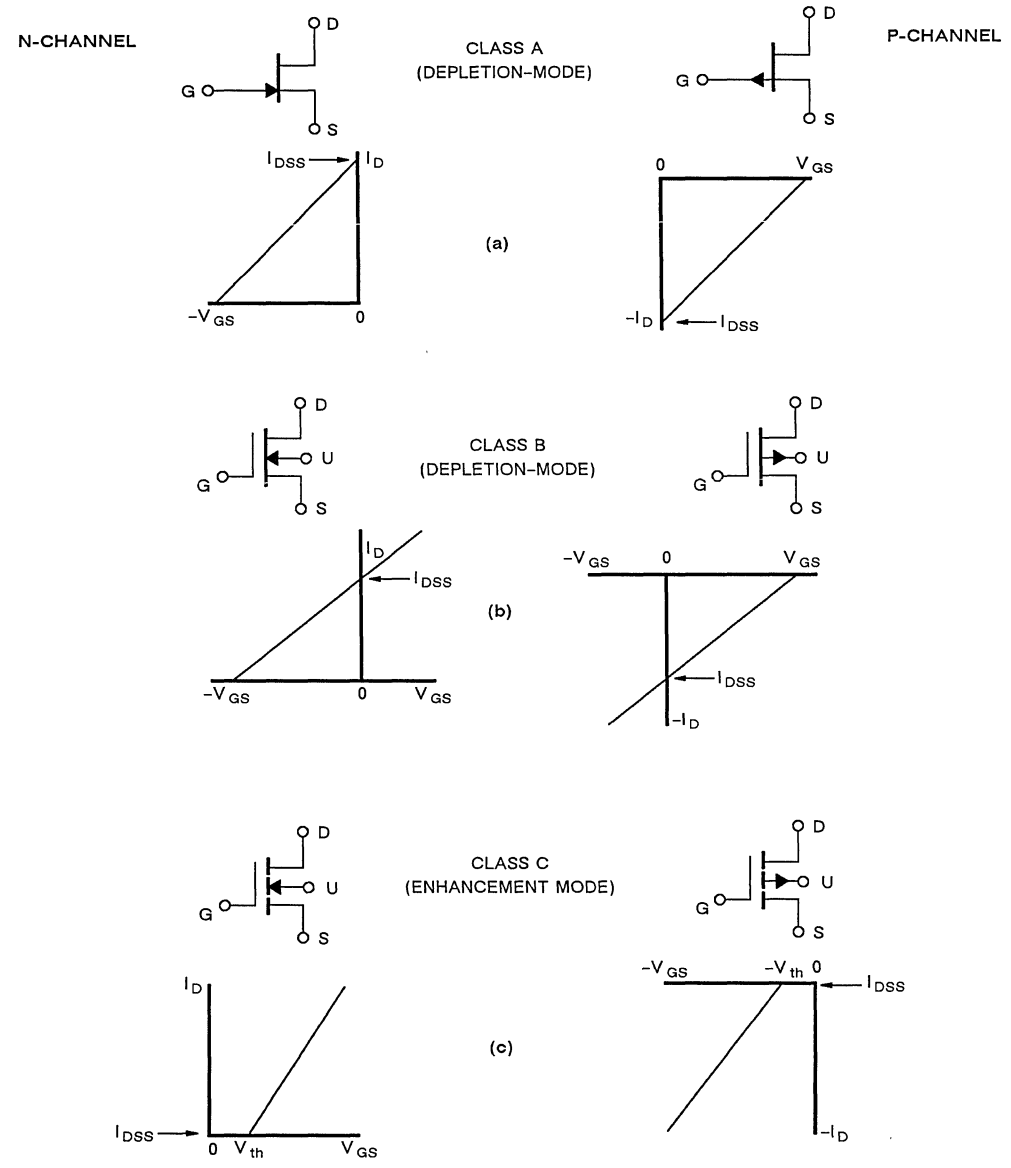
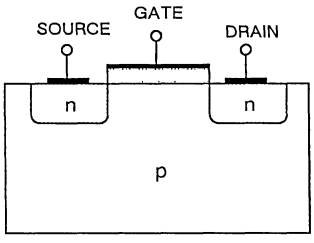
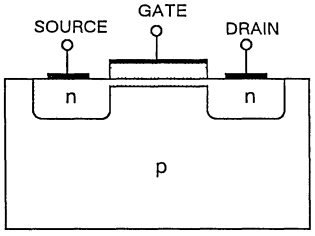


Figure 1. Classification of FETs

The transfer characteristics of the n-channel, depletion- mode MOSFET are shown in Figure 1(b). Because the gate is isolated (see Figure 2b), V_{GS} can be reversed without creating a gate current. The gate may be made either positive or negative with respect to the source. By allowing the gate-to-source potential to go positive and increasing the magnitude of gate voltage, additional free electrons will be attracted beneath the gate oxide further enhancing the diffused channel and allowing I_D to become greater than I_{DSS}!

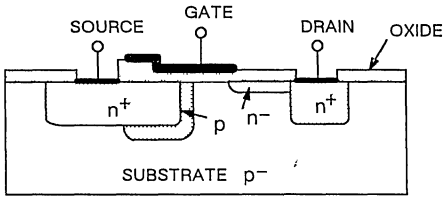


(a) Enhancement-mode

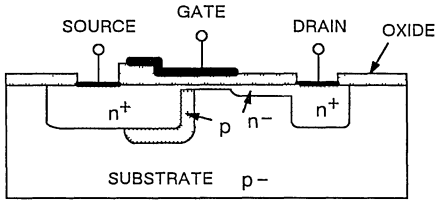


(b) Depletion-mode

Figure 2. Classic Planar MOSFETs

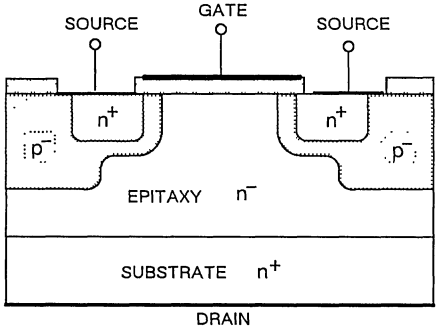


(a) Enhancement-mode

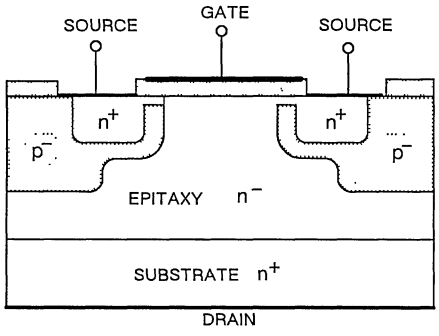


(b) Depletion-mode

Figure 3. Short-Channel Double-Diffused MOSFET



(a) Enhancement-mode



(b) Depletion-mode

Figure 4. Vertical Power MOSFET

This mode of operation results in a unique series of output characteristics where, for the n-channel depletion-mode MOSFET, we see near-linear performance in what appears as the enhancement region. This performance is shown in Figure 5. The foregoing establishes that the depletion-mode MOSFET is a "normally on" device; that is, when V_{GS} = 0, I_D = I_{DSS} . When a normally off device is needed, the enhancement-mode MOSFET is selected.

9

Applications For Depletion-Mode MOSFETs

As a Current Regulator

The ideal current source supplies a fixed current to a load independent of the impressed voltage. Such a source would exhibit zero output conductance. Aside from the fact that depletion-mode MOSFETs can handle higher voltages and greater currents than most JFETs, they exhibit two characteristics which provide near-ideal performance as a current regulator. First, when the impressed voltage exceeds pinchoff, V_P , the saturation characteristics exhibit near-constant current (low output conductance) over a wide voltage range (see Figure 5). Second, performance as a depletion-mode transistor allows for simplified biasing to achieve the desired results.

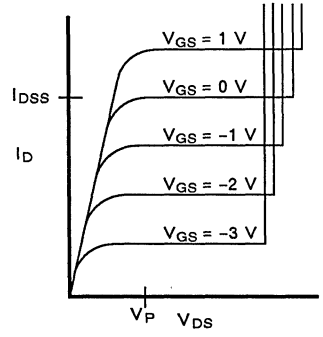


Figure 5. Output Characteristics N-Channel Depletion-Mode MOSFET

Basic Regulator Circuit

For a given device where I_{DSS} and $V_{GS(off)}$ are both known, the value of bias required to establish the regulating current may be approximated by

$$V_{GS} = V_{GS(off)} \left(1 - \frac{I_D}{I_{DSS}}\right)^{1/2} \quad (1)$$

The biasing resistor, R_S, required in the source of the MOSFET is

$$R_S = \frac{V_{GS}}{I_D} \quad (2)$$

A change in either supply voltage or load impedance will change the regulating current in proportion to the magnitude of the output conductance of the MOSFET.

$$dI_D = {}^{d}V_{DS}\, g_{os} \quad (3)$$

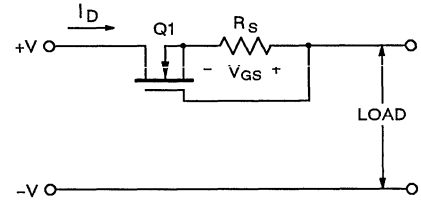


Figure 6. Basic Regulator Circuit

A typical constant-current regulator circuit that employs a depletion-mode MOSFET is shown in Figure 6. As with any depletion-mode FET, the lower the ratio between I_D and I_{DSS} the better the regulation, as shown in Figure 7 and Table 1.

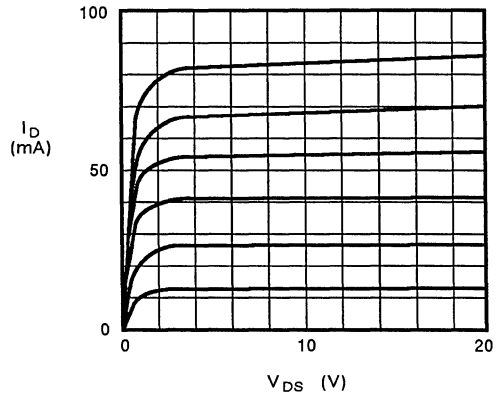


Figure 7. Output Characteristics of a depletion-mode MOSFET

Table 1

$\frac{I_D}{I_{DSS}}$	% Regulation
0.02	0.5
0.05	1.0
0.10	1.5
0.20	2.5
0.30	3.5

Extending Power Level Using MOSPOWER

The n-channel, depletion-mode MOSFET can be used in conjunction with an enhancement-mode power device to give an appreciable boost to the power handling capability of a current regulator. Such a power regulator circuit is shown in Figure 8, where both the operating voltage and regulating current are set by the selection of the MOSPOWER FET, Q2. Regulation may suffer somewhat when using large MOSPOWER FETs due to the higher g_{OS} typical of large power FETs. Q2, operating in the linear mode, will, in all likelihood, require a heatsink. The basic regulator circuit, Q1 and R_S, is used to establish a small bias current that, in conjunction with R1, sets the bias level for the enhancement-mode MOSPOWER FET.

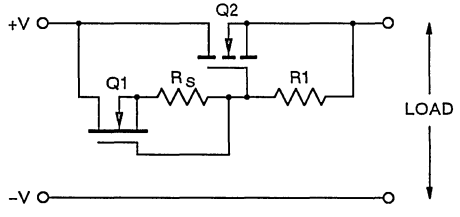


Figure 8. Extended-Range Current Limiter

A Simple Regulator for Telecom

Modern telephone handsets are steadily increasing their electronic content. Useful features, such as a memory to retain the last number dialed, require constant voltage to retain the information in memory. Typically, small memory ICs require only a few microamperes at 3 to 4 V to perform. This sustaining voltage must be available at all times, even when the phone is inactive or "on hook." Some handsets use a small battery cell to fill this need, while other designs use the -48 V which is available from the telephone line.

To utilize the incoming line, one needs to reduce the voltage and loosely regulate it, without consuming much power. In most systems, current drain in excess of 10 to 15 μA will alert the central office to an "off hook" condition and the subscriber's phone is presumed "busy." A simple depletion-mode regulator using the ND2410 can satisfy these requirements very economically. As shown in Figure 9, the depletion-mode MOSFET is used in a current-regulator mode to supply 10 μA to a 500-kΩ load. This establishes a voltage of 5-V to power the memory circuit. If the memory requires 2 microamperes, only 8 μA will flow through the resistor, and the voltage drops to 4 V, which is sufficient to sustain the memory. Should the telecom line rise to 60 volts, the current regulator continues to supply a fixed 10 μA to the load; the surplus voltage is dropped by the MOSFET. The regulation is not precise, but more than sufficient to provide a simple and reliable solution. Alternatives such as 3-terminal bipolar regulators require high bias currents (over 1 mA) and are not readily available to sustain the high voltages necessary for use on telephone lines.

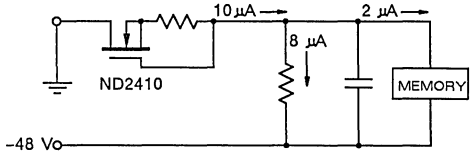


Figure 9. Telecom Voltage Regulator for Memory - Resident Redlaling

As a Switch

When considering a switch, we usually select one whose natural, quiescent state is either normally-on or normally-off. With no applied power (or voltage), the depletion-mode MOSFET is normally-on.

Improving the dV/dt of Thyristors

The ND2410 can be used very effectively in power SCR circuits to improve the critical dV/dt rating. Spurious turn-ON of an SCR caused by dV/dt can result in permanent damage to an SCR or an out-of-sequence turn-ON that can have disastrous effects in high-powered phase-control equipment.

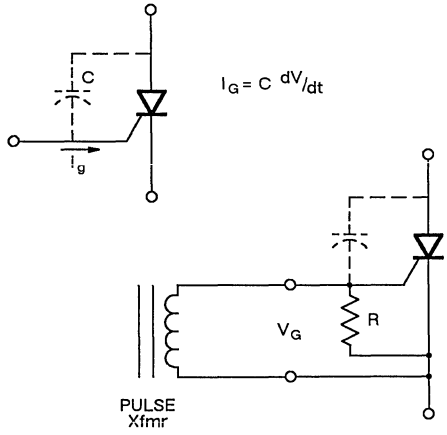


Figure 10. dV/dt Triggering of SCRs

Traditionally, SCRs fired by pulse transformers have used a resistor from gate to cathode to shunt false gate signals caused by dV/dt as shown in Figure 10. This method requires a large wattage resistor, since the normal gate trigger signal is also applied across the resistor. The resistor, therefore, shunts part of the normal gate current, thus reducing the signal available for adequate turn-on of the SCR. The ideal solution would be a shunting resistor that seems to disappear when a normal gate signal is applied.

Just such an effect can be achieved using the normally on feature of the ND2410 as shown in Figure 11. With no gate pulse applied, the depletion-mode transistor is "on" with an equivalent resistance of about 10 Ω. When the gate current is applied, the voltage drop across R_{GS} turns the transistor off, allowing all of the gate current to flow through the SCR gate.

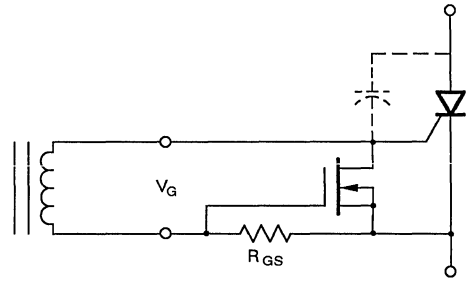


Figure 11. Depletion Mode Active Shunt

Since the MOSFET turns off in a few nanoseconds, it has very little effect on normal SCR operation. In an actual experiment, the dV/dt of a 25-A SCR (similar to a 2N692) was improved from 300 V/μs (with no gate shunt network) to 2000 V/μs with the depletion-mode shunt.

Some suggestions for effective operation:

1. Use a fast-rising gate pulse: $I_G > 3 \times I_{gt}$
2. The shunt should be located as physically close to the SCR gate terminal as possible to reduce the winding inductance and noise pick-up from long gate wires.
3. $R_{GS} \geq \frac{V_{GS(off)}}{I_G}$
4. Do not use with non-isolated gate drive circuits; a pulse transformer should be used.

APPLYING MOSFETS IN LOW VOLTAGE CIRCUITS

Richard L. Bonkowski

INTRODUCTION

The application possibilities for low-power MOSFETs are so numerous that they often are suitable for use in low-voltage circuits (5 to 15 V) as replacements for bipolars or as switches driven by digital integrated circuits. Lamp and relay drivers, small motor controls, and stand-by power-transfer switches are just a few of these popular low-voltage circuits. These applications deserve special consideration as they highlight one of the important differences between MOS and bipolar technology: MOS is voltage controlled, while bipolar devices are current controlled. Applying MOSFETs in these low-voltage circuits is greatly simplified by the availability of low-threshold MOSFETs from Siliconix.

Transfer Characteristics

To better understand the performance of MOSFETs in low gate voltage applications, one can examine the transfer characteristics of a typical device shown in Figure 1.

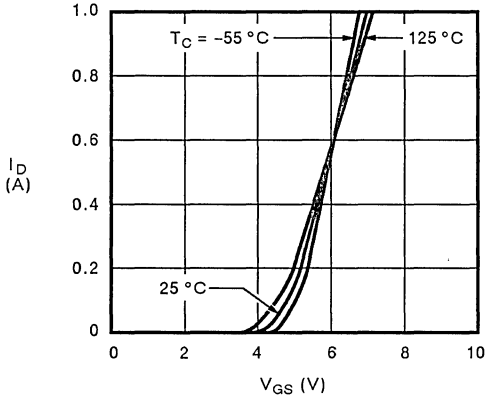


Figure 1. Normalized Transfer Characteristics 2N6786

To realize the full rated I_D current, a gate drive of approximately 7 volts is required. At the typical "high" state output of a TTL gate (3 to 4.5 V), this transistor could be completely "off" or, at best, conducting only 10 or 20% of rated current. A curve for a Siliconix low-threshold transistor, the 2N7000 FETlington, is shown in Figure 2.

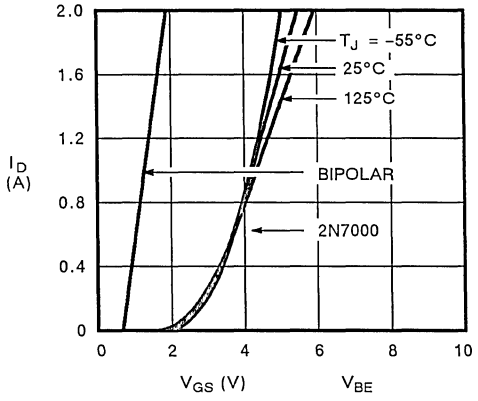


Figure 2. Normalized Transfer Characteristics 2N7000

At TTL drive levels, this device can conduct 40 to 100% of its rated current. It should be noted that TTL is normally considered to be "5-V logic," but practical available gate drive is generally to 4.5 V. If the transfer characteristic of a small bipolar transistor was shown on the same scale as the 2N7000, one could see the relative independence of collector current once a base voltage level greater than 0.7 V is applied.

Benefits of Low V_T

Siliconix low-threshold MOSFETs offer the user a real advantage in applying the benefits of low losses and high switching speed to low-voltage circuits. At low switching frequencies, the gate drive power required by MOSFETs is virtually nil, compared to the 1 mW or more required by comparable bipolars. Because MOSFETs are essentially resistive in the "on" state, conduction losses can be significantly less for MOS than for bipolar devices.

Logic-Level Applications

TTL Gate Drives

While TTL gates operate from 5 V, the typical voltage available at a gate output is 3.5 V. This is clearly insufficient to drive a normal MOSFET whose threshold voltage can be 4.0 V. Low V_T MOSFETs can sometimes be used in such applications, if only a small fraction of their rated current is needed or a higher $r_{DS(on)}$ can be tolerated. A a better solution is to use open-collector TTL and a pull-up resistor to the 5-V bus, as shown in Figure 3a.

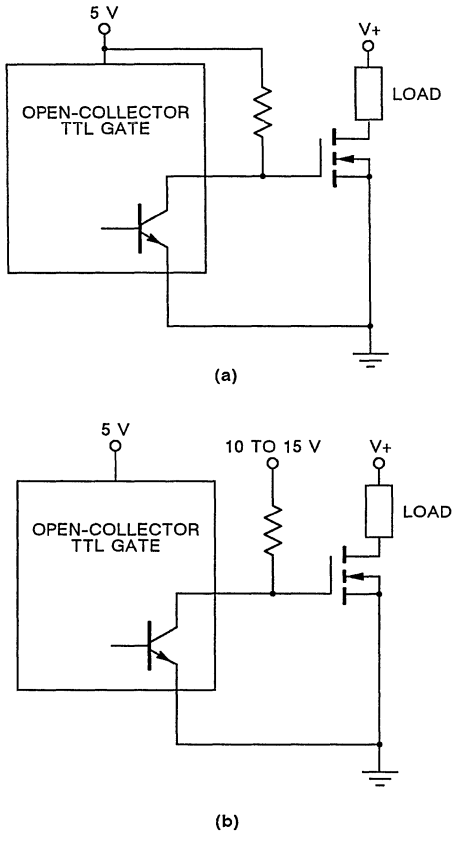


Figure 3. Open Collector TTL Gate Drive

This technique will provide a greater drive voltage, and the designer can use the data from Siliconix data sheets showing the $r_{DS(on)}$ for 4.5-V gate drive. Of course, open collector TTL, connected to a 10- or 15-V supply (Figure 3b) is an even better solution, allowing the designer to achiever even greater turn-on of Siliconix low V_T MOSFETs or use of our normal threshold MOSFETs.

The designer should also bear in mind that the switching speed of the MOSFET is dependent on the gate driver's ability to source and sink peak current to charge and discharge the input capacitance of the FET. Typical TTL can source about 1.0 mA per gate and sink about 10 mA. For very high-speed applications or to drive large MOSFETs, an intermediate buffer may be needed. For a more complete discussion of gate drive requirements, see the Siliconix MOSPOWER Data Book (1988), page 9-18.

CMOS Gate-Drives

Because CMOS logic can operate from 10- or 15-V supplies, it seems more naturally compatible with MOSFET transistors. While this solves the V_{GS} problem, speed can still be an issue as CMOS gates usually switch slower than TTL. CMOS gates are also limited in source and sink current, but may be paralleled if additional drive is needed. External buffers may be used with CMOS, as previously suggested for bipolar TTL.

Low-Voltage Circuits

Circuits powered by batteries are of particular interest for MOSFET applications. Because MOSFETs can be more power efficient than bipolars, they can be used to great advantage in battery powered applications.

In 12-V circuits, conventional MOSFETs are readily applicable. At lower voltages (eg. a 6-V Ni-Cad source) or at low temperatures in automobiles (cold-cranking can drop the battery voltage to 5 V), the designer must be aware of gate drive conditions. For the 12-V "cold cranking" situation or a 6-V Ni-Cad near discharge (5 V), the $I_{D(ON)}$ and $r_{DS(on)}$ data at 4.5 V is particularly important.

Figure 4 shows a typical automotive application for a "high-side switch" or solid-state relay. The gate voltage for the high current MOSPOWER switch is supplied from a voltage doubler IC (Si7661). To prevent activation of a load under low battery conditions, Q2, a low-threshold 2N7000 prevents Q1 from turning on, even if only 4.5 V of gate control is available from a cold battery. If Q1 could not be held off, control of a non-essential load (lights, radio, etc.) might be lost, further burdening the battery during starting.

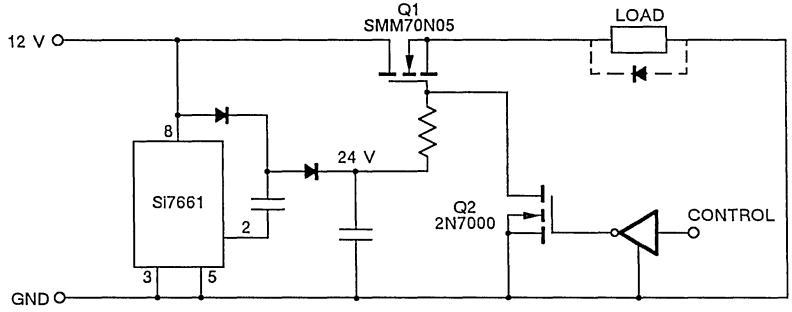


Figure 4. Automotive High-Side Switch

Low-Threshold P-Channel MOSFETs

Most of this discussion has focussed on n-channel transistors because of their wide selection, low cost, and better availability. High-side switches, as shown in Figure 5, can be easily implemented with p-channel MOSFETs and open-collector or open-drain logic at low-voltage levels.

Figure 5 High-Side P-Channel Switch

The threshold of the p-channel is not usually critical unless the supply voltage is very low. With a 12-V supply and a 4-V threshold, 8 V are available to enhance conduction of the FET. If The supply were only 5 V, the enhancement would be minimal and $r_{DS(on)}$ would be very high. A low-V_T transistor, such as TP0610, should be used in this case.

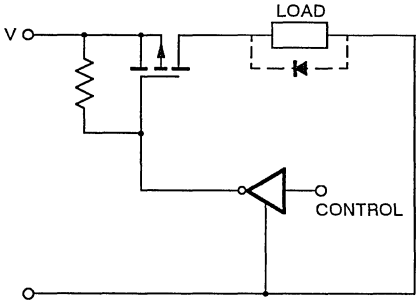


Figure 5. High-Side p-Channel Switch

Design Considerations

When using low-threshold MOSFETs, one should be aware of the changes in V_T due to environmental conditions. At high temperatures, V_T decreases. A device with a 1.0-V threshold at 25 °C might drop to 0.5 or 0.6 V at 150 °C. Under these conditions, the MOSFET could gate-on due to electrical noise or fail to switch off if the pull-down circuit cannot drop V_{gs} to a low enough value. Operation in an environment susceptible to radiation (e.g., x-rays) can permanently depress V_T, resulting in false turn-on due to noise or depletion-mode operation, that is, a normally-on state requiring a negative gate voltage for turn-off.

When comparing MOSFETs, be aware that some manufacturers achieve low V_T through the use of thinner gate oxides. This lowers the maximum gate voltage rating of the transistor (Siliconix parts are all rated for at least ±20 V and makes them more susceptible to ESD (electrostatic discharge) damage. Transistors rated at ±15 V maximum gate voltage should be used and handled with proper caution.

CONCLUSIONS

Understanding and attention to proper gate drive is essential for successful application of MOSFETs. In many instances, low V_T Siliconix MOSFETs are a ready solution to achieve economical circuit design where limited gate drive is available. The following table shows some of the more popular Siliconix low-threshold parts and their performance with gate signals of 5 V or less.

Table 1 Siliconix Low Threshold MOSFETs

Part Number*	$V_{(BR)DSS}$	V_T (MAX) (V)	Low V_{GS} Performance $r_{DS(ON)}$ (Ω)	V_{GS} (V)
VN0300	30	2.5	3.3	5
VN0610	60	2.5	7.5	5
VN10	60	2.5	7.5	5
VN2222	60	2.5	7.5	5
VN66	60	2.5	5	5
VN67	60	2.5	5	5
VN80	80	2.5	5	5
2N6661	90	2.0	5.3	5
VN1206	120	2.0	10	2.5
VN1210	120	2.0	10	2.5
VN1706	170	2.0	10	2.5
VN2406	240	2.0	10	2.5

*Note: Only the first few significant digits are given for some part numbers. Each family consists of a variety of package options indicated by suffix letters. Package style determines the thermal performance of the product which, in turn, determines current and power capabilities. See the individual data sheets for complete performance data.

AN ULTRA-BROADBAND ANALOG SWITCH

Ed Oxner

Many TTL and CMOS-compatible analog switches are commercially available, but none operate usefully into the UHF region. The following instructions describe how to make one that does.

The heart of the ultra-wideband analog switch is the Siliconix SD210DE series of small-signal enhancement-mode double-diffused MOS (DMOS) FETs. This series features low on-resistance and low interelectrode capacitances--an unusual combination. In either a 50- or a 72-Ω system, the SD210DE DMOS FET provides reasonably low insertion loss when on and excellent off-isolation when off.

In this design, the "T" configuration (see Figure 1) was chosen for its optimum off-state performance over a wide dynamic and frequency range. The configuration uses a pair of DMOS transistors tied back-to-back; that is, with sources in common and the drains acting as the input and output. The shunting DMOS transistor contributes to the high off-isolation when the switch is off. The body terminal of each SD210DE is electrically tied to its respective source. As with any DMOS FET, tying the body to the source forms a body-drain diode across the MOSFET. In the SD210DE, body-drain diode conduction occurs at close to 0.5 V.

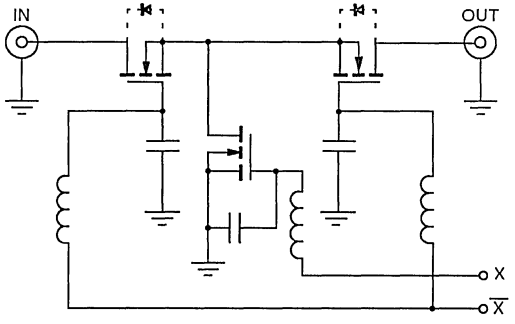


Figure 1. Electrical Schematic of Broadband Switch

A high dynamic signal (in this case, +10 dBm) across 50 Ω results in an rms signal voltage of 0.707 V. This would be sufficient to cause forward conduction through the body-drain diode irrespective of gate control, resulting in an off-isolation loss. Using a pair of DMOS FETs in the "T" configuration places one of the two diodes in opposition (i.e., in reverse conduction). As a consequence, the off-isolation remains unaffected. However, because of the body-drain diode's low forward conduction (approximately 350 Ω), in a 50- or 72-Ω system, the shunt arm of the "T" requires only one DMOS FET. This 350 Ω shunt has little effect on insertion loss.

Other options for limited dynamic range switching (besides the "T" configuration) include the popular "L" configuration and possibly a single DMOS transistor with the body terminal clamped to a negative supply.

Varying the gate voltage makes the DMOS transistor act as a wideband variable attenuator as well as an analog switch.

The switch's layout and assembly begins by selecting for the substrate a low-loss double copper-clad PCB (RT/Duroid 5870). Next, a 50-Ω (or 72-Ω) transmission line is etched onto this substrate, as Figure 2 shows. This line is suitably configured to accept the SD210DE.

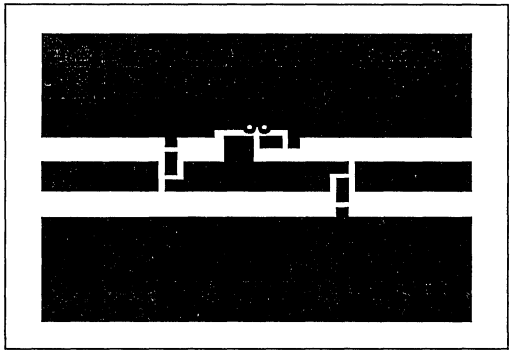


Figure 2. Circuit Board Mask (Top View) Showing Placement of SD210DE

Finally, each DMOS gate is bypassed and isolated using a combination of shunt capacitors and series RFCs (radio-frequency chokes). The shunting capacitors are chip capacitors (Varadyne 3BX050S393K -- 3.9 nF) and the RFCs are 10 self-supporting turns of #26AWG enamel magnet wire, each turn measuring 4.7 mm in diameter.

To drive the analog switch, simultaneously apply a logic HIGH (for turn-on) to the series DMOS gates and a logic LOW to the shunt DMOS gate. As the logic HIGH increases in potential, the r_{DS} of the DMOS transistor improves, resulting in a progressively improved insertion loss. Consequently, performance improves with 15-V logic as compared with 5-V logic, as Figures 3 through 6 show.

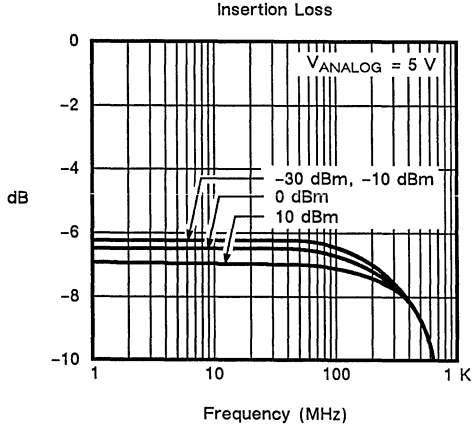


Figure 3. Insertion Loss for a SD210DE "T" Switch with a 50-Ω Input/Output and 5-V Logic

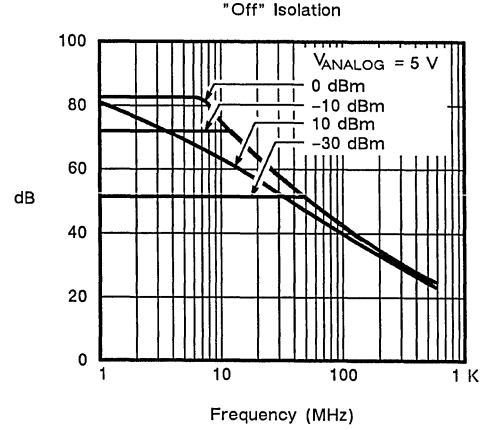


Figure 4. Off-Isolation for a SD210DE "T" Switch with a 50-Ω Input/Output and 5-V Logic

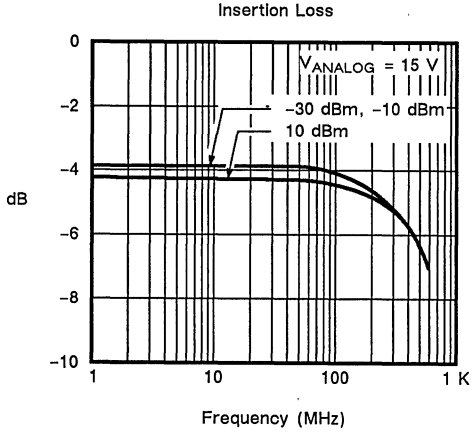


Figure 5. Insertion Loss for a SD210DE "T" Switch with a 50-Ω Input/Output and +15-V Logic

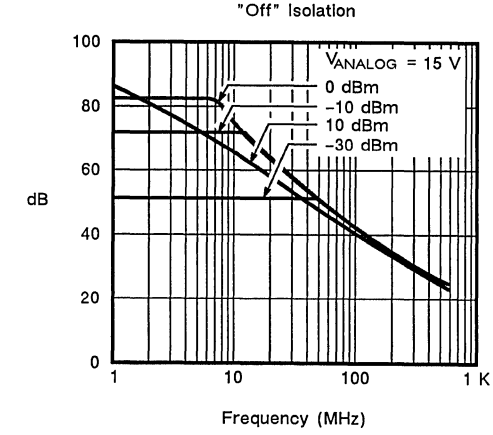


Figure 6. Off-Isolation for a SD210DE "T" Switch with a 50-Ω Input/Output and +15-V Logic

Because of the high gate impedance, the switch will remain in either state (on or off) when the logic is removed, provided that the gate-driving impedance is also extremely high. Performance decays with time, of course, depending upon cleanliness of the circuit board, and humidity.

The performance of this analog switch was measured using the Hewlett-Packard vector voltmeter, Model HP8405A, with its accompanying 50-Ω accessory kit, the HP11570A. The off-isolation tests were limited by the HP11570A's dynamic range and interchannel isolation. At signal levels of 0 dBm an +10 dBm, measurements to 70 dB were possible, but at lower signal levels the dynamic range was less. As a result of this dynamic range limit, the measured off-isolation was limited to −52 dB at a signal level of −30 dBm.

The apparent lack of off-isolation at high signal levels may partly be due to the layout. No shielding was attempted, even between the DMOS transistor's source and drain.

The performance curves in Figures 3 to 6 are, with these explanations, self-evident. The analog switch rolls off −3 dB at about 500 MHz.

Siliconix incorporated

A HIGH QUALITY AUDIO CROSSPOINT SWITCH

Bob Zavrel
Revised January 1988

INTRODUCTION

Recent advances in analog switch integrated circuits have made superior audio switch specifications possible. A crosspoint switch for the most demanding audio applications is described here. Although this switch may be used in recording studio and radio broadcast mixers where little compromise is acceptable, the low cost and small size makes this switch ideal for a diverse range of applications. Such applications can include audio crosspoint switches found in video systems, audio synthesizers, high quality multiplexers, and home entertainment systems.

A high quality audio frequency switch should have the following features:

1. Reasonable cost
2. Unity or variable gain
3. Very low harmonic distortion (< 0.01%)
4. Flat response (DC to > 1 MHz)
5. Low crosstalk
6. High OFF Isolation
7. Excellent phase linearity
8. High speed switching
9. Freedom from switch "popping"
10. Small size
11. Use of DC coupling only

The size of a complex audio switching array can be greatly reduced by using IC analog switches. The prototype array is an 8x2 stereo crosspoint switch mounted on a 4x7 inch board. Other switch configurations may be fabricated with little effect on the switch characteristics. This single board can replace a score of rotary switches and the bundles of audio cable often found in audio mixers. Furthermore, ground loop problems are reduced by eliminating the cable bundles.

Siliconix SD5002s were chosen because of low ON resistance, low switch capacitance, and very fast switching times. The LF347 quad op amp was chosen for its excellent audio characteristics in a quad package. Two LF347s are used in this switch providing a summing and output amplifier for each of four channels. Since the SD5002s switch into virtual grounds, they are held "normally open" by applying

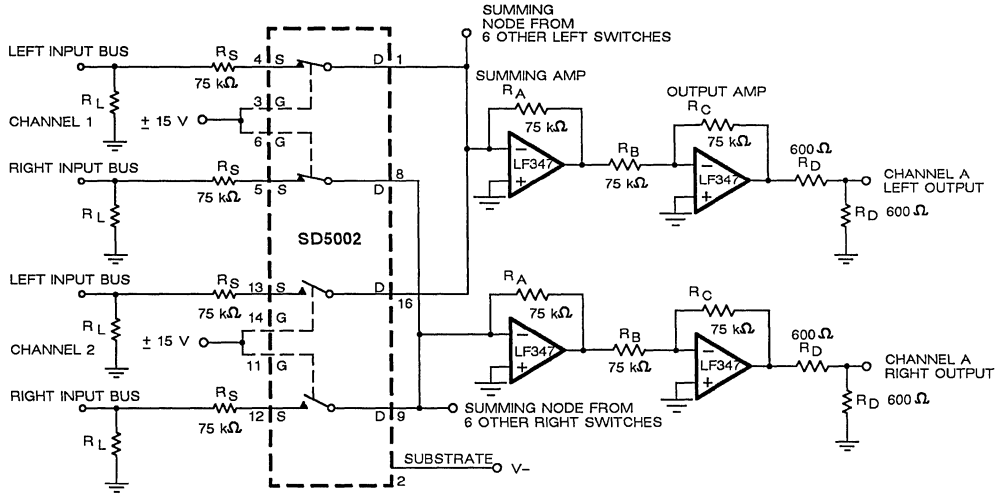


Figure 1.

–15 V to the switch gates. To turn them on it is sufficient to apply a V+ level to the gates. For any switch configuration, the appropriate switch(es) are closed by biasing the appropriate gate(s) to the positive voltage supply. In this circuit, pairs of switches are controlled together to affect the left and right channels of a stereo input simultaneously. This is accomplished simply by tying the applicable switch gates together and using a common bias.

Figure 1 shows how a single SD5002 is configured as a 2x1 stereo switch. Figure 2 shows how the circuit can be expanded into a switch matrix. Eight SD5002s are required to construct the 8x2 stereo matrix array. One R_L is required for each channel input for termination while four R_S's are employed to feed the signal from the swiitches to the amplifiers. Input buses are consequently formed in front of these resistors.

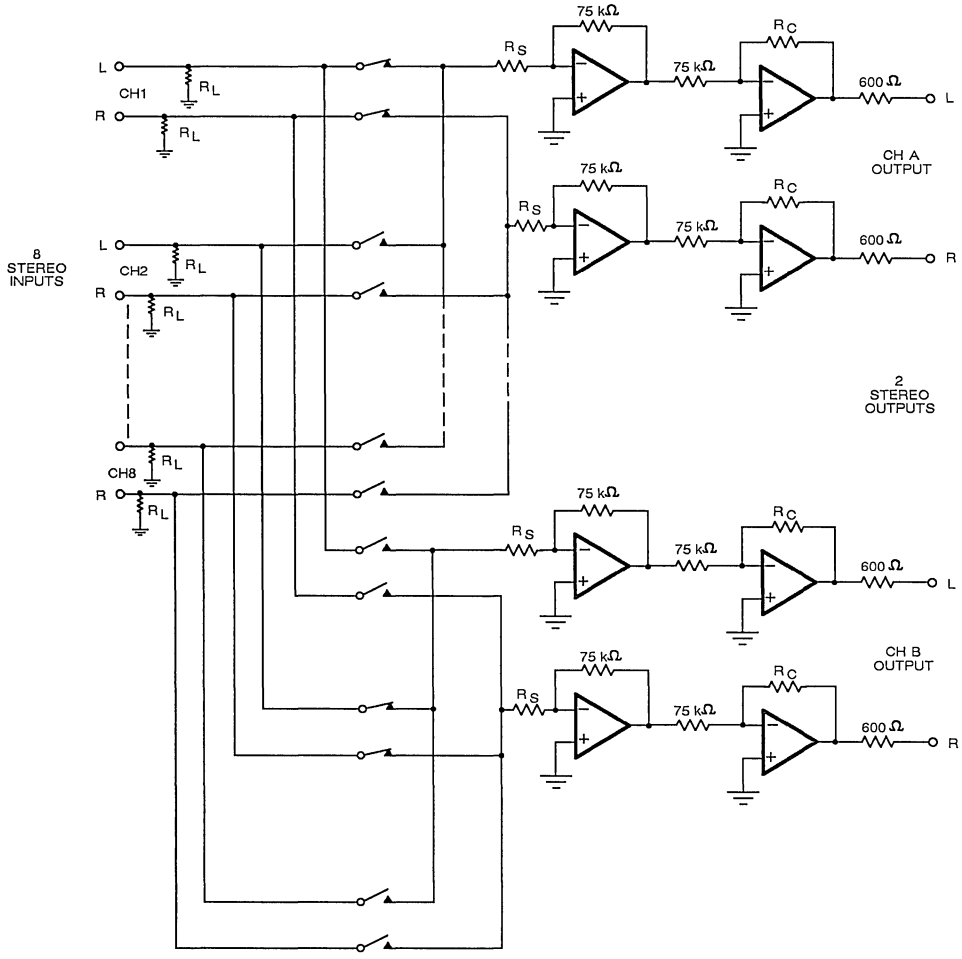


Figure 2. A High Quality 8 x 2 Stereo Crosspoint Switch

The SD5002 drains are connected to these input buses. A larger array will cause reduced system performance due to longer lead lengths and increased circuit capacitance. Nevertheless, large matrices can be configured with little performance compromise because of the low initial switch capacitance. R_L's value should reflect the value of the source impedance. Deletion of R_L will seriously degrade crosstalk and off isolation performance while lower values of R_L will improve these specifications. R_C may be adjusted for a wide range of system gain while a value of about 150 kΩ will set the circuit to unity gain. R_D sets the value of the output impedance and if the switch is to feed a high impedance load, R_O should be included to maintain system performance.

Electrolytic and mica capacitors are used on the circuit board for bypassing the two power supply voltages. Supply voltage bypassing will reduce both high and low frequency noise and help stabilize the system. The entire circuit should be well shielded particularly if it will be exposed to strong rf or power line fields. Conductors carrying high current should be kept away from the circuit. Double sided PC board should be used creating a ground plane on the component side as an additional precautionary measure.

Table 1 shows the switch performance of the 8x2 crosspoint configuration. R_L was set to 10 k Ω, reflecting the high impedance of the test oscillator's output. Regulated power supply voltages of plus and minus 9 to 15 volts may be used. The signal voltages should be kept under about 3.5 V_{p-p} to maintain switch performance.

TABLE 1

Frequency (Hz)	Crosstalk (dB)	"Off" Isolation (dB)	THD
50	–74	-75	0.006
100	–74	–75	0.005
200	–74	–75	0.004
500	–74	–75	0.003
1	–74	–75	0.003
2	–73	–74	0.003
5	–70	–71	0.003
10	–67	–68	0.004
20	–62	–62	0.006
50	–55	–55	0.020
100	–50	–49	0.045

Signal voltages: 3 Vp-p

Supply voltages: ±12 volts

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FAX: 612-944-3794

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(612) 932-0600
FAX: 612-932-0613

Plymouth (55441)
Marshall Industries
3800 Annapolis Lane
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FAX: 612-559-8321

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12774 Boenker
(314) 291-4650
FAX: 314-291-5391

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Hamilton/Avnet, #05
13743 Shoreline Court
(314) 344-1200
FAX: 314-291-8889

NEW HAMPSHIRE

Manchester (03103)
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444 E. Industrial Park Drive
(603) 624-9400
TWX: 710-474-3255
FAX: 603-624-2402

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One Keystone Avenue
(609) 424-0100
TWX: 710-940-0262
FAX: 609-751-8624

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Hamilton/Avnet, #19
10 Industrial Road
(201) 575-3390
TWX: 710-734-4388
FAX: 201-575-5839

Fairfield (07006)
Marshall Industries
101 Fairfield Road
(201) 882-0320
TWX: 710-989-7052
FAX: 201-882-0095

Mt. Laurel (08054)
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158 Gaither Dr., Unit 100
(609) 234-9100 (NJ)
(215) 627-1920 (PA)
FAX: 609-778-1819

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Pioneer Std.
45 Route 46
(201) 575-3510
TWX: 710-734-4382
FAX: 201-575-3454

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11728 Linn N.E.
(505) 292-2700
FAX: 505-275-2819

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2524 Baylor Drive S.E.
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FAX: 505-243-1395

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Pioneer Std.
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(607) 722-9300
FAX: 607-722-9562

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(716) 887-2800
TWX: 710-522-1692
FAX: 716-887-2866

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Hamilton/Avnet, #08
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(516) 231-9800
FAX: 516-434-7426

Hauppauge (11787)
Marshall Industries
275 Oser Avenue
(516) 273-2424 and
(516) 273-2053
FAX: 516-434-4775

Johnson City (13790)
Marshall Industries
129 Brown Street
(607) 798-1611
FAX: 607-797-7031

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TWX: 710-567-1248
FAX: 914-937-2553

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2060 Town Line Road
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FAX: 516-737-4520

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FAX: 516-997-6375

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FAX: 704-522-8564

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FAX: 919-872-4435

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Marshall Industries
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FAX: 919-872-2431

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4800 E. 131st Street
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954 Senate Drive
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3520 Park Center Dr.
(513) 898-4480
TWX: 810-459-1735
FAX: 513-898-9636

Dayton (45424)
Pioneer Std.
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TWX: 810-459-1622
FAX: 513-236-8133

Dayton (45414)
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FAX: 513-454-0494

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30325 Bainbridge Rd., Bldg. A
(216) 349-3838
FAX: 216-349-1894

Solon (44139)
Marshall Industries
30700 Bainbridge Rd. Unit A
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FAX: 216-248-2312

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FAX: 614-882-8650

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12121 E. 51st St., Suite 102
(918) 252-7297
FAX: 918-250-8763

Tulsa (74146)
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3158 S. 108th E. Ave., Ste # 274
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FAX: 918-664-8515

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8333 S.W. Cirrus Dr.
(503) 644-5050
FAX: 503-646-8256

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5250 N.E. Elam Young Parkway
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(503) 640-6000
FAX: 503-640-5846

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6024 S.W. Jean Road
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261 Gibralter Road
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2800 Liberty Avenue, Bldg. E.
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FAX: 412-281-8662

Pittsburgh(15238)
Pioneer Std.
259 Kappa Drive
(412) 782-2300
TWX: 710-795-3122
FAX: 412-963-8255

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FAX: 512-339-6232

Austin (78754)
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(512) 837-1991
FAX: 512-832-9810

Austin (78758)
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1826D Kramer Lane
(512) 835-4000
FAX: 512-835-9829

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(512) 835-0220
FAX: 512-339-9252

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FAX: 512-837-0981

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Marshall Industries
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FAX: 214-770-0675

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Pioneer Std.
13710 Omega Road
(214) 386-7300
FAX: 214-490-6419

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(713) 895-9200
FAX: 713-462-6714

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FAX: 713-988-1732

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FAX: 214-234-4385

Stafford (77477)
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4850 Wright Road 190
(713) 240-7733
FAX: 713-240-0582

Sugarland (77478)
Quality Components
1005 Industrial Rd.
(713) 240-2255
FAX: 713-240-6988

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Salt Lake City (84119)
Hamilton/Avnet, #09
1585 West 2100 South
(801) 972-2800
FAX: 801-977-9266

Salt Lake City (84115)
Marshall Industries
466 Lawndale Dr., Ste. #C
(801) 485-1551
FAX: 801-487-0936

West Valley City (84119)
Wyle Laboratories-EMG
1325 W. 2200 S.
Ste. E
(801) 974-9953
FAX: 801-972-2524

WASHINGTON

Bothell (98011)
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11715 N. Creek Pkwy, South
Suite 112
(206) 486-5747
FAX: 206-486-6964

Redmond (98052)
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(206) 881-6697
FAX: 206-867-0159

Redmond (98052)
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15385 N.E. 90th Street
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FAX: 206-881-1567

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Bell
W227N913 W. Mound Dr.
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FAX: 414-547-6547

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20875 Crossroads Cir, Ste. 400
(414) 784-4510
FAX: 414-784-9509

Waukesha (53186)
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FAX: 414-797-8270

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TWX: 610-929-3065
FAX: 604-291-1227

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FAX: 604-294-1206

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Hamilton/Avnet, #60
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FAX: 613-226-1184

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(613) 820-8313
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FAX: 403-250-1591

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237 Hymus Boulevard
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TWX: 610-421-3251
FAX: 514-695-3707

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Hamilton/Avnet, #65
2795 Rue Halpern
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TWX: 610-421-3731
FAX: 514-335-2481

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B-1810 Wemmel
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Herlevang 13
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Dublin 10
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FAX: (1) 46.66.60.28

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FAX: (1) 46.30.01.29

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5 Rue Jean Zay
42271 St. Priest En Jarez Cedex
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TLX: 300021
FAX: (1) 77.93.26.31

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91940 Les Ulis
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TLX: 603351
FAX: (1) 64.46.95.95

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94523 Rungis Cedex
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TLX: 204674F
FAX: (1) 45.60.55.49

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7000 Stuttgart 70
TEL: (0711) 720010
TLX: 7255638
FAX: (0711) 7200132

EBV Elektronik GmbH
Øberweg 6
D-8025 Unterhaching
TEL: 089-61105-1
TLX: 524535
FAX: 089-61105-230

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Weimarstr 48
7000 Stuttgart 1
TEL: (0711) 61910-0
TLX: 722271
FAX: (0711) 613750

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4040 Neuss
TEL: (02101)530072
TLX: 8517605
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3006 Burgwedel 1 Hannover
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TLX: 923694

EBV Elektronik GmbH
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6000 Frankfurt M. 90
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TLX: 413590
FAX: (069) 7894458

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Königsbergerstrasse 16A
D. 1000 Berlin
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TLX: 184707

Ing. Büro K.H. Dreyer
Albert Schweitzer-Ring 36
2000 Hamburg 70
TEL: (040) 669027
TLX: 2164484

Ing. Büro K.H. Dreyer
Flensburger Strasse 3
2380 Schleswig
TEL: (04621) 24055
TLX: 221334

Ultratronik GmbH
Gewerbestr, 4
8036 Herrsching
TEL: (08152) 3709-0
TLX: 526459
FAX: (08152) 5183

ITALY

Dott Ing. Giuseppe De Mico
S.P.A.
20060 Cassina de Pecchi
Via Vittorio Veneto 8
Milano
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TLX: 330869
FAX: (02) 9522227

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Elektrotechniek BV
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NL-2600 AC Delft
TEL: 015-609906
TLX: 38250
FAX: 015-619194

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A/S Kjell Bakke
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P.O. Box 24
N-2001 Lillestrøm
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TLX: 19407
FAX: (06) 831455

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1100 Lisboa
TEL: (1) 534631, 540314, 561755
TLX: 64119

SPAIN

Redislogar S.A.
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28002 Madrid
TEL: (91) 413 91 11
TLX: 23967 JALO-E
FAX: (91) 416 19 71

Redislogar S.A.
Aragon 208-210
08011 Barcelona
TEL: (93) 254 90 48/49
FAX: (93) 323 4803

SWEDEN

Komponentbolaget NAXAB
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S-171-04 Solna
TEL: 08-985140
TLX: 17912 KOMP
FAX: 08-7645451

SWITZERLAND

Abalec A.G.
Grabenstrasse 9
8952 Schlieren
TEL: 01-730-0455
TLX: 59834
FAX: 01-730-9801

TURKEY

Türkelek Electronic Co. Ltd.
Hatay Sokak No. 8
Ankara
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TLX: 44580

UNITED KINGDOM

Abacus Electronics Ltd.
Abacus House
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Newbury, Berkshire RG14 5SF
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FAX: (0635) 38670
TLX: 847589

Abercorn Electronics Ltd.
Suite 1A
17 Waterloo Place
Edinburgh, Scotland EH1 3BG
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TLX: 727229
FAX: 031-556-7246

Barlec-Richfield Ltd.
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West Sussex RH13 5PX
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TLX: 877222
FAX: 0403-41746

Farnell Electronic
Components Ltd.
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Leeds LS12 2QQ
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TLX: 55147
FAX: 0532-633404

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7 West Pallant
Chichester
West Sussex P019 1TD
TEL: 0243-773511
TLX: 86230
FAX: 0243-779196

HB Electronics Ltd.
Lever Street
Bolton BL3 6BJ
TEL: (0204) 386361
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FAX: (0204) 384911

Hill Electronics
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TEL: 755611
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FAX: (06286) 66873

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159 High Street
West Drayton
Middlesex UB7 7XB
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TLX: 21958
FAX: 0895-422044

YUGOSLAVIA

Contact: Belram S.A.
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B-1150 Brussels, Belgium
TEL: 734-33-32, 734-26-19
TLX: 21790

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Piso 8 of. 41
1037 Buenos Aires
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241 Brown Road
Noble Park, Victoria 3174
TEL: 61-3-795 9011
TLX: AA31370
FAX: 61-3-795 6818

BRAZIL

Hitech
Av. Eng. Luiz Carlos Berrini
801 Conj. 111/121
04571 Brooklin
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Authorized U.S. Agent
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Miami, FL 33126
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FAX: (305) 593-1762

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Rm. 2001B Nam Fung Centre
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Tsuen Wan
N.T.
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CABLE: ARRAYEL
FAX: 0-4995803

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Unit 1009, 10/F
Conic Investment Bldg.
13 Hok Yuen St.
Hung Hom
Kowloon
TEL: 3-621833
TWX: 37119 ATEK HX
FAX: 3-7644782

Century Technology Co. Ltd.
Flat B-1 6/F., Tonic Industrial Ctr.
No. 19, Lam Hing Street
Kowloon Bay,
Kowloon
TEL: 3-7966683
TLX: 51226 CEPCO HX
FAX: 3-7998819
CABLE: CENTURYEPC

Dodwell Industrial
Electronics Division
8/F Tai Yau Bldg.
181 Johnston Road
Wanchai
TEL: 5-8616200/5-8315700
TLX: 66623 GILND HX
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Oriol Services &
Consultants Pvt. Ltd.
P. B. No. 9275
4, Kurla Industrial Estate
Narayan Nagar, L.B.S. Marg.
Ghatkopar, Bombay 400086
TEL: 512-2973 / 5113621
TLX: 011-72102

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Telsys Ltd.
Atidum Ind. Park, Bldg. 3
Dvora Hanevia St.
Neve Sharet
Tel-Aviv 61431
TEL: (3) 492001
TLX: 032392
FAX: (3) 497407

JAPAN

Tomen Electronics Corporation
1-1 Uchisaiwai-Cho, 2-Chome
Chiyoda-Ku, Tokyo 100
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FAX: 506-3479

KOREA

Buseok Trading Co.
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35 Yoido-Dong Youngdeungpo-Ku
Seoul
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TLX: K28742 KPTRDCO
FAX: (02) 7847702

Tong Baek Trading Co. Ltd.
Rm. #201 New Hanil Bldg.
156-1 Yumri-Dong
Mapo-Ku Seoul 121
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TLX: K28569 TBTRACO
FAX: (02) 7190818

MALAYSIA

GE Industries (M) Sdn Bhd
334 A-336A (First Floor)
Jalan Pudu
55100 Kuala Lumpur
TEL: 2410403/2488295
TLX: 2412689

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Ion Associates Inc.
1504 109th Street
(214) 647-8225
Easylink: 62956328
FAX: 214-641-9839

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Unit B, 192 Wairau Rd.
Glenfield
TEL: (09) 444 2645

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Alexan Commercial
812 Elcano Street
Binando
Manila
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TLX: 27484 CEI PH

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Carter Semiconductor (S) PTE Ltd.
07-03 Cuppage Centre
55 Cuppage Road
Singapore 0922 R.O.S.
TEL: 7347424
TLX: 36443 CARSIN
FAX: 734-2449

DOS Electronics PTE Ltd.
80 Genting Lane
No. 02-09 Genting Block
Ruby Ind. Complex
Singapore 1334, R.O.S.
TEL: 7433312
TLX: RS 35382 DOS
FAX: 743-7435

SOUTH AFRICA

Electrolink (PTY) Ltd.
P.O. Box 1020
Capetown 8000
TEL: 215-350
TLX: 527-7320

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CABLE: DONBC TAIPEI
FAX: (02) 763-1241

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Sukhumvit 63
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TLX: 82455 DYNASUP
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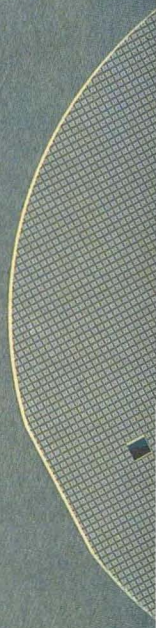

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